# Embedded System Design and Modeling
## EE382V, Unique 16985, Fall 2010

**Lectures**: TTh 3:30-5:00pm, ENS 109

**Instructor**: Andreas Gerstlauer <gerstl@ece.utexas.edu>
Office hours: T 5:00-6:00pm, W 2:00-4:00pm, ACE 6.118

**Class webpage**: http://www.ece.utexas.edu/~gerstl/ee382v_f10/

## Description

Embedded computer systems are ubiquitous, integrated into many devices we interact with on a daily basis. Driven by ever increasing application demands and technological advances that allow us to put complete multi-processor systems on a chip (MPSoCs), system complexities are growing exponentially. Together with tight constraints and market pressures, this makes the system design process a tremendous challenge and well-defined design methods and design automation techniques crucial to its success.

This course presents state-of-the-art methods, concepts, tools and techniques for system-level design and modeling of complete multi-processor systems from specification down to implementation across hardware-software boundaries. Using the SpecC and SystemC languages and the System-On-Chip Environment (SCE), we will specify, simulate, analyze, model and design systems based on examples of typical embedded applications.

## Prerequisites

- Embedded real-time system design and hardware/software interfacing
  (EE345M Embedded & Real-time Systems, or equivalent);
- Working knowledge of C/C++, algorithms and data structures
  (EE322C Data Structures, or equivalent);
- Digital hardware design and hardware description languages
  (EE360M Digital System Design using VHDL, or equivalent).

## Topics

Most likely covered in class at some point:
- Embedded systems, electronic system-level (ESL) design;
- System-level design languages (SLDLs): SpecC, SystemC;
- Models of Computation (MoCs): finite state machines (FSMs), dataflow, process networks, discrete event;
- System specification, profiling, analysis and estimation;
- System-level design: partitioning, scheduling, communication synthesis;
- System-level modeling: processor and RTOS modeling, transaction-level modeling (TLM) for communication;
- System-level synthesis: design space exploration (DSE);
- Embedded hardware and software implementation: synthesis and cosimulation;
- System design examples and case studies.

**Textbooks**

Required
1. D. D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, *Embedded System Design: Modeling, Synthesis, Verification*, ISBN 978-1-4419-0503-1, Springer, 2009.

Optional
2. A. Gerstlauer, R. Doemer, J. Peng, D. Gajski, *System Design: A Practical Guide with SpecC*, ISBN 0-7923-7387-1, Kluwer, 2001,.
3. T. Groetker, S. Liao, G. Martin, S. Swan, *System Design with SystemC*, ISBN 1-4020-7072-1, Kluwer, 2002.
4. F. Vahid, T. Givargis, *Embedded System Design: A Unified Hardware/Software Introduction*, ISBN 978-0-471-38678-0, John Wiley & Sons, 2001.

**Grading**

| | |
|---|---|
| Homeworks: | 15% |
| Labs: | 20% |
| Midterm: | 25% |
| Project: | 40% |

Late submissions will not be accepted. Oral discussion of homework problems is encouraged but make sure to submit your own individual and independent solution. Labs and final projects can be done in teams. Collaboration on projects is encouraged. Copying of any part of a solution without explicit reference to its source is plagiarism and considered cheating.

**Outline and Schedule (Tentative)**

| Week | Dates | Topic |
|---|---|---|
| 1 | Aug 26 | Introduction |
| 2 | Aug 31, Sep 2 | Design methodologies, models and languages |
| 3 | Sep 7, 9 | The SpecC System-Level Design Language |
| 4 | Sep 14, 16 | Models of computation: process-based |
| 5 | Sep 21, 23 | Models of computation: state-based |
| 6 | Sep 28, 30 | System specification and design |
| 7 | Oct 5, 7 | Computation modeling and refinement |
| 8 | Oct 12, 14 | Communication modeling and refinement |
| 9 | Oct 19, 21 | System Modeling, Review |
| 10 | Oct 26, 28 | **Midterm**, Guest lecture |
| 11 | Nov 2, 4 | The SystemC system-level design language |
| 12 | Nov 9, 11 | System synthesis and design space exploration |
| 13 | Nov 16, 18 | Electronic system-level design tools and design studies |
| 14 | Nov 23, 25 | Review and wrapup, *Thanksgiving holiday* |
| 15 | Nov 30, Dec 2 | **Project presentations** |

**Electronic Mail Notification Policy**

In this course e-mail will be used as a means of communication with students. You will be responsible for checking your e-mail regularly for class work and announcements. The complete text of the University electronic mail notification policy and instructions for updating your e-mail address are available at http://www.utexas.edu/its/policies/emailnotify.html.

**Use of Blackboard and Class Web Site**

This course uses the class web page and Blackboard to distribute course materials, to communicate and collaborate online, to submit assignments and to post solutions and grades. You will be responsible for checking the class web page and the Blackboard course site regularly for class work and announcements. As with all computer systems, there are occasional scheduled downtimes as well as unanticipated disruptions. Notification of disruptions will be posted on the Blackboard login page. Scheduled downtimes are *not* an excuse for late work. However, if there is an unscheduled downtime for a significant period of time, I will make an adjustment if it occurs close to the due date.

**Students with Disabilities**

The University of Texas at Austin provides upon request appropriate academic accommodations for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4641 TTY or the College of Engineering Director of Students with Disabilities at 471-4382.

**Religious Holidays**

Religious holy days sometimes conflict with class and examination schedules. If you miss an examination, work assignment, or other project due to the observance of a religious holy day you will be given an opportunity to complete the work missed within a reasonable time *after* the absence. It is the policy of The University of Texas at Austin that you must notify each of your instructors at least fourteen days prior to the classes scheduled on dates you will be absent to observe a religious holy day.