System Design Issues in Embedded Processing

9/16/10

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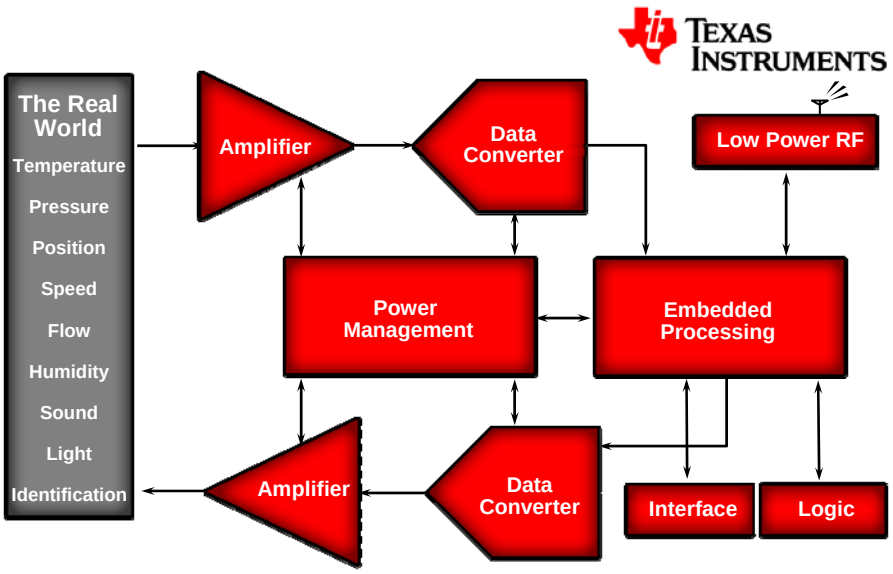
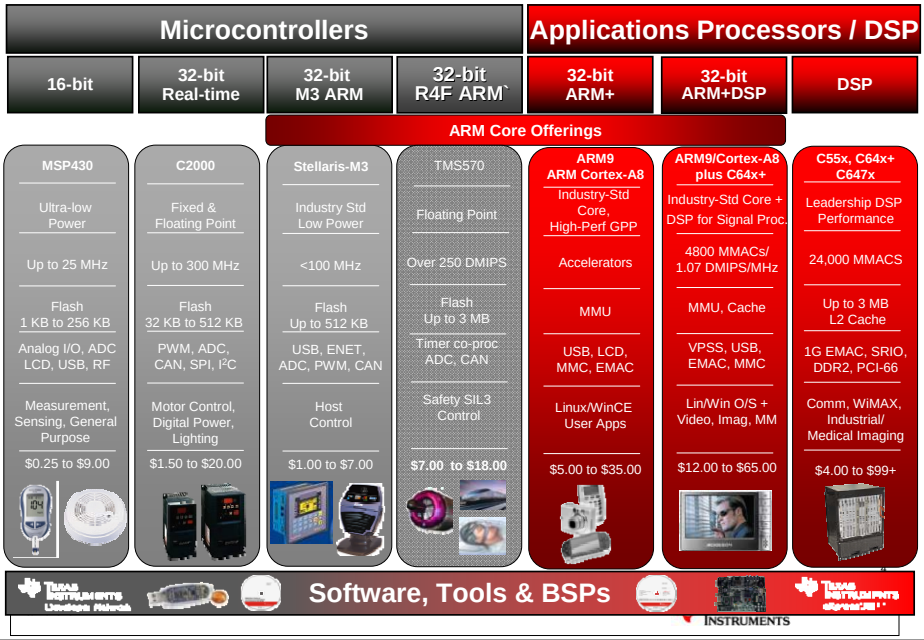
Agenda

- What does TI do?
- From MCU to MPU to DSP: What are some trends?
- Design Challenges
- Tools to Help

TI - the complete system



TI Embedded Processing Portfolio



Design Goals / Trends

Customer	TI
• Size	• Innovative packaging, on chip integration
• Cost	• Efficient manufacturing, lower process geometries
• Power (Battery Life, Green)	• Lowest power processor, wide operating range, fast wake-up
• Performance	• High speed, architecture break-throughs, multicore, hardware accelerators

Trends and Issues

• Size	• Integration = Software complexity • Packaging = Manufacturing concerns (flow temp)
• Cost	• Process geometry = EMI, Analog interface, leakage current
• **Power (Battery Life, Green)**	• Low Power = Power backplane issues, lead-free • Efficient computing = Fast wake-up, interrupt programming, RTOS
• Performance	• Multicore= task sharing, scheduling, hardware

Design Issue: Low Power

- Complex Power backplane – different parts of SoC operate at different voltages
- Intelligent peripherals – DMA, Transfer, wake up CPU, Bus, Cache, etc.
- Complex Clocking – run different parts at different frequencies
- Low Voltage
- Leakage Currents

WHY LOW VOLTAGE??

Advantage

Power ~ CV^2f_c

Energy per Conversion ~ CV^2

If Voltage is reduced from 1.2V => 0.4V, energy per operation is reduced by 10X!!!

Problem

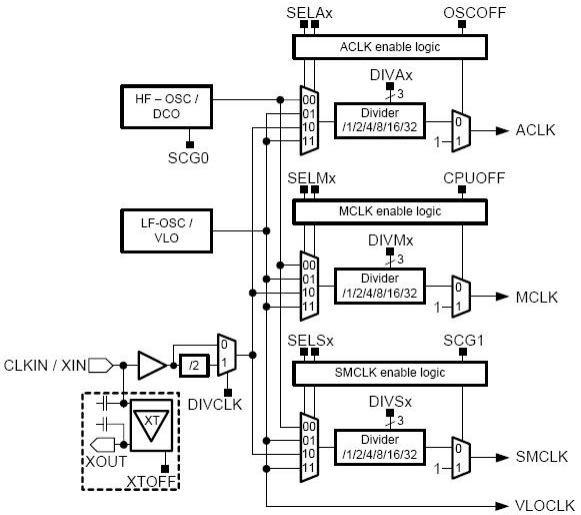
Speed at low voltage is reduced

- 100 MHz @ 1.2V
- 10 MHz @ 0.5V

Compact Clock System (CCS)

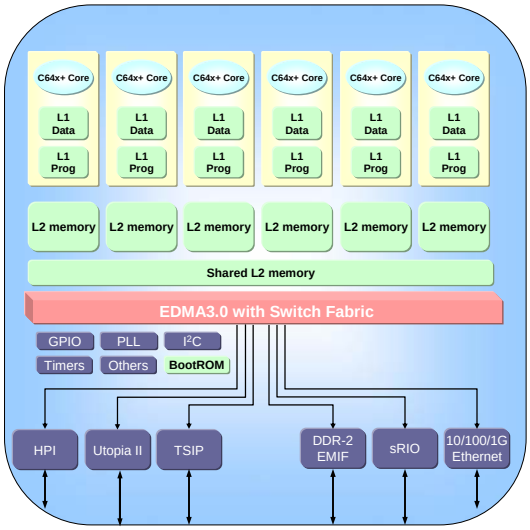
3 clock sources

- HFCLK in the 1MHz range, trimmed to 3% accuracy
- LFCLK in the 20kHz range used in low power modes
- External clock supporting up to 4MHz



TMS320C6472

Power Optimized, High Performance Multicore Processor



- **Six C64x+ DSP Core @ 500/625/700 MHz**
  - 16/32 bit ISA, SPLoop, more MPY, …
- **Memory**
  - 32 KB L1 program RAM
  - 32 KB L1 data RAM
  - 608 KB local L2 RAM
  - 768 KB shared L2 RAM
  - 768 KB shared L2 ROM
    - Boot ROM
  - DDR2 (32-bit) EMIF
- **Communications Subsystem**
  - 2x sRIO
  - 2x 10/100/1000 Ethernet
  - 3x Telecom serial ports (3072 timeslots)
  - UTOPIA II
  - I²C
  - Host port
- 90nm process
- 737 pin, 24x24mm FC-BGA, 0.8 pitch
- **EVM and Samples available now for NDA customers**
- **EVM and Samples available for broad market in 1Q09**

BeagleBoard Gives You a PC in your Pocket

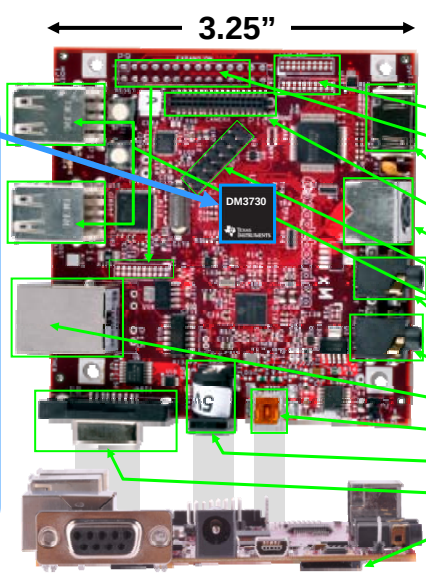
Laptop-like performance

TI DM3730 (AM37x-compatible)

- 1 GHz superscaler ARM® Cortex ™-A8
- More than 2,000 Dhrystone MIPS
- Up to 20 Million polygons per sec graphics
- HD video capable C64x+™ DSP core

Memory

- 512 MB LPDDR RAM



USB & standard PC expansion

- LCD Expansion
- I²C, I²S, SPI, MMC/SD Expansion
- DVI-D
- Camera Header
- S-Video
- JTAG
- USB Hosts
- Stereo Out
- Stereo In
- 10/100 Ethernet
- USB 2.0 HS OTG*
- Alternate Power
- RS-232 Serial*
- Micro-SD Slot*

beagleboard.org

* Supports booting from this peripheral

Some Design Tools – FREE! Online!

- TINA-TI – design and simulation tool
- Selection Tools – MCU and DSP – find the right part and sample
- SwitcherPRO – Design Power supply
- FilterPRO – design a filter
- Code Examples – get the verified code
- GraCE – graphical programming
- Ti.com

GraCE: Graphical Programming