

System Design Issues in Embedded Processing

9/16/10

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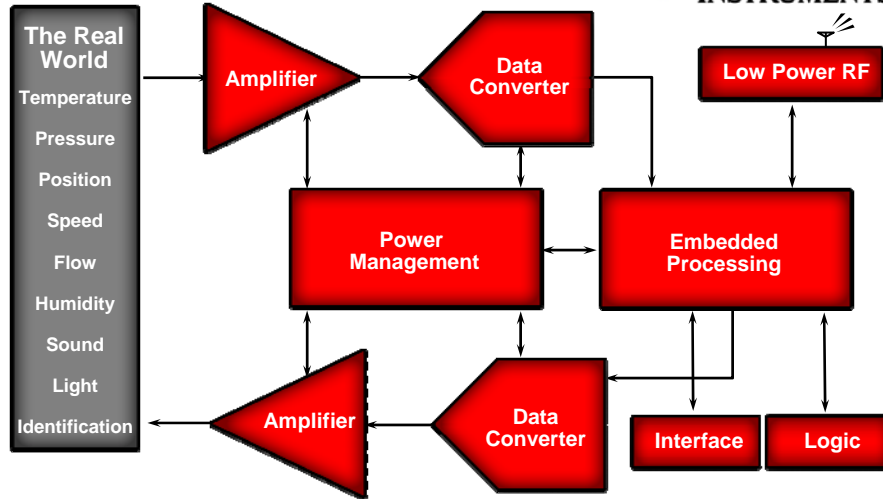
Agenda

- What does TI do?
- From MCU to MPU to DSP: What are some trends?
- Design Challenges
- Tools to Help

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TI - the complete system



TI Embedded Processing Portfolio

Microcontrollers				Applications Processors / DSP		
16-bit	32-bit Real-time	32-bit M3 ARM	32-bit R4F ARM*	32-bit ARM+	32-bit ARM+DSP	DSP
ARM Core Offerings						
MSP430 Ultra-low Power Up to 25 MHz Flash 1 KB to 256 KB Analog I/O, ADC, LCD, USB, RF Measurement, Sensing, General Purpose \$0.25 to \$9.00	C2000 Fixed & Floating Point Up to 300 MHz Flash 32 KB to 512 KB PWM, ADC, CAN, SPI, I ² C Motor Control, Digital Power, Lighting \$1.50 to \$20.00	Stellaris-M3 Industry Std Low Power <100 MHz Flash Up to 512 KB USB, ENET, ADC, PWM, CAN Host Control \$1.00 to \$7.00	TMS570 Floating Point Over 250 DMIPS Flash Up to 3 MB Timer co-processor, ADC, CAN Safety SIL3 Control \$7.00 to \$18.00	ARM9 ARM Cortex-A8 Industry-Std Core, High-Perf GPP Accelerators MMU USB, LCD, MMC, EMAC Linux/WinCE User Apps \$5.00 to \$35.00	ARM9/Cortex-A8 plus C64x+ Industry-Std Core + DSP for Signal Proc. 4800 MMACS/1.07 DMIPS/MHz MMU, Cache VPSS, USB, EMAC, MMC Lin/Win O/S + Video, Imag, MM \$12.00 to \$65.00	C55x, C64x+ C647x Leadership DSP Performance 24,000 MMACS Up to 3 MB L2 Cache 1G EMAC, SRIO, DDR2, PCI-66 Comm, WiMAX, Industrial/Medical Imaging \$4.00 to \$99+



Software, Tools & BSPs



INSTRUMENTS

Design Goals / Trends

Customer

- Size
- Cost
- Power (Battery Life, Green)
- Performance

TI

- Innovative packaging, on chip integration
- Efficient manufacturing, lower process geometries
- Lowest power processor, wide operating range, fast wake-up
- High speed, architecture breakthroughs, multicore, hardware accelerators



Trends and Issues

- Size
- Cost
- **Power (Battery Life, Green)**
- Performance

- Integration = **Software complexity**
- Packaging = Manufacturing concerns (flow temp)
- Process geometry = EMI, Analog interface, leakage current
- Low Power = **Power backplane issues**, lead-free
- Efficient computing = Fast wake-up, interrupt programming, **RTOS**
- **Multicore**= task sharing, scheduling, hardware



Design Issue: Low Power

- Complex Power backplane – different parts of SoC operate at different voltages
- Intelligent peripherals – DMA, Transfer, wake up CPU, Bus, Cache, etc.
- **Complex Clocking** – run different parts at different frequencies
- **Low Voltage**
- Leakage Currents

TI Proprietary Information - Strictly Private or similar placed here if applicable

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WHY LOW VOLTAGE??

Advantage

Power $\sim CV^2f_c$

Energy per Conversion $\sim CV^2$

If Voltage is reduced from 1.2V \Rightarrow 0.4V, energy per operation is reduced by 10X!!!

Problem

Speed at low voltage is reduced

- 100 MHz @ 1.2V

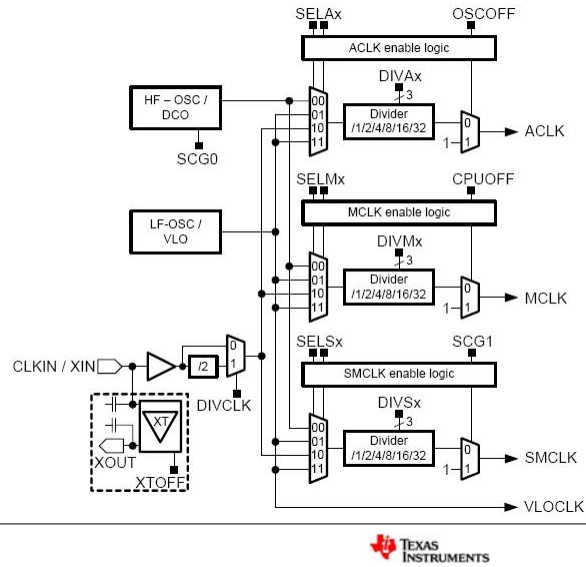
- 10 MHz @ 0.5V



Compact Clock System (CCS)

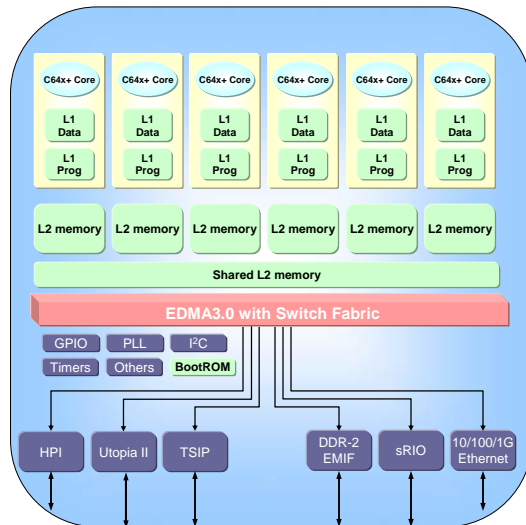
3 clock sources

- HFCLK in the 1MHz range, trimmed to 3% accuracy
- LFCLK in the 20kHz range used in low power modes
- External clock supporting up to 4MHz



TMS320C6472

Power Optimized, High Performance Multicore Processor



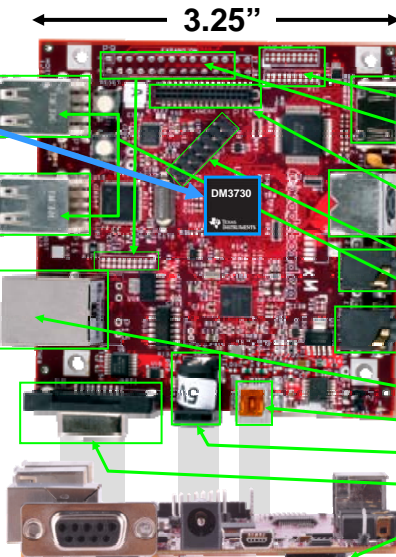
- **Six C64x+ DSP Core @ 500/625/700 MHz**
 - 16/32 bit ISA, SLoop, more MPY, ...
- **Memory**
 - 32 KB L1 program RAM
 - 32 KB L1 data RAM
 - 608 KB local L2 RAM
 - 768 KB shared L2 RAM
 - 768 KB shared L2 ROM
 - Boot ROM
 - DDR2 (32-bit) EMIF
- **Communications Subsystem**
 - 2x sRIO
 - 2x 10/100/1000 Ethernet
 - 3x Telecom serial ports (3072 timeslots)
 - UTOPIA II
 - iPC
 - Host port
- 90nm process
- 737 pin, 24x24mm FC-BGA, 0.8 pitch
- **EVM and Samples available now for NDA customers**
- **EVM and Samples available for broad market in 1Q09**

BeagleBoard Gives You a PC in your Pocket

Laptop-like performance

TI DM3730 (AM37x-compatible)

- 1 GHz superscaler ARM® Cortex™-A8
- More than 2,000 Dhrystone MIPS
- Up to 20 Million polygons per sec graphics
- HD video capable C64x™ DSP core
- 512 MB LPDDR RAM



USB & standard PC expansion

- LCD Expansion
- I²C, I²S, SPI, MMC/SD Expansion
- DVI-D
- Camera Header
- S-Video
- JTAG
- USB Hosts
- Stereo Out
- Stereo In
- 10/100 Ethernet
- USB 2.0 HS OTG*
- Alternate Power
- RS-232 Serial*
- Micro-SD Slot*

beagleboard.org

* Supports booting from this peripheral



Some Design Tools – FREE! Online!

- TINA-TI – design and simulation tool
- Selection Tools – MCU and DSP – find the right part and sample
- SwitcherPRO – Design Power supply
- FilterPRO – design a filter
- Code Examples – get the verified code
- GraCE – graphical programming
- Ti.com

GraCE: Graphical Programming

The screenshot displays the Code Composer Studio (CCS) interface for a project named "temperature.clg". The main window shows the "USCI_A0 - Power User Mode" configuration page, which is part of the GraCE (Graphical Programming) tool. The interface includes several tabs: "Overview", "Basic User", "Power User", and "Registers". The "Overview" tab is active, showing a block diagram of the USCI_A0 module in UART Mode. The block diagram includes a "Clock source" section with "SMCLK" and "BRCLK" options, and a "UART Mode" section with "UCxRX" and "UCxTX" pins. The "UCxRX" pin is connected to "P3.5/UCAR-D/UCARSDMI" and the "UCxTX" pin is connected to "P3.4/UCART-D/UCARTSDMI". Below the block diagram is a timing diagram showing the UART signal waveform. The waveform starts with a "Start" bit, followed by data bits "D0", "D1", and "Dn". The "8 bit" field is set to "8 bit", the "Parity" field is set to "None", and the "Stop" field is set to "One". The baud rate is set to "115200 bps" and the transmit time is $t_{\text{bit}} = 8.7 \mu\text{s}$. The "Transmit Interrupt" checkbox is unchecked. The "Problems" window at the bottom shows "0 errors, 0 warnings, 0 infos".

Available Packages:

- MSP430 CSL
- CSL
- Peripherals
 - ADC10
 - Clock2xx
 - GPIO
 - GA
 - TimerA3
 - TimerB0
 - USCI_A0
 - USCI_B0
 - WDTPlus
- XDCtools

Description	Resource	Path	Location