System-on-a-Chip (SoC) Design

EE382V, Fall 2014

Homework #3

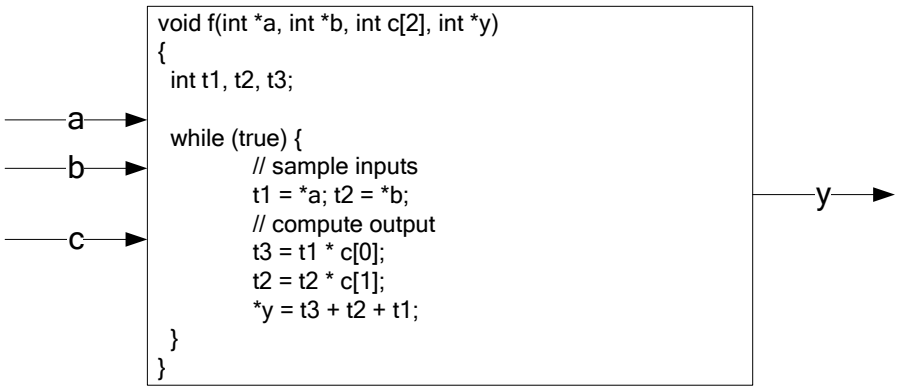
Assigned: October 16, 2014
Due: November 2, 2014

Instructions:

- Please submit your solutions via Canvas. Submissions should include a single PDF with the writeup and single Zip or Tar archive for source code.
- You may discuss the problems with your classmates but make sure to submit your own independent and individual solutions.

Problem 1: High-Level Synthesis (100 points)

Consider the following system:



Assume a datapath resource constraint of one adder and one multiplier, where the adder requires one clock cycle while the multiplier is pipelined with a latency (delay) of two cycles and a throughput of one operation per cycle (i.e. a data introduction interval of 1).

(a) Derive a minimal-latency schedule for one iteration of the loop body inside *f* . How many cycles does it take to compute 100 output values?

(b) Unroll the loop inside *f* one time and derive a minimal-latency schedule for one iteration of the new loop (which will contain two iterations of the original loop). How many cycles does it take to compute 100 output values?

(c) Instead of unrolling, pipeline the loop and derive a minimal-latency schedule for the pipelined loop body. Show the schedule for at least two overlapping loop iterations. What is the smallest loop introduction interval (II) that can be achieved? How many cycles does it take to compute 100 output values?

(d) Use the left-edge algorithm to determine a minimal set of registers and a corresponding register binding for your solution from (a).

(e) For your implementation in (d), draw a multiplexer-based realization of your final datapath and show the state machine of the controller driving the datapath computation.