# Embedded System Design and Modeling

**EE382V, Unique 17303, Spring 2014**

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**Lectures**: TTh 11:00-12:30pm, WEL 3.402

**Instructor**: Andreas Gerstlauer <gerstl@ece.utexas.edu>
Office hours: TW 2:00-3:00pm, ACE 6.118

**Teaching Assistant**: Parisa Razaghi <parisa.r@utexas.edu>
Office hours: TBD

**Class webpage**: http://www.ece.utexas.edu/~gerstl/ee382v_s14/

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## Description

Embedded computer systems are ubiquitous, integrated into many devices we interact with on a daily basis. With ever increasing application demands and advances in semiconductor technology, such systems are more than ever realized as application-specific, heterogeneous multi-processor systems-on-chip (MPSoCs). Exponentially growing complexities, tight constraints and rising chip design costs, however, have made traditional implementation approaches infeasible and instead demand novel, well-defined and formal methods for programming and design of complete systems across hardware and software boundaries.

This course covers theory and practice of system-level design of embedded multi-processor and multi-core systems. Focusing on the necessary modeling foundations to enable design automation, the course will present state-of-the-art methods and techniques for specification, synthesis and performance modeling at the system level. In the labs, the SpecC and SystemC languages and the System-On-Chip Environment (SCE) will be used to specify, simulate, analyze, model and synthesize systems based on typical embedded application examples.

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## Prerequisites

- Embedded real-time system design and hardware/software interfacing (EE345M/EE380L.6 Embedded & Real-time Systems, or equivalent);
- Working knowledge of C/C++, algorithms and data structures (EE322C Data Structures, or equivalent);
- Digital hardware design and hardware description languages (EE360M Digital System Design using VHDL, or equivalent).

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## Topics

Most likely covered in class at some point:

- Embedded systems, electronic system-level (ESL) design and design methodologies;
- System-level design languages (SLDLs): SpecC, SystemC;
- Models of Computation (MoCs), concurrency and time: finite state machines (FSMs), parallel programming models, threads, process networks, dataflow, discrete event;
- System specification, profiling, analysis and estimation;
- System-level synthesis: algorithms for mapping, scheduling and design space exploration;
- System refinement, virtual platform prototyping and system simulation: processor and RTOS modeling, transaction-level modeling (TLM) for communication;
- Embedded hardware and software implementation: synthesis and co-simulation;
- System-level design tools, examples and case studies.

## Textbooks

Recommended

1. D. D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, *Embedded System Design: Modeling, Synthesis, Verification*, ISBN 978-1-4419-0503-1, Springer, 2009.

Optional

2. E. A. Lee, S. Seshia, *Introduction to Embedded Systems: A Cyber-Physical Systems Approach*, ISBN 978-0-557-70857-4, 2011.
3. A. Gerstlauer, R. Doemer, J. Peng, D. Gajski, *System Design: A Practical Guide with SpecC*, ISBN 0-7923-7387-1, Kluwer, 2001,.
4. T. Groetker, S. Liao, G. Martin, S. Swan, *System Design with SystemC*, ISBN 1-4020-7072-1, Kluwer, 2002.

## Grading

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|---|---|
| Homeworks: | 20% |
| Labs: | 20% |
| Midterm: | 25% |
| Project: | 35% |

Late submissions will not be accepted. Oral discussion of homework problems is encouraged but make sure to submit your own individual and independent solution. Labs and final projects can be done in teams. Collaboration on projects is encouraged. Copying of any part of a solution without explicit reference to its source is plagiarism and considered cheating.

## Outline and Schedule (Tentative)

| Week | Dates | Topic |
|---|---|---|
| **1** | Jan 14, 16 | Introduction: embedded systems, design methodologies |
| **2** | Jan 21, 23 | The SpecC and SystemC system-level design languages |
| **3** | Jan 28, 30 | System specification: semantics, concurrency, time |
| **4** | Feb 4,6 | Models of computation: process-based, KPNs, dataflow |
| **5** | Feb 11, 13 | Models of computation: state-based, FSMs |
| **6** | Feb 18, 20 | System-level synthesis: multi-processor mapping and scheduling |
| **7** | Feb 25, 27 | Performance estimation and evaluation, system refinement |
| **8** | Mar 4, 6 | Design space exploration |
| | Mar 11, 13 | *Spring Break* |
| **9** | Mar 18, 20 | Review, **Midterm** |
| **10** | Mar 25, 27 | Virtual platform prototyping, system simulation |
| **11** | Apr 1, 3 | Computation refinement and modeling |
| **12** | Apr 8, 10 | Communication refinement, transaction-level modeling |
| **13** | Apr 15, 17 | System implementation, hardware/software synthesis |
| **14** | Apr 22, 24 | Electronic system-level design tools and design studies |
| **15** | Apr 29, May 1 | **Project presentations** |

**Electronic Mail Notification Policy**

In this course e-mail will be used as a means of communication with students. You will be responsible for checking your e-mail regularly for class work and announcements. The complete text of the University electronic mail notification policy and instructions for updating your e-mail address are available at http://www.utexas.edu/its/policies/emailnotify.html.

**Use of Blackboard and Class Web Site**

This course uses the class web page and Blackboard to distribute course materials, to communicate and collaborate online, to submit assignments and to post solutions and grades. You will be responsible for checking the class web page and the Blackboard course site regularly for class work and announcements. As with all computer systems, there are occasional scheduled downtimes as well as unanticipated disruptions. Notification of disruptions will be posted on the Blackboard login page. Scheduled downtimes are *not* an excuse for late work. However, if there is an unscheduled downtime for a significant period of time, I will make an adjustment if it occurs close to the due date.

**Students with Disabilities**

The University of Texas at Austin provides upon request appropriate academic accommodations for qualified students with disabilities. For more information, contact the Services for Students with Disabilities (SSD) at 471-5259, http://ddce.utexas.edu/disability/.

**Religious Holidays**

Religious holy days sometimes conflict with class and examination schedules. If you miss an examination, work assignment, or other project due to the observance of a religious holy day you will be given an opportunity to complete the work missed within a reasonable time after the absence. It is the policy of The University of Texas at Austin that you must notify each of your instructors at least fourteen days prior to the classes scheduled on dates you will be absent to observe a religious holy day.