Graphical System Design

Jacob Kornerup, Ph.D.
LabVIEW R&D
National Instruments

About me

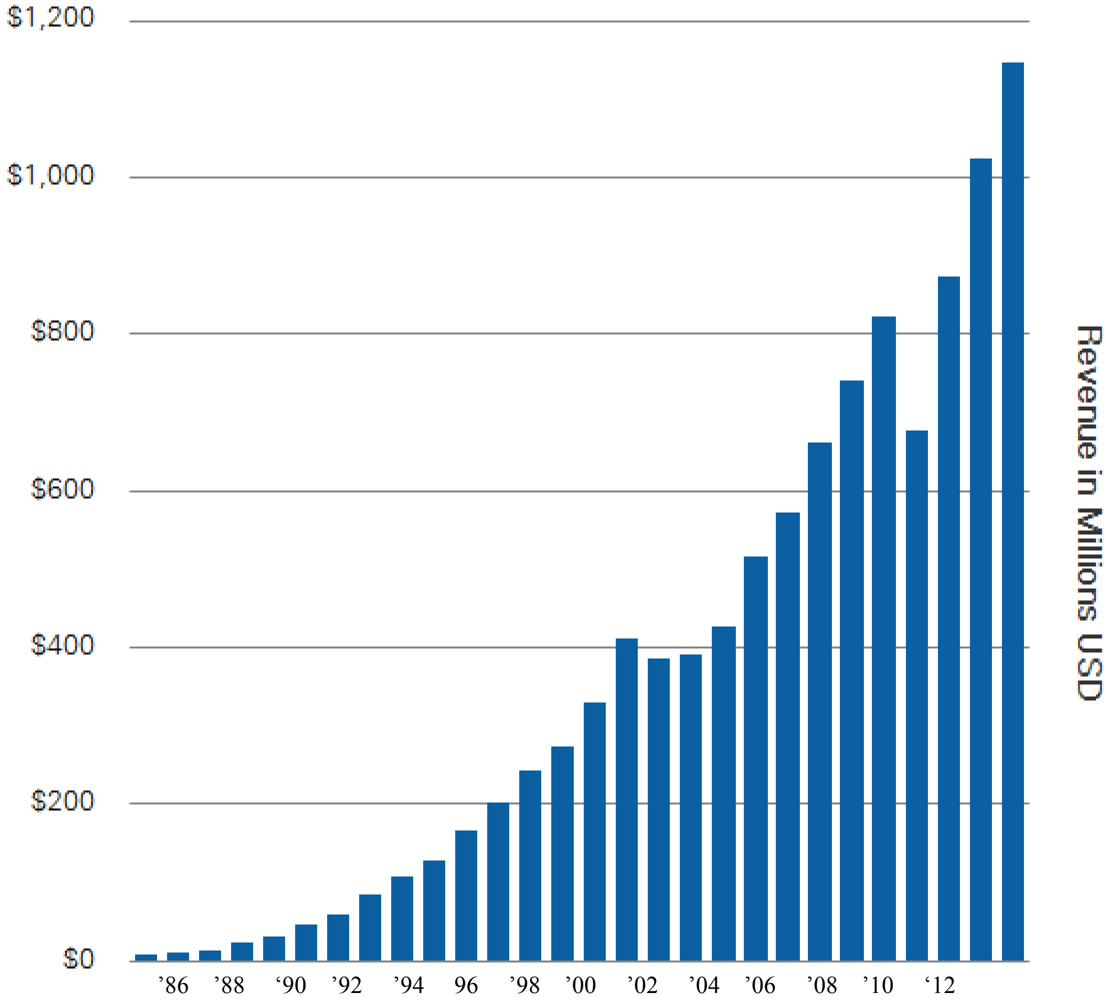
- Ph.D. UT Computer Sciences 1997
  - Parallel, functional programming
- Assistant Professor 1997-99
  - ECE Dept. SMU, Dallas
- Principal SW Architect, National Instruments, 1999 -
  - Real-time systems
  - Programming with time
  - Real-time networking
  - Models of Computation
  - High Level Synthesis for FPGAs
  - Research projects with Drs. Gerstlauer and Evans

Agenda for Today

- Embedded system design
- Platform based design
- Models of Computation
- Real-time streaming applications
- System design tools

National Instruments

- **Revenue:** $1.14 Billion in 2013
- **Global Operations:** Approximately 6,870 employees; operations in more than 40 countries
- **Broad customer base**: More than 35,000 companies served annually
- **Diversity**: No industry >15% of revenue
- **Culture**: Ranked among top 25 companies to work for worldwide by the Great Places to Work Institute



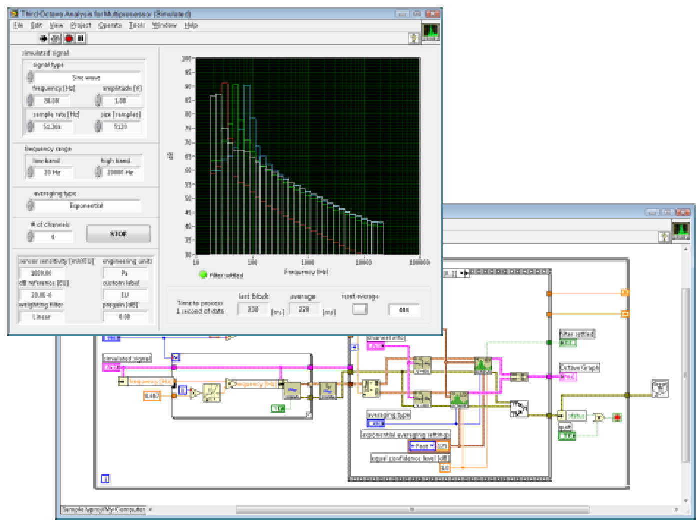
We Enable Graphical System Design

LEGO® MINDSTORMS ® NXT EV3

From K…

POWERED BY

NATIONAL INSTRUMENTS LabVIEW™

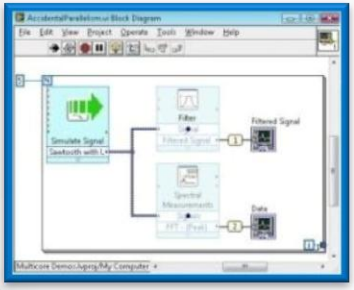


SPACEX

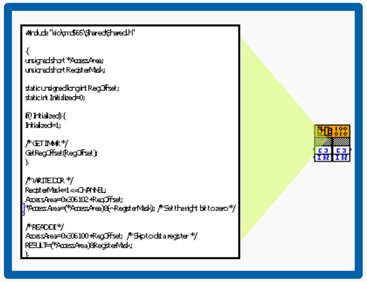
… to Rocket Science

High-Level Design Models

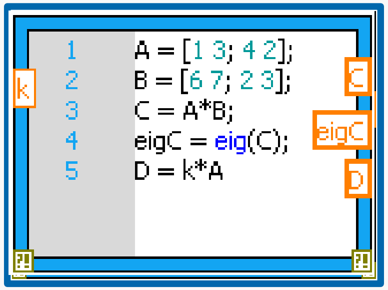
Data Flow



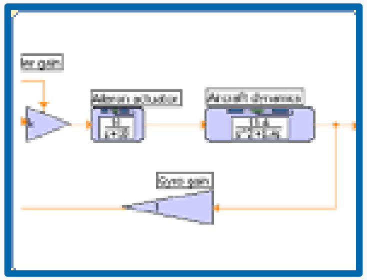
C Code



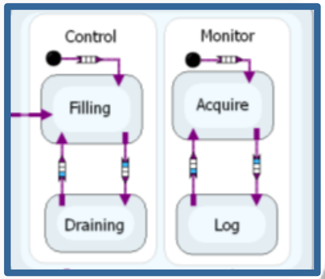
Textual Math



Simulation



Statechart



NATIONAL INSTRUMENTS LabVIEW™

Graphical System Design Platform

PC/Mac/Linux

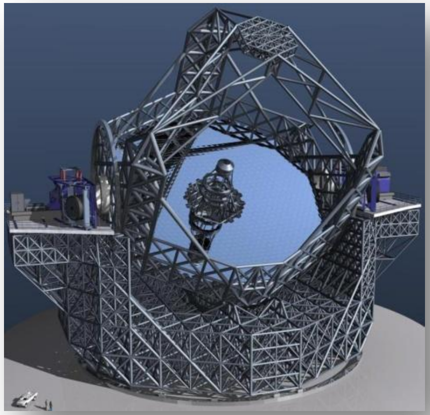
PXI

CompactRIO

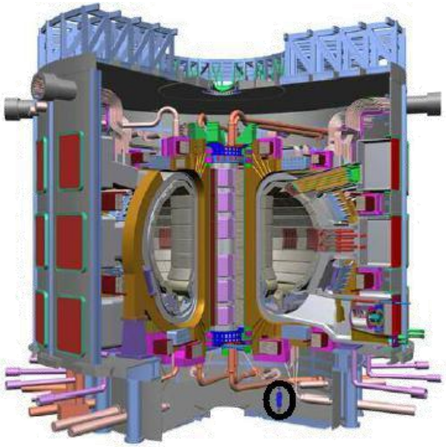
FlexRIO

Custom

Tough Real-Time Challenges

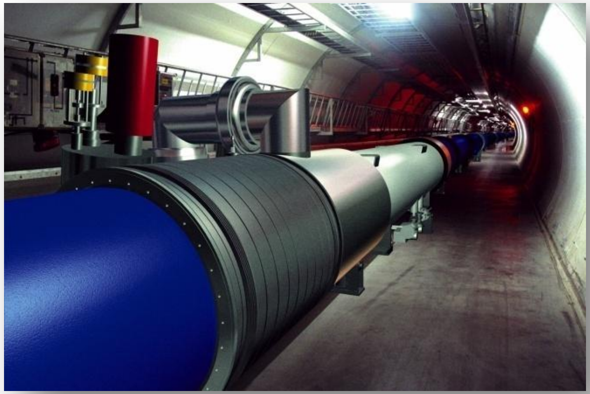


Large Telescope Mirror Control

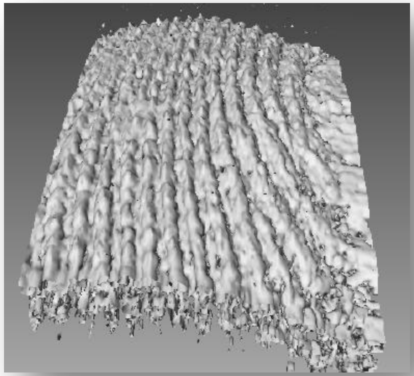


Tokomak Plasma Control

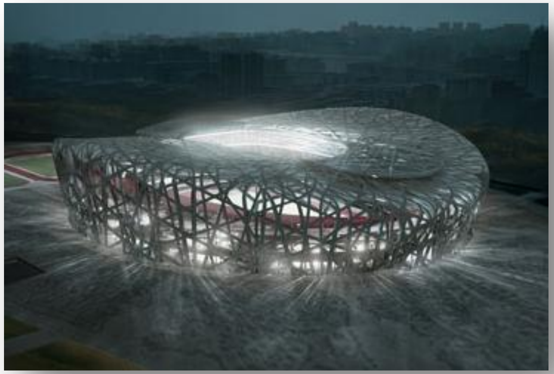
Wind Turbine Sound Source Characterization



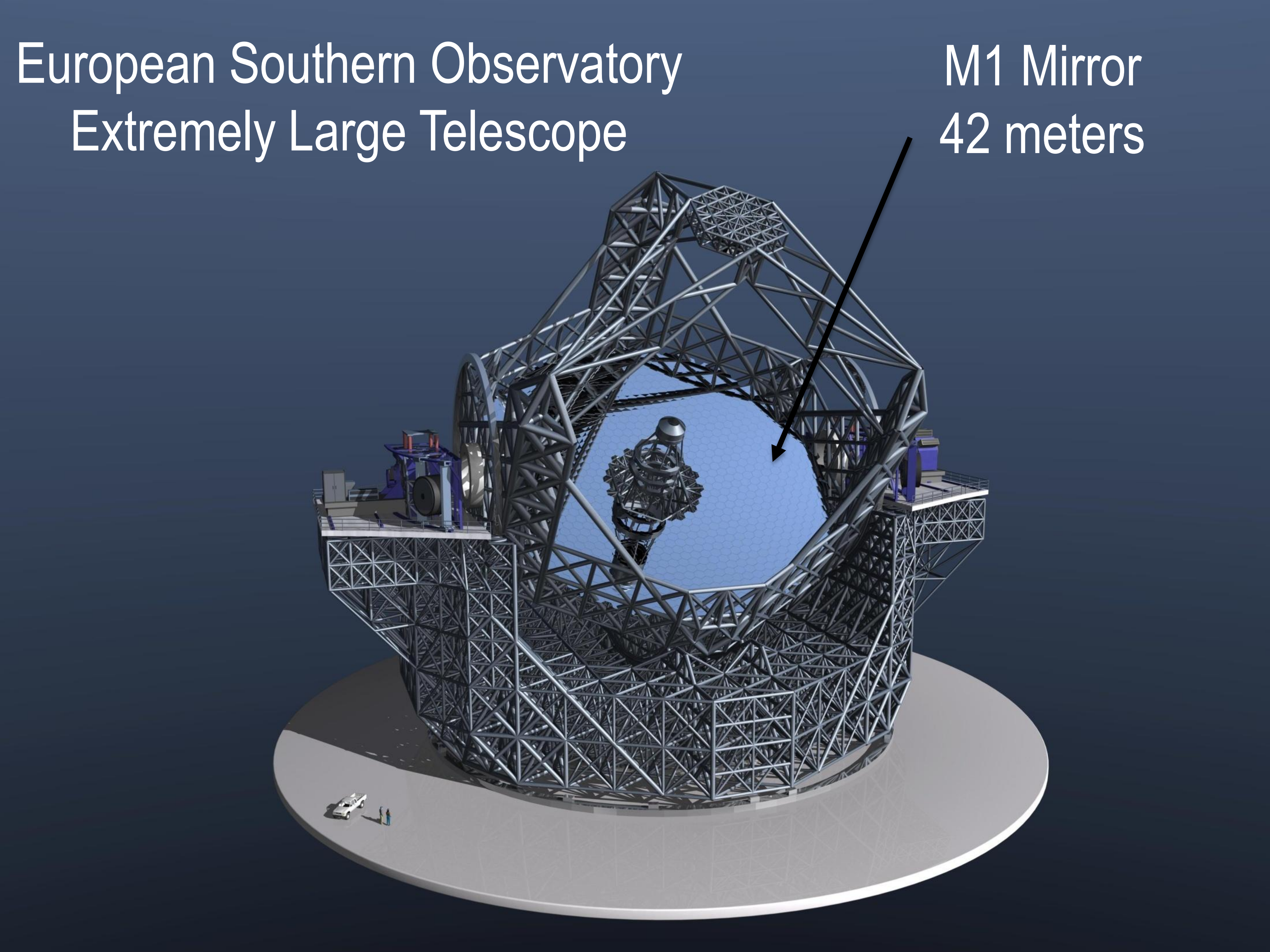
CERN Hadron Collider



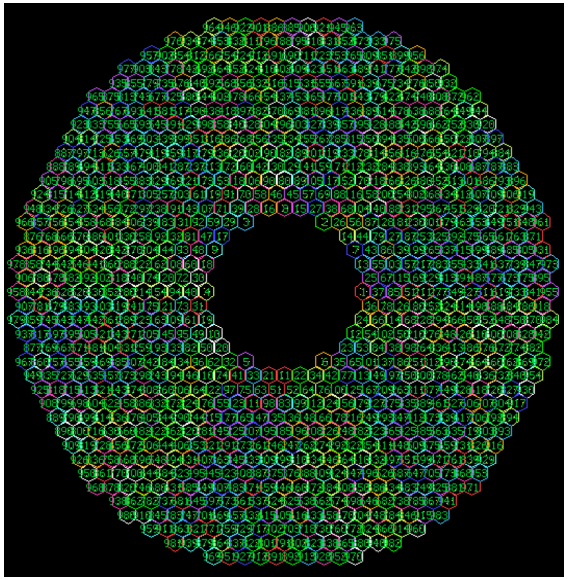
Early Cancer Detection

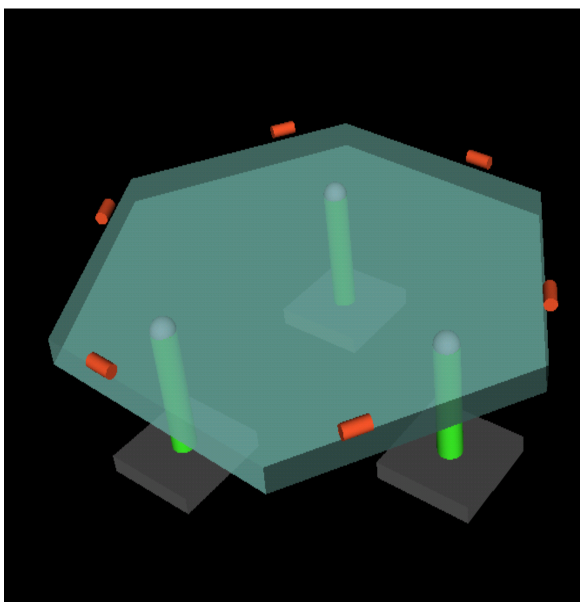


Structural Health Monitoring


European Southern Observatory
Extremely Large Telescope
M1 Mirror
42 meters

ESO ELT M1 Mirror Control





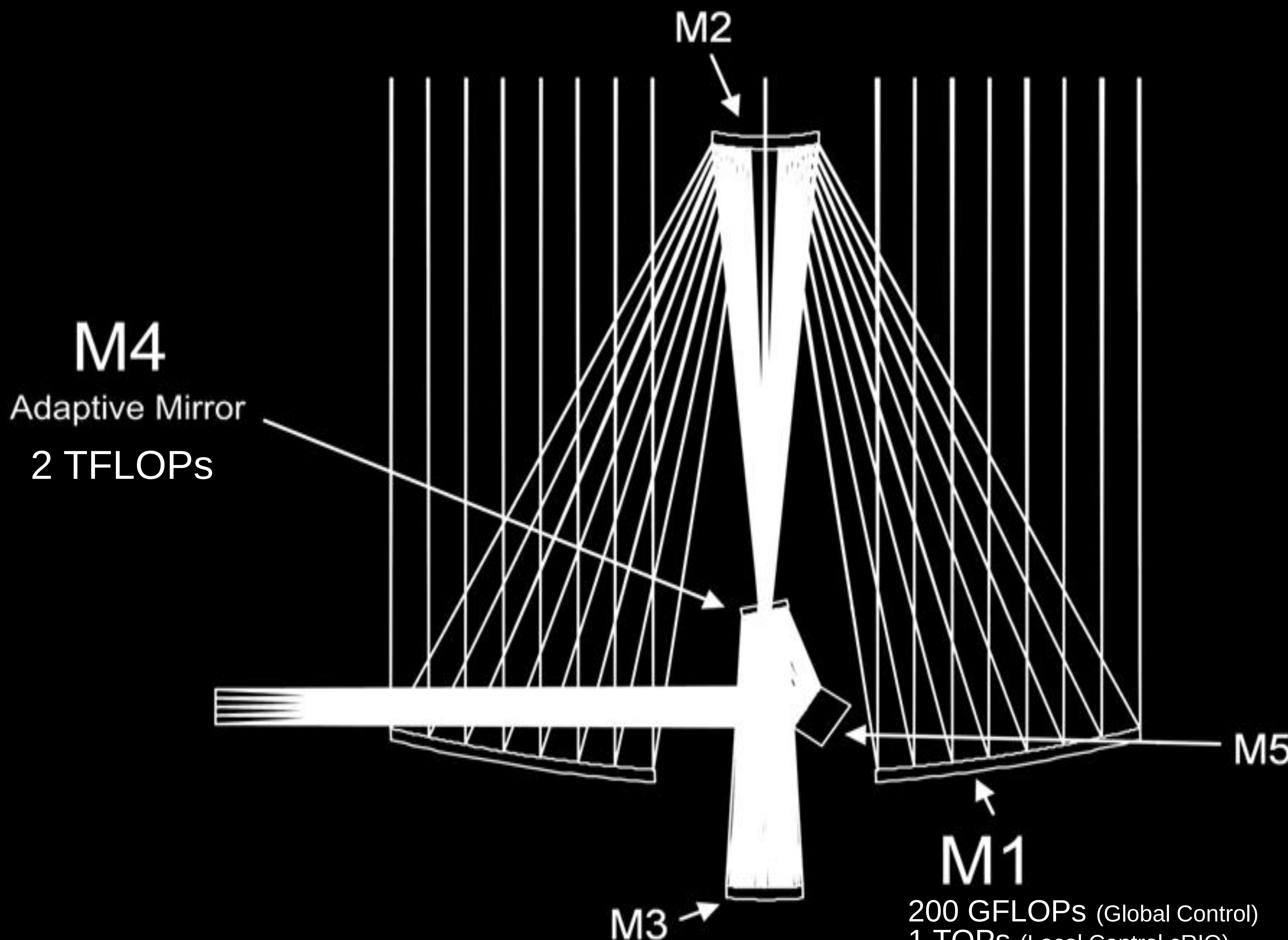
984 MIRRORS

3,000 ACTUATORS

6,000 SENSORS

3k x 6k MATRIX

1 MILLISECOND

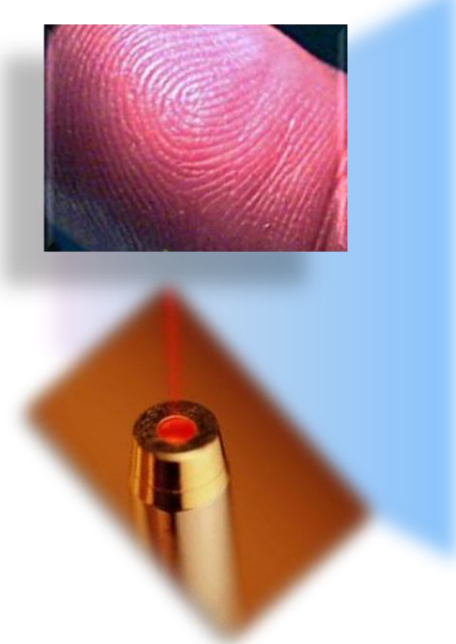

M2
M4
Adaptive Mirror
2 TFLOPs
M5
M1
200 GFLOPs (Global Control)
1 TOPs (Local Control cRIO)
M3

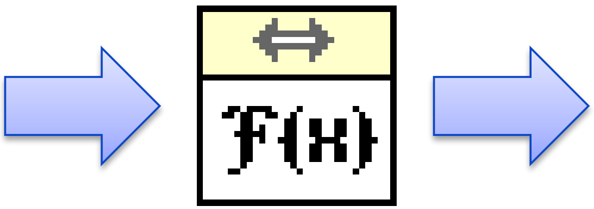
Optical Coherence Tomography Research

Early Cancer Detection with LabVIEW & PXI

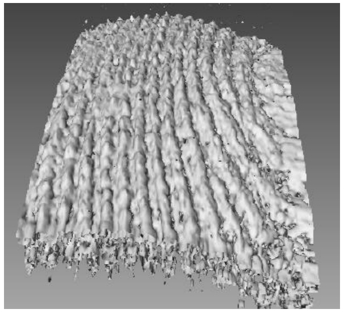
北里大学
KITASATO UNIVERSITY

K. Ohbayashi
Kitasato University,
Center for Fundamental Sciences





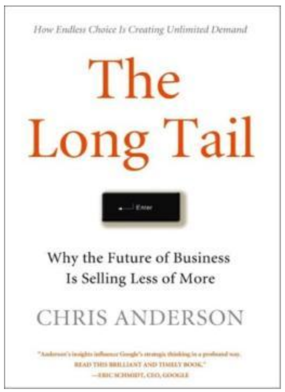
2D
FFT

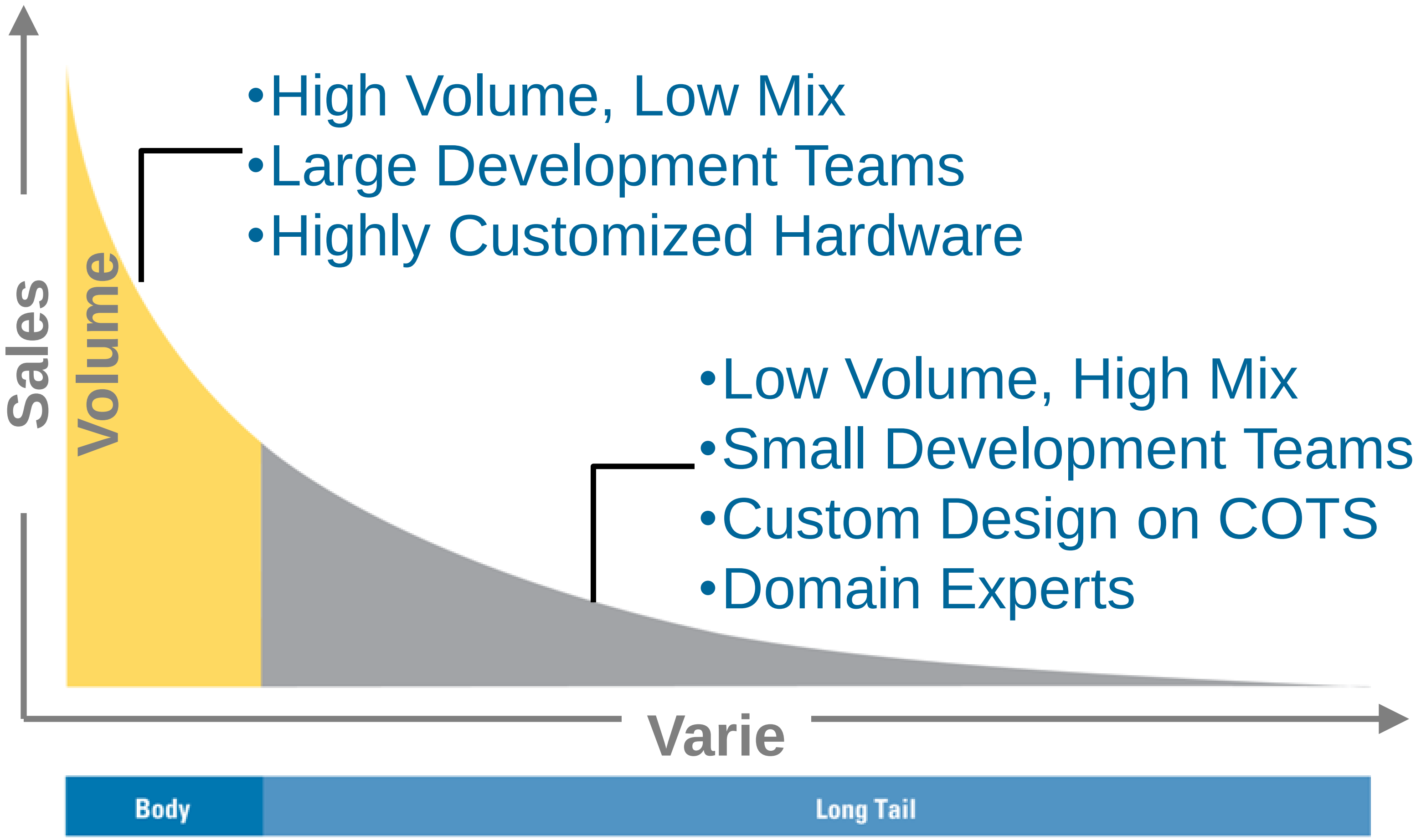


~ 1.5 M FFTs / sec for Real-Time Performance

Business Trends

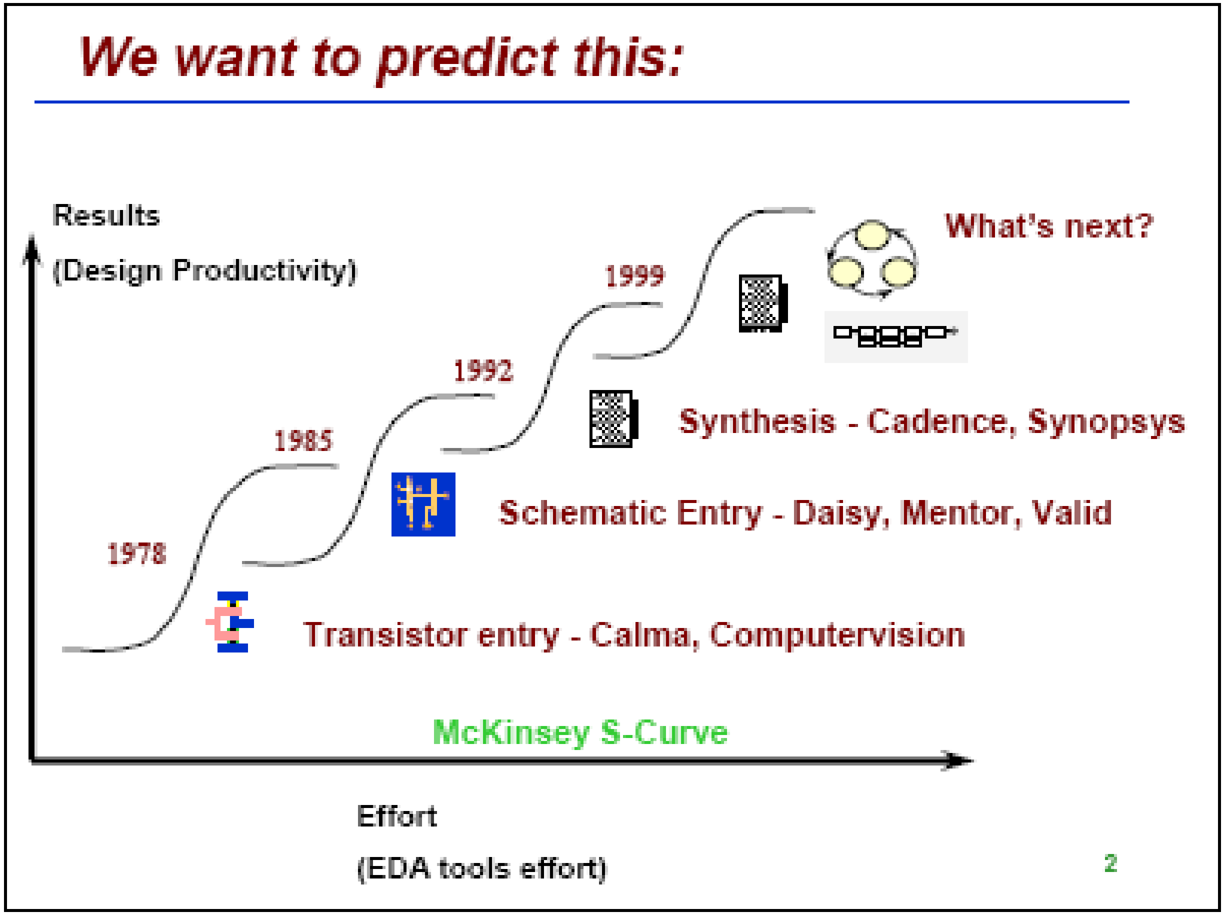
The Long Tail





["The Long Tail," Chris Anderson *Wired*, 2004]

Design discontinuities in EDA tools



[1] Kurt Keutzer, UC Berkeley EECS 244 class

Addressing Design Discontinuity

- New Methodology maps from the higher level abstraction down to the reliable foundation
  - A design-entry approach that offers **10X productivity** improvement.
  - A functional verification approach that offers **10-100X speed-up in verification**
  - An implementation approach that is **predictable and reliable**

[1] Matthias Gries, Kurt Keutzer. "Building ASIPs: The Mescal Methodology", Springer, 2005, 0-387-26057-9

National Instruments Vision *Evolved*

"To do for embedded what the PC did for the desktop."

Graphical System Design

Virtual Instrumentation

- Complex instrumentation
- RF
- Digital
- Distributed

Virtual Instrumentation and Embedded Systems

- Real-time measurements
- Embedded monitoring
- Hardware in the loop

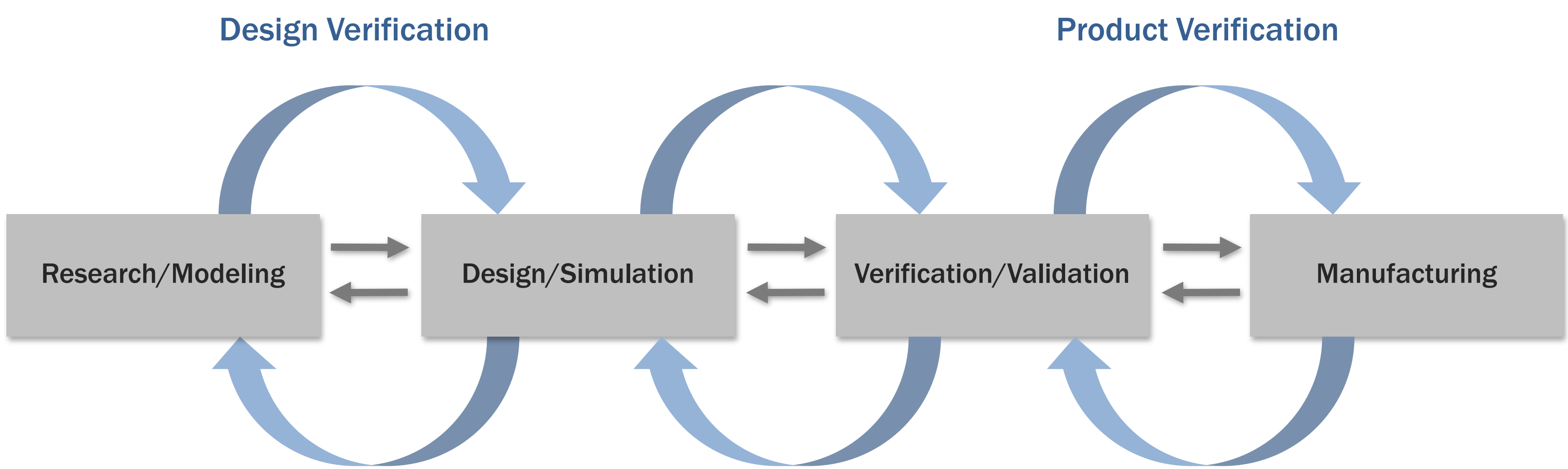
Embedded Systems

- Industrial control
- RT/FPGA systems
- Electronic devices
- C code generation

DESIGN ▷ **PROTOTYPE** ▷ **DEPLOY**

The Next 30 Years:
Expanding LabVIEW into System Design

NATIONAL INSTRUMENTS LabVIEW



Trends in Embedded Software

Alberto Sangiovanni-Vincentelli, UC Berkeley

"The *design of embedded systems is becoming more difficult* as design complexity increases, time-to-market pressures continue, and development teams with diverse backgrounds are assembled. The *platform-based design* methodology (PBD) is a technique to combat these challenges." [5]

"Given the cost and risks associated to developing hardware solutions, an increasing number of companies is selecting *hardware platforms that can be customized by reconfiguration and/or by software programmability*. In particular, *software is taking the lion's share of the implementation budgets and cost*. In cell phones, more than *1 million lines of code* is standard today, while in automobiles the estimated number of lines by 2010 is in the order of *hundreds of millions*." [6]

[5] A. Davare, et al. "A Next-Generation Design Framework for Platform-Based Design"
[6] Alberto Sangiovanni-Vincentelli, "Quo Vadis, SLD? Reasoning About the Trends and Challenges of System Level Design", Proceedings of the IEEE, Vol. 95, No. 3, March 2007.

Platform Based Design & Models of Computation

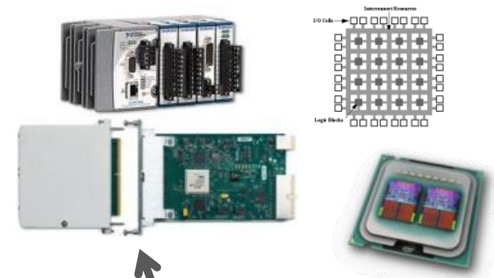
- Constructs for application domain experts
- Structured implementation with the right levels of abstraction
- Separation of concerns between functionality and architecture
- Evolve designs on hardware “generations”
- Design flow that supports analysis, simulation, verification and synthesis

[1] E.A. Lee, “Embedded Software”, Revised from UCB ERL Memorandum M01/26, November 1, 2001,
[2] E.A. Lee and S. Neuendorffer, “Concurrent Models of Computation for Embedded Software”, Memorandum No. UCB/ERL M04/26, July 22, 2004
[3] Alberto Sangiovanni-Vincentelli, "Quo Vadis, SLD? Reasoning About the Trends and Challenges of System Level Design", Proceedings of the IEEE, Vol. 95, No. 3, March 2007.

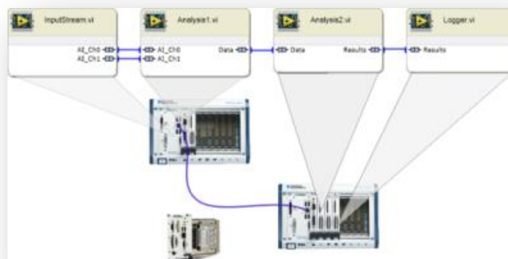
The Y-Chart System Design Methodology

Application Logic

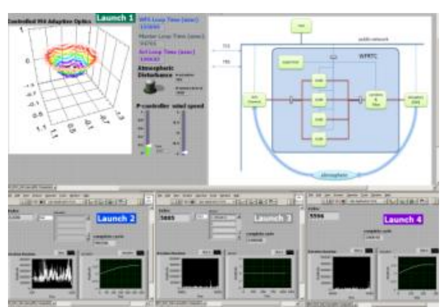
Platform Architecture



Analysis & Mapping



Performance Evaluation



1. Kienhuis, Deprettere, van der Wolf, and Vissers., "A Methodology to Design Programmable Embedded Systems - The Y-Chart Approach. Embedded Processor Design Challenges: Systems, Architectures, Modeling, and Simulation" - SAMOS, p.18-37, Jan. 2002.
2. Keutzer, Newton, Rabaey, Sangiovanni-Vincentelli, "System-level Design: Orthogonalization of Concerns and Platform-based Design," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 19(12): p. 1523-1543, Dec. 2000.

Platform Dimensions

- Distributed
- Heterogeneous computing platforms
  - Real-time OS, FPGA, Desktop OS, GPU
- Communication schemes
- Real-time
- IO
- Timing

Application Dimensions

- Algorithm development
- IO characterization
  - Timing characteristics
- Real-time constraints
- Integrating Models of Computation
- State management

Trends in Embedded Software

Edward Lee, UC Berkeley

"The principal role of embedded software is interaction with the physical world. Consequently, *the designer of that software should be the person who best understands that physical world."* [domain expert] [1]

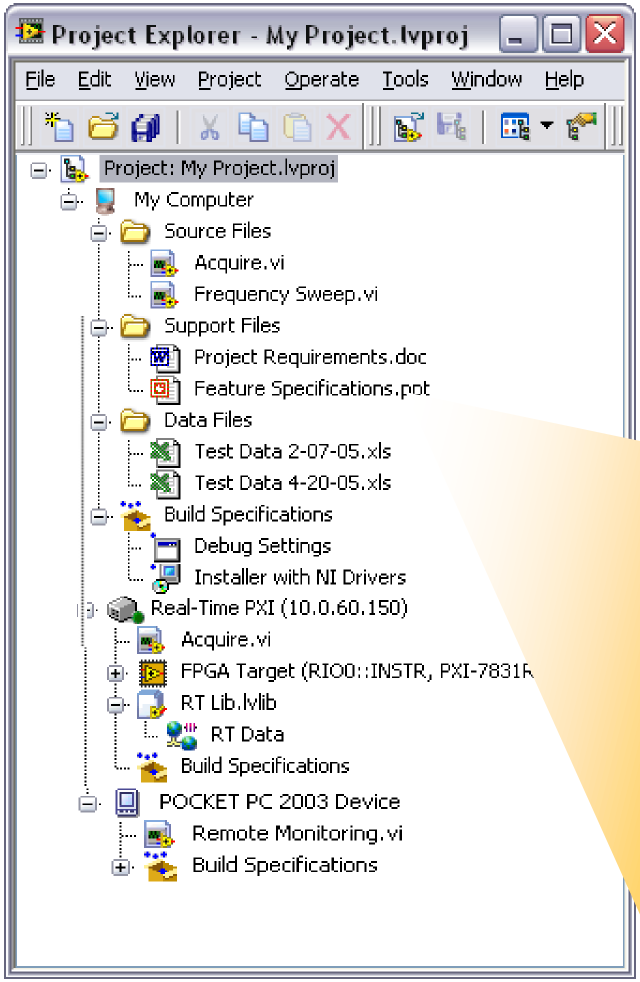
"The engineers that write embedded software are *rarely computer scientists.* They are *experts in the application domain* with a good understanding of the target architectures they work with." [1]

"Design of embedded software will require *models of computation* that *support concurrency.*" [1]

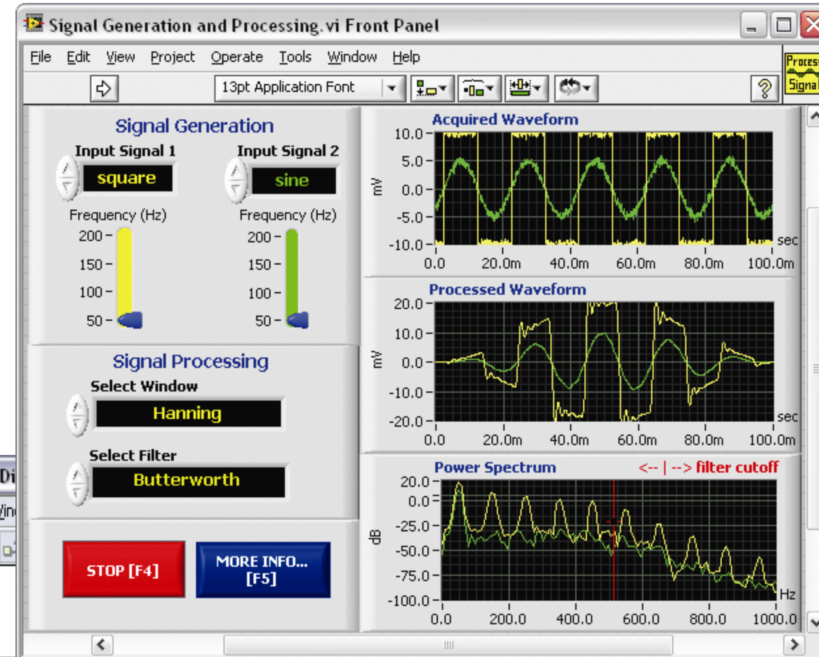
"In embedded software, *concurrency* and *time* are essential aspects of a design." [2]

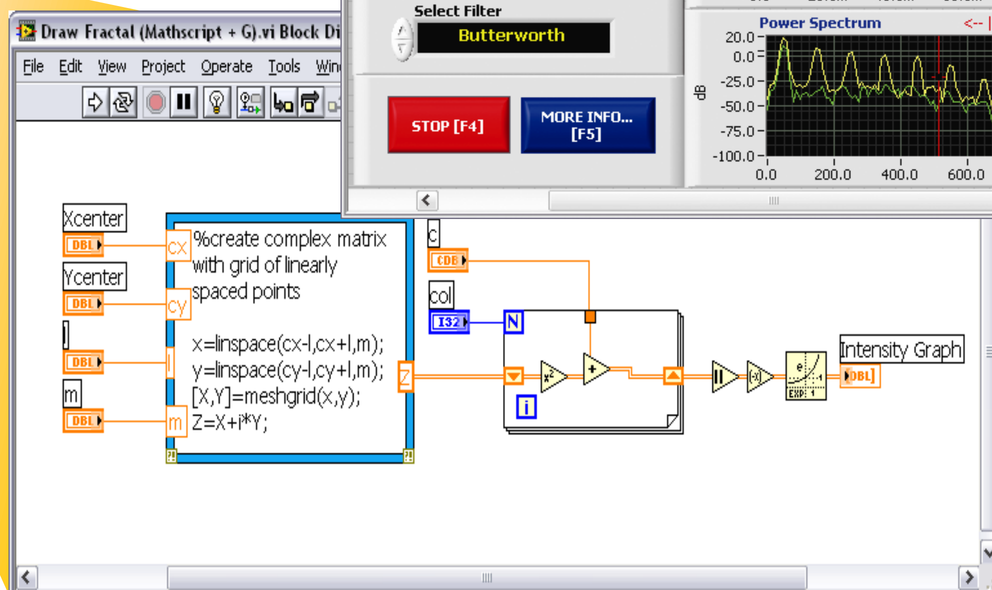
[1] E.A. Lee, "Embedded Software", Revised from UCB ERL Memorandum M01/26, November 1, 2001, (http://ptolemy.eecs.berkeley.edu/publications/papers/02/embsoft/embsoftwre.pdf)
[2] E.A. Lee and S. Neuendorffer, "Concurrent Models of Computation for Embedded Software", Memorandum No. UCB/ERL M04/26, July 22, 2004 (http://mesl.ucsd.edu/gupta/cse237b/Readings/concurrentmodels.pdf)

LabVIEW Today



Multiple Programming Models





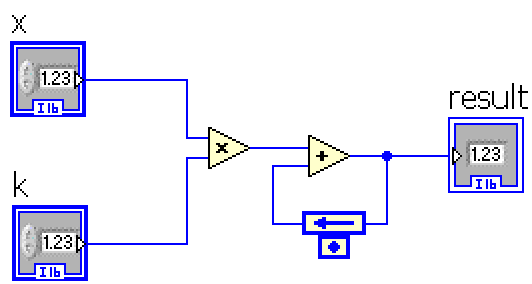
Distributed Computing

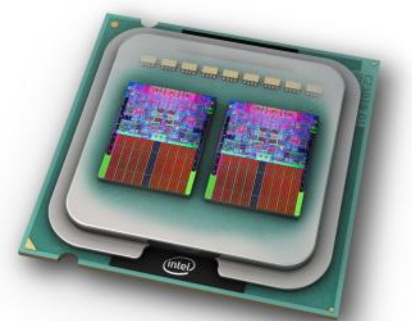
NATIONAL INSTRUMENTS

Models of Computation

Idea → **Model of Computation** → **Implementation**

Multiply / Accumulate



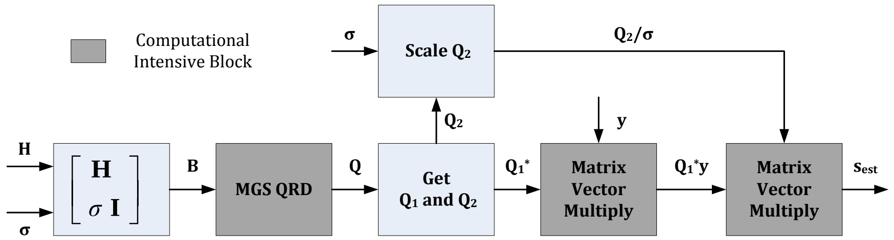


Design and Simulation

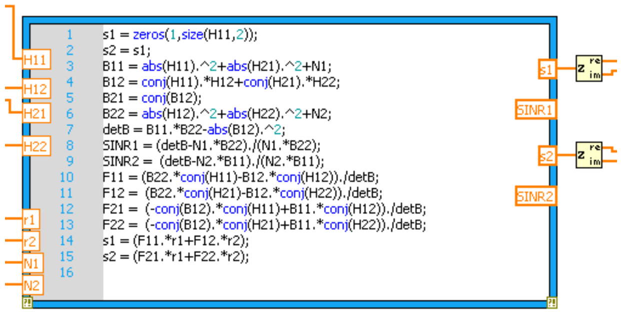
MMSE Equalizer (matrix inversion) problem:

$$\hat{\mathbf{x}} = \left(\hat{\mathbf{H}}^*\hat{\mathbf{H}} + \sigma^2\mathbf{I}\right)^{-1}\hat{\mathbf{H}}^*\mathbf{y}$$

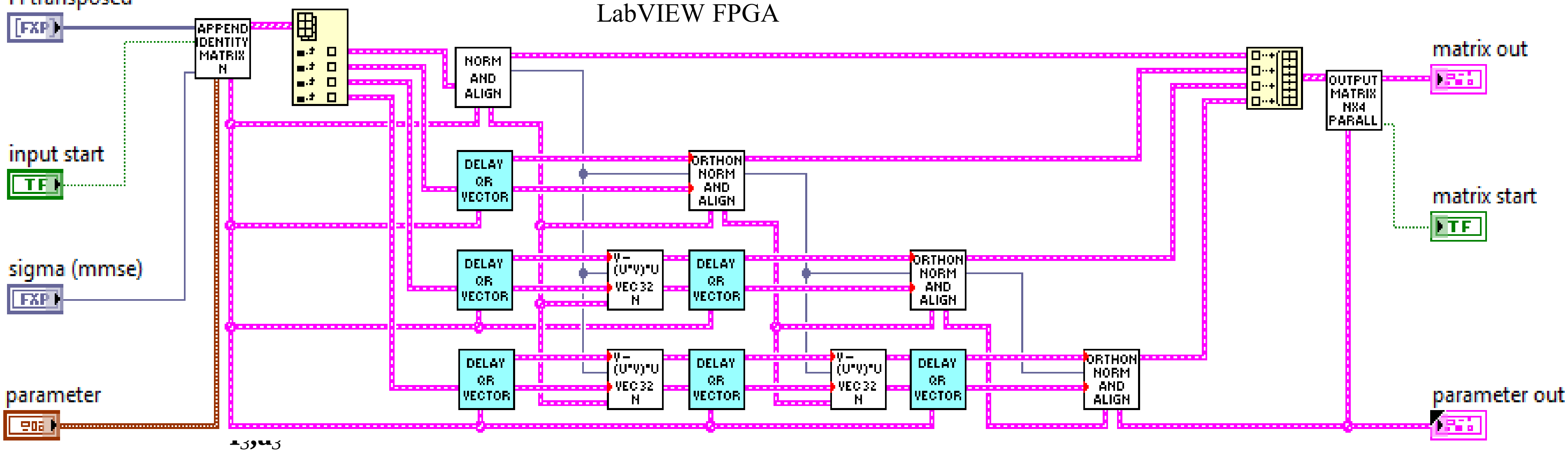
Conceptual Block Diagram



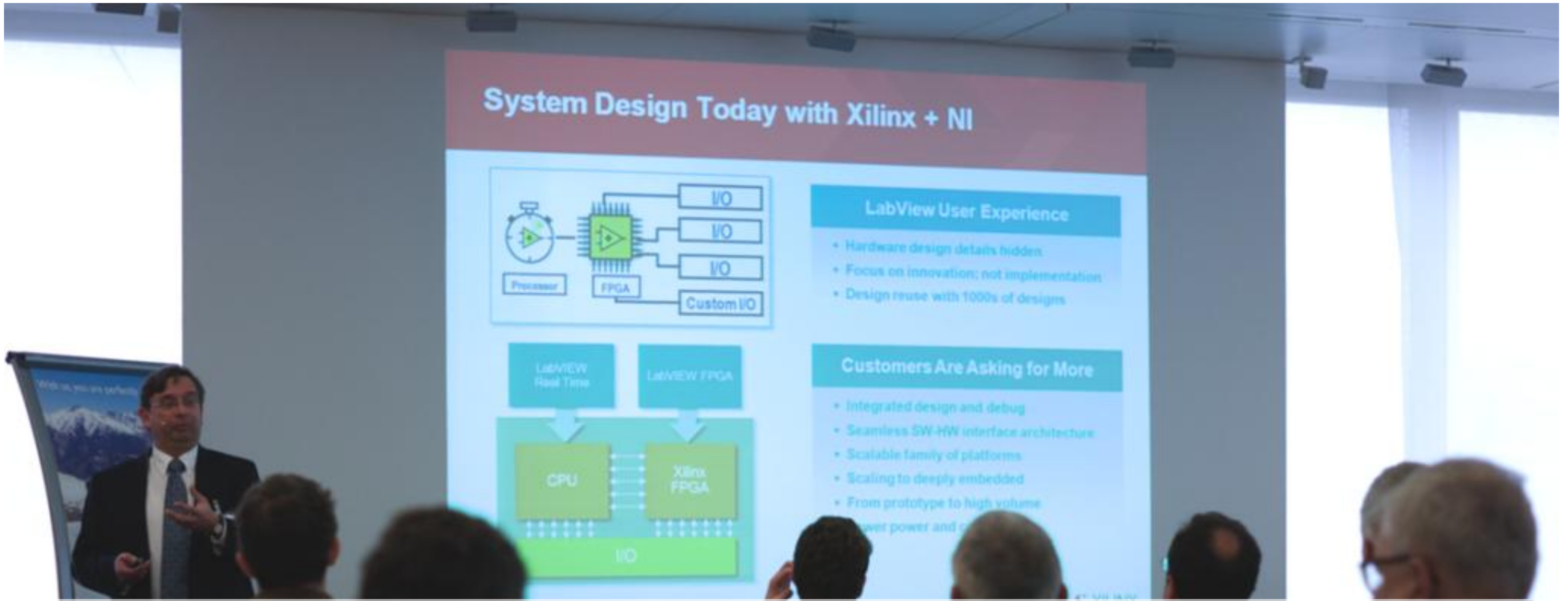
Textual Math



LabVIEW FPGA



Heterogeneous Architectures



"You need a high-level language to bring FPGA to the masses, people who are not essentially hardware programmers. We think LabVIEW is a very good tool that enables the domain experts to program FPGAs…"

– Ivo Bolsens, CTO, Xilinx

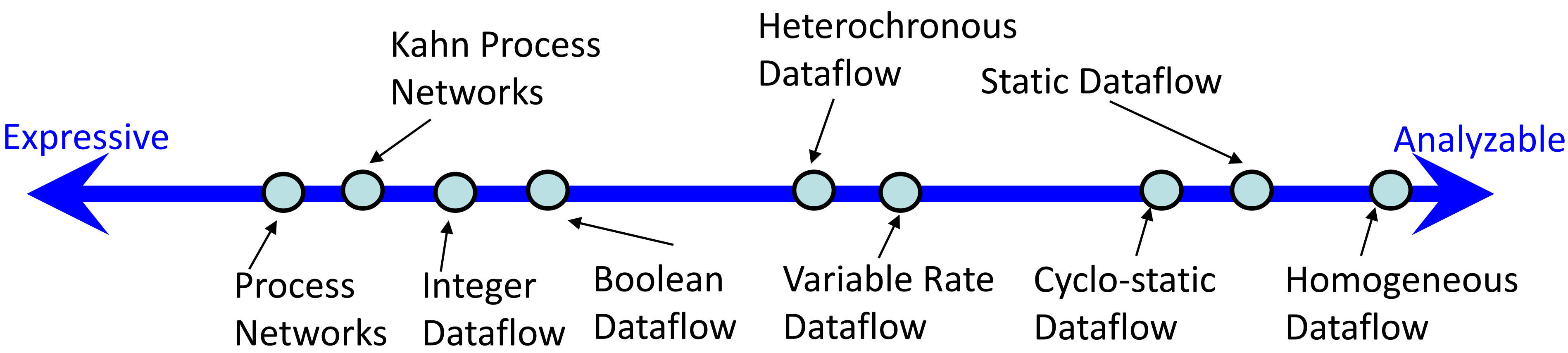
LabVIEW-Based System Design Tools

- Current project at National Instruments
  - Exploration of concepts and directions
- 2 arcs of exploration
  - System Design Tool
  - DSP algorithm development

Looking Closer at DSP Design

- Focus on DSP streaming applications running on FPGAs
- Explore the right Models of Computation (MoCs)
- Provide analysis and optimization
  - Throughput, latency, area
- Allow simulation and test bed creation
- Generate performing VHDL code
- Provide debugging capabilities

MoCs for Streaming Applications

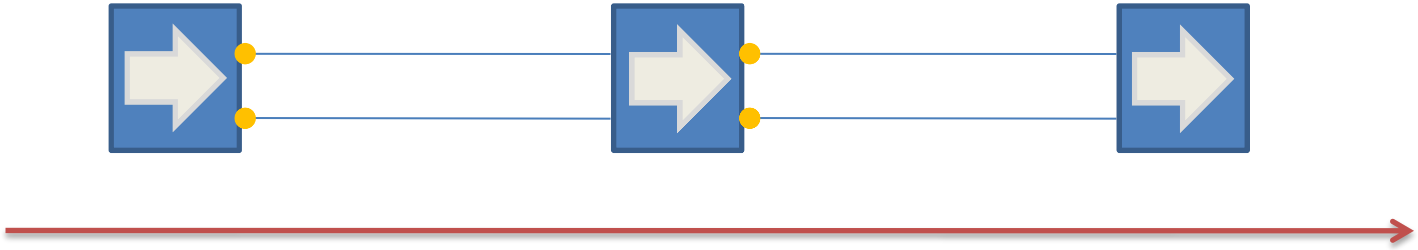


Deter-ministic?	No	Yes
Synchronous?	No	Yes
Deadlock and boundedness decidable?	No	Yes
Static scheduling?	No	Yes

Key trade-off: Analyzability vs. Expressibility

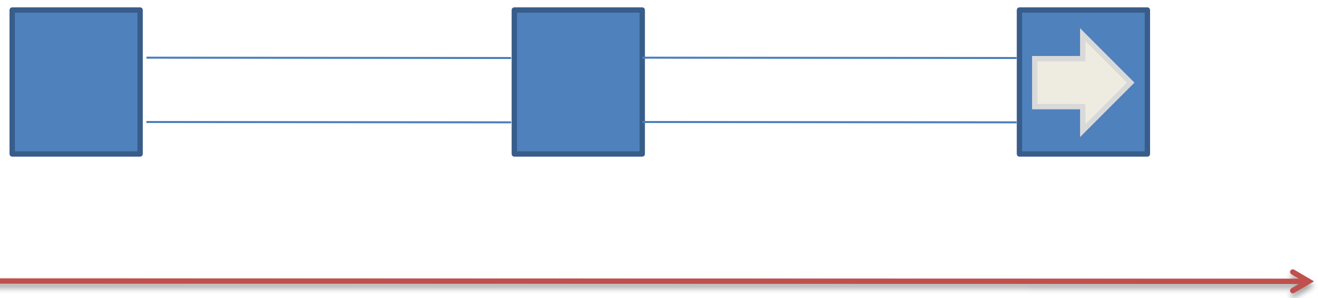
Dataflow Execution

- LabVIEW Dataflow



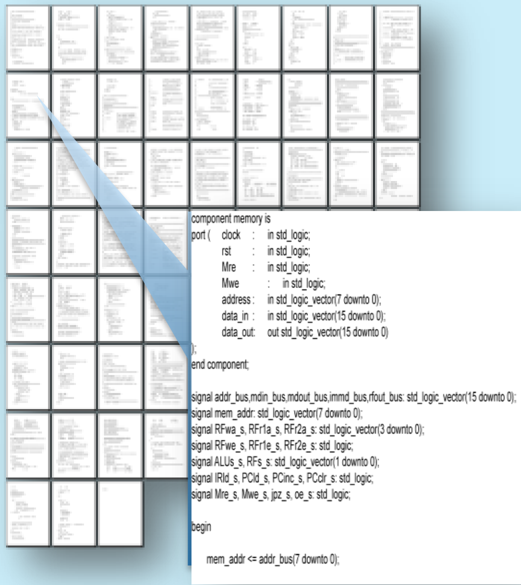
Multirate Execution

- LabVIEW Execution

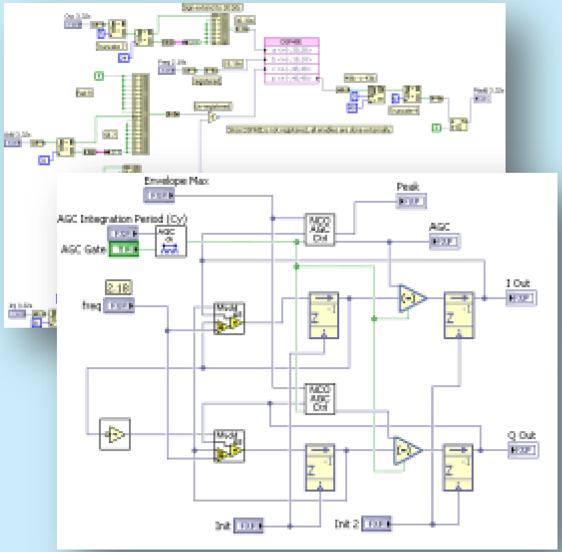


- Asynchronous Execution

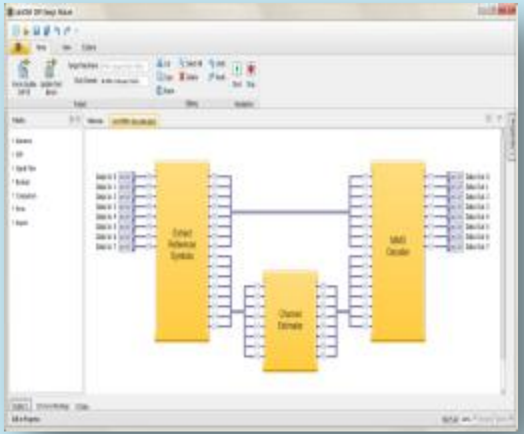
Platforms for FPGA-based System Design



HDL/RTL

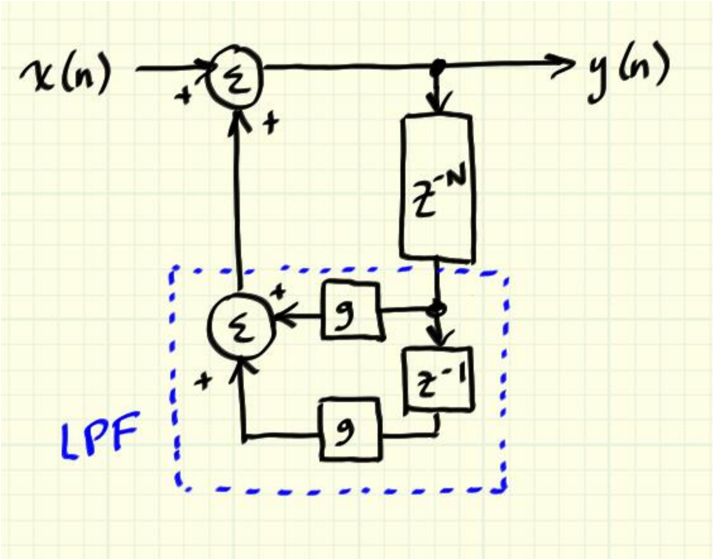


LabVIEW Today

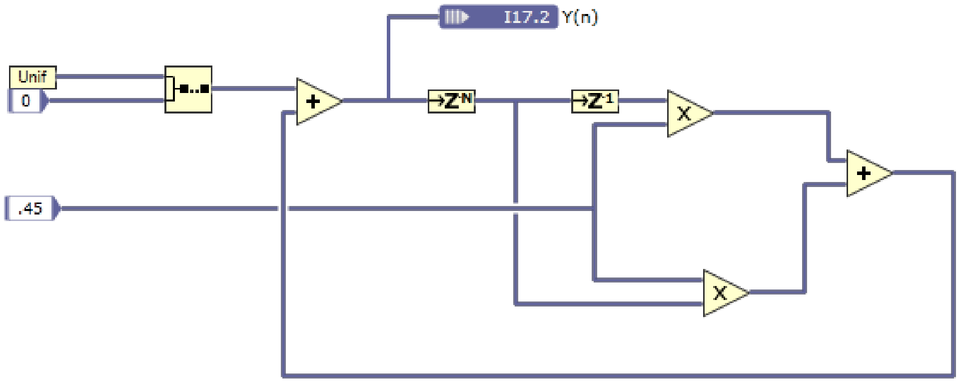


LabVIEW DSP
Design Module
Early Access Program

Making Applications Faster to Design

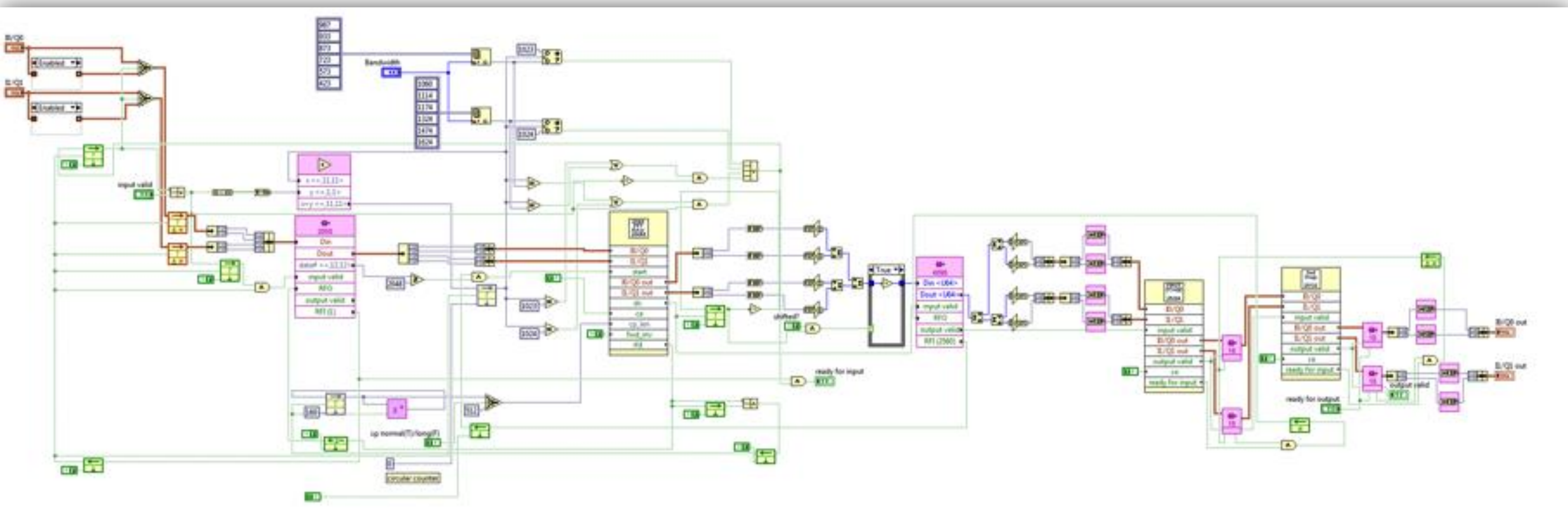


Karplus-Strong Plucked String Algorithm



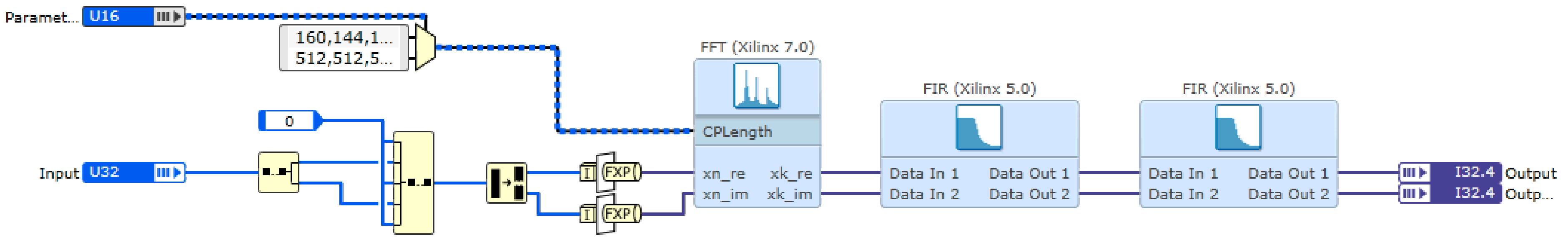
DSP Diagram

High-Speed Streaming is Complex Today



- Challenges
  - LabVIEW G model
    - Original specification from algorithm designer
    - Not feasible for highly efficient implementation on FPGA targets
  - Implementation challenges
    - Floating to fixed point conversion
    - Array data to point-by-point data conversion
    - Explicit concurrency representation
    - FPGA target constraints
    - Integration with internal and third-party IP

Domain Expert Expectations for High-Speed Streaming

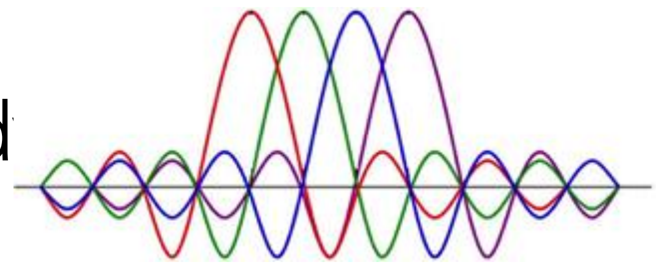


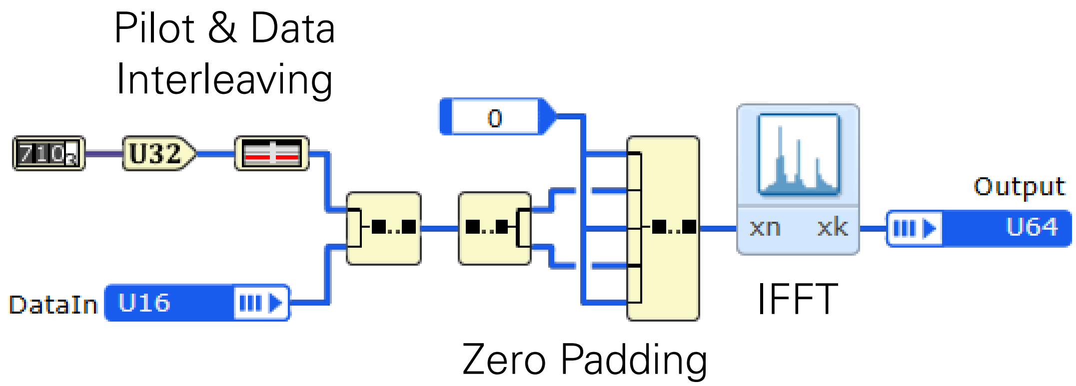
Parameterized Synchronous Dataflow

- High-level DSP representation that matches algorithm theory
  - Algorithms written independently of hardware target
  - Deal in domain terms of token rate, throughput, and latency
- Explore high-level design tradeoffs without diving into implementation details
  - Tune performance with high-level constraints
  - Access the details if needed

OFDM Transmitter

20 MHz LTE Transmission Band

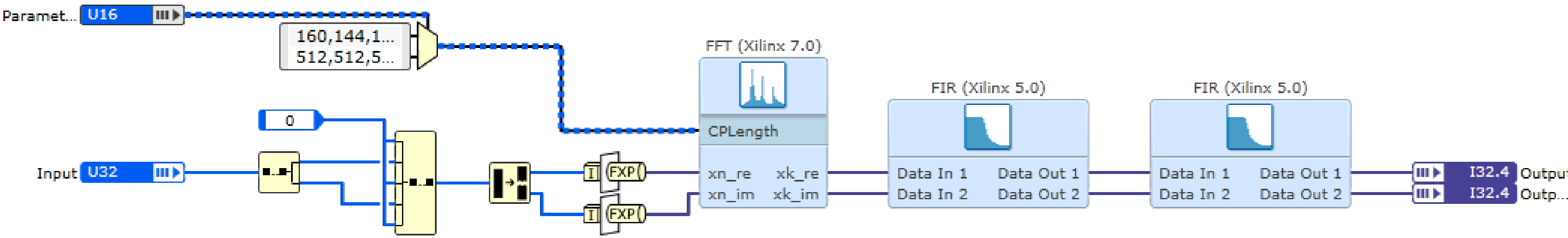




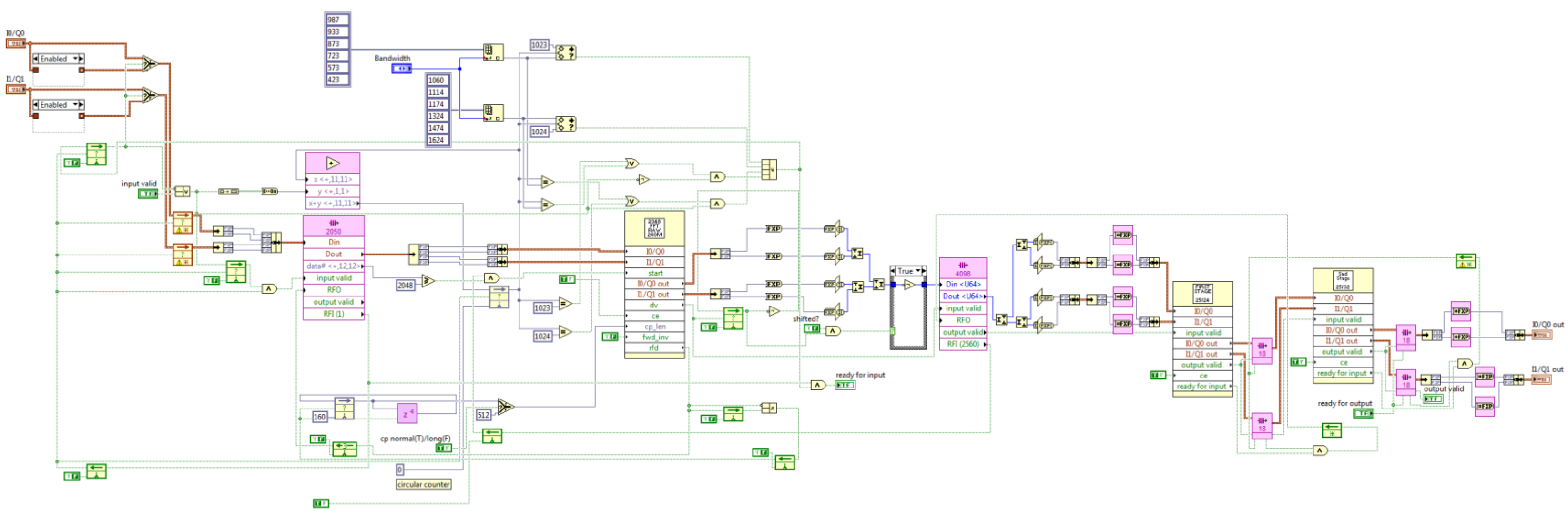
- Rapidly prototype PHY layer baseband DSP
- Co-design PHY layer algorithms with higher MAC layer protocols
- Seamless integration with wide array of RF hardware

DSP Design Module Value

Enable an algorithm designer to specify an intuitive diagram



that generates real-time DSP implementations on FPGAs



RF/Communications PHY FPGA Software

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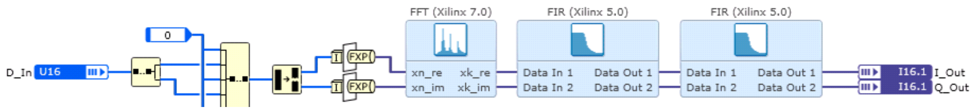
Graphical System Design Platform



LabVIEW DSP Diagram Module

LabVIEW FPGA	LabVIEW IP XILINX	LabVIEW FPGA IP Builder	3rd Party IP

RIO Hardware

Summary

- Complexity of system design
- New productivity tools
- System design
  - Design distributed systems
- DSP Design
  - Design DSP algorithms