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Citizenship: Germany

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Objective Research and development of networked, distributed and embedded computer systems with heterogeneous multi-processor and homogeneous multi-core system architectures. Investigation, implementation, and application of novel architectures, algorithms, tools, and methodologies for computer system design across hardware and software boundaries. Technical management, leadership and vision for deployment and growth of new technologies.

Education

4/2004	University of California, Irvine Ph.D., Information and Computer Science , GPA: 4.0 / 4.0 Thesis title: <i>Modeling Flow for Automated System Design and Exploration</i> Advisor: Prof. Daniel D. Gajski	Irvine, CA
9/1998	University of California, Irvine M.S., Information and Computer Science , GPA: 3.97 / 4.0	Irvine, CA
5/1997	University of Stuttgart Diplom-Ingenieur (M.S.), Electrical Engineering , <i>summa cum laude</i> Thesis title: <i>Development of a Standard Cell Library in CMOS and Pass Transistor Logic for Low Power Applications</i>	Stuttgart Germany
10/1991	University of Stuttgart Vordiplom (B.S.), Electrical Engineering , <i>cum laude</i>	Stuttgart Germany

Experience

8/2008-now	Electrical and Computer Engineering Assistant Professor <ul style="list-style-type: none">▪ Researched electronic-system level (ESL) modeling and synthesis concepts and techniques▪ Researched custom SoC computing platforms for stochastic simulation of biological networks, probabilistic computing techniques for ultra low-power circuit operation, and acceleration of stochastic control algorithms for cyber-enabled manufacturing in collaborations with professors in ECE and CS.	University of Texas, Austin, TX
6/2004-8/2008	Center for Embedded Computer Systems Assistant Researcher <ul style="list-style-type: none">▪ Researched and developed electronic system-level (ESL) design automation (EDA) tools and concepts for C/C++ based synthesis, optimization, partitioning and design of heterogeneous multi-processor and multi-core system platforms and SoC/NoC communication architectures.▪ Successfully transferred and commercialized Specify-Explore-Refine (SCE/SER) technology for adoption by the Japanese Aerospace Exploration Agency (JAXA), JAXA suppliers like NEC Toshiba Space Systems and general market availability. SER is licensed and sold commercially by InterDesign Technologies, Inc.▪ Managed, led and supervised R&D projects including product planning, specification, development and quality assurance in team of 5-10 scientists, developers and engineers.▪ Interfaced with clients in Japan on requirements and deliverables. Managed project schedule and resources to successfully meet milestones and deadlines.▪ Drove implementation of several complex MPSoC design examples for space and satellite applications (using MIPS-compatible Toshiba CPUs and busses, PCI and FPGAs), cellular phone platforms (ARM/AMBA, Motorola DSP) and multimedia processing (on Xilinx/OPB).	University of California Irvine, CA

- 1998-3/2004 Center for Embedded Computer Systems University of California
Irvine, CA
Graduate Research Assistant
- Architected and developed (in C++ and Python) a complete, automated SoC Design Environment (SCE) for synthesis of abstract system specifications down to optimized hardware/software (RTL/ISS) implementations.
 - Researched system-level design models and the SpecC system design methodology in contracts with the Semiconductor Research Cooperation (SRC) and industry sponsors.
 - Co-supervised and led research and development team of 5-10 students, visiting researchers and developers.
 - In contracts with Motorola, Inc. and Conexant, Inc., implemented several embedded system designs and system-on-chip (SoC) applications for audio (MP3), video (JPEG, JBIG) and mobile baseband (GSM) processing in a combination of hardware and software.
- 1996-1997 Integrated Systems Engineering, Computer Science University of Stuttgart
Stuttgart, Germany
Graduate Research Assistant
- Investigated different logic families for use with a new semiconductor technology (three-dimensional silicon-on-insulator (SOI) process).
 - Developed a standard cell library in Double Pass-Transistor Logic (DPL) and standard static CMOS logic.
 - Implemented and simulated several gate/transistor-level designs in all logic families.
- 1995-1996 Institute for Microelectronics Stuttgart University of Stuttgart
Stuttgart, Germany
Research Assistant
- Developed a RISC micro-controller core in VHDL.
 - Automated synthesis of the RTL description into a gate-level netlist using CAD tools.
 - Simulation and verification of the design at different levels.
- 1993-1994 Institute of Comm. Networks and Computer Engineering University of Stuttgart
Stuttgart, Germany
Research Assistant
- Simulation of different permit distribution protocols for a permit-based fiber-to-the-home (FTTH) ATM access network with tree topology.
 - Queuing theory based statistical analysis for different traffic scenarios.
- 1989-1997 Ehrler Prüftechnik Steinenbronn
Germany
Senior Software Engineer and Project Manager
- Developed and designed real-time multitasking software for process control, data acquisition, analysis and automation in complex industrial test benches for automotive applications.
 - Managed and led software projects with teams of 2-5 people. Coordinated software design, development and testing with internal electrical and mechanical design teams.
 - Documented and negotiated software requirements specifications with various clients. Developed specification contracts and product documentation.
 - Supervised, coordinated and performed deployment, installation and maintenance of testbench software at client sites in Europe and USA.
 - Supervised and trained new software team members.
- 1994 Böblingen Instruments Division (BID) Hewlett-Packard GmbH
Böblingen, Germany
Summer Intern
- Designed and implemented a C++ sub-process for printing in an optical time-domain reflectometer (OTDR) measurement instrument.

Teaching

- 2008-now Electrical and Computer Engineering University of Texas,
Austin, TX
Assistant Professor
- Developed graduate class on embedded system design & modeling (E382V, F'08)
- 2005-2008 Electrical Engineering and Computer Science University of California
Irvine, CA
Lecturer
- Instructor on record for undergraduate class in digital system design (EECS/CSE 31, F'07).
 - Substitute lecturer for undergraduate classes in digital logic/system design (EECS/CSE 31).
 - Substitute lecturer for graduate class on SoC design and exploration (EECS 221).

1997-2002	Information and Computer Science Teaching Assistant	University of California Irvine, CA
	<ul style="list-style-type: none"> ▪ Advanced graduate seminar in system design (ICS 259, W'02). ▪ Senior undergraduate computer design laboratory (ICS 155B, S'98). ▪ Senior undergraduate logic design laboratory class (ICS 155A, W'98). ▪ Senior undergraduate class in computer networks (ICS 153, F'97). 	

Honors and Awards

1998, 2002	Professional Development Award, Young Student Mentor	Design Automation Conference
2000-2001	Motorola Research Fellow	Motorola, Inc.
1998	Advanced Study Institute Grant	NATO ASI
1997	Graduated <i>summa cum laude</i> (“mit Auszeichnung”)	University of Stuttgart, Germany

Professional Service

Volunteer Activities	<ul style="list-style-type: none"> ▪ Organized invited talks at the Center for Embedded Computer Systems (CECS). ▪ Organized CECS booth at Design Automation Conference exhibition. ▪ Co-organizer of the UT Austin VLSI seminar series.
Conference Organization	<ul style="list-style-type: none"> ▪ Local Arrangements Chair: IESS '07 ▪ Special session organizer: ASPDAC '09 ▪ Technical Program Committee: DATE '06-'09, IESS '07, DTIS '08, CODES+ISSS '09, CASES'09 ▪ Session chair: DATE '06, IESS '07, DATE '09
Reviews	<ul style="list-style-type: none"> ▪ Conferences: DAC, DATE, ICCAD, ISSS+CODES, ASPDAC, SASIMI ▪ Journals: IEEE D&T Magazine, IEEE TVLSI, IEEE TCAD, JCSC, JES, DAES
Memberships	<ul style="list-style-type: none"> ▪ IEEE (since 1997): Circuits & Systems Society, Computer Society ▪ ACM (since 1997): Special Interest Group on Design Automation (SIGDA)

Tutorials and Presentations

Conference Tutorials	<ul style="list-style-type: none"> ▪ “Modeling, Synthesis and Verification,” in <i>System-Level Modeling, Analysis and Synthesis of Embedded Multi-core Designs</i>, Design, Automation & Test in Europe (DATE), April 2009 ▪ “Embedded System Modeling,” in <i>Concepts and Tools for Practical Embedded System Design</i>, Asia and South Pacific Design Automation Conference (ASPDAC), January 2007. ▪ “System-Level Modeling and Design: Experimentation with SpecC,” in <i>System Level Specification beyond RTL</i>, Design, Automation & Test in Europe (DATE), March 2002. ▪ “Modeling and Design with SpecC” and “Design of a GSM Vocoder,” in <i>SpecC Language and Design Methodology</i>, Design, Automation & Test in Europe Conference (DATE), March 2001.
Industry Consulting	<ul style="list-style-type: none"> ▪ “Principles of Embedded Systems: Modeling, Synthesis and Verification,” in <i>High-Level Design</i>, VLSI Design Education Center (VDEC), Tokyo, Japan, January 2008. ▪ “Modeling and Design with SpecC” and “Design of a GSM Vocoder,” in <i>SpecC Language and Design Methodology</i>, Motorola Semiconductor Products Section, Austin, April 2001.
Invited Talks	<ul style="list-style-type: none"> ▪ “Electronic System Level Modeling for Automated MPSoC Design and Exploration,” National Instruments, IBM Austin Research Labs, and Freescale, November/December 2008. ▪ “Programming, Modeling and Synthesis of Multi-Processor System Software,” UC Santa Barbara, March 2008. ▪ “Embedded Processor and RTOS Modeling for MPSoC Design and Validation,” Infineon Technologies AG, University of Stuttgart, Munich University of Technology, University of Paderborn, Germany, and University of Tokyo, Japan, June/August 2007. ▪ “A System Design Environment for Automatic Model Generation and Prototyping,” Robert Bosch GmbH, Germany, March 2006. ▪ “Layer-Based Communication Design for Automatic SoC Platform Generation”, University of Tübingen, Germany, October 2005. ▪ “Methodology and Environment for System-Level Design”, Xilinx, San Jose, August 2003. ▪ “System-Level Design Language, Methodology and Environment”, IBM Research and BMW Research and Development, Germany, January/March 2003. ▪ “Modeling and Design with SpecC”, C-LAB, University of Paderborn, Germany, March 2001.

Selected Publications

- Books**
- A. Rettberg, M. Zanella, R. Dömer, A. Gerstlauer, F. Rammig (editors), *Embedded System Design: Topics, Techniques and Trends*, Springer Science+Business Media, June 2007.
 - A. Gerstlauer, R. Dömer, J. Peng, D. Gajski, *System Design: A Practical Guide with SpecC*, Kluwer Academic Publishers, 2001.
 - D. D. Gajski, J. Zhu, R. Dömer, A. Gerstlauer, S. Zhao, *SpecC: Specification Language and Methodology*, Kluwer Academic Publishers, 2000.
- Book Chapters**
- G. Schirner, R. Dömer, A. Gerstlauer, “High-Level Development, Modeling and Automatic Generation of Hardware-Dependent Software,” in W. Ecker, W. Mueller, R. Doemer (eds.), *Hardware-Dependent Software: Principles and Practice*, Springer, to appear 2009
 - A. Gerstlauer, H. Yu, D. Gajski, “RTOS Modeling for System-Level Design,” in R. Lauwereins, J. Madsen (Eds.), *Design, Automation, and Test in Europe: The Most Influential Papers of 10 Years DATE*, Springer, 2008, and A. A. Jerraya, S. Yoo, N. Wehn, D. Verkest (Eds.), *Embedded Software for SoC*, Kluwer, 2003.
- Journal Papers**
- R. Dömer, A. Gerstlauer, J. Peng, D. Shin, L. Cai, H. Yu, S. Abdi, D. Gajski, “System-on-Chip Environment: A SpecC-based Framework for Heterogeneous MPSoC Design,” *EURASIP Journal on Embedded Systems (JES)*, vol. 2008, Article ID 647953, 13 pages, 2008
 - D. Shin, A. Gerstlauer, R. Dömer, D. D. Gajski, “An Interactive Design Environment for C-based High-level Synthesis of RTL Processors,” *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 16, no. 4, pp. 466-475, April 2008.
 - A. Gerstlauer, D. Shin, J. Peng, R. Dömer, D. D. Gajski, “Automatic, Layer-based Generation of System-On-Chip Bus Communication Models,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 26, no. 9, pp. 1676-1687, September 2007.
- Conference Papers**
- A. Gerstlauer, J. Peng, D. Shin, D. Gajski, A. Nakamura, D. Araki, Y. Nishihara, “Specify-Explore-Refine (SER): From Specification to Implementation,” *Design Automation Conference (DAC)*, Anaheim, CA, June 2008.
 - G. Schirner, A. Gerstlauer, R. Dömer, “Abstract, Multifaceted Modeling of Embedded Processors for System Level Design,” *Asia and South Pacific Design Automation Conference (ASPDAC)*, January 2007.
 - L. Cai, A. Gerstlauer, D. Gajski, “Retargetable Profiling for Rapid, Early System-Level Design Space Exploration,” *Design Automation Conference (DAC)*, June 2004.
 - A. Gerstlauer and D. Gajski, “System-Level Abstraction Semantics,” *International Symposium on System Synthesis (ISSS)*, October 2002.
 - W. Mueller, R. Dömer, A. Gerstlauer, “The Formal Execution Semantics of SpecC,” *International Symposium on System Synthesis (ISSS)*, October 2002.
- Professional Documents**
- R. Dömer, A. Gerstlauer, D. Gajski, “SpecC Language Reference Manual, Version 2.0,” SpecC Technology Open Consortium (STOC), December 2002.
 - R. Dömer, A. Gerstlauer, D. Gajski, “SpecC Language Reference Manual, Version 1.0,” SpecC Technology Open Consortium (STOC), March 2001.

For a complete list of publications, please visit: <http://www.ece.utexas.edu/~gerstl/research.html>

Skills

- Languages**
- German (native), English (fluent), French (read)
- Computing**
- Programming languages: Python, C/C++, Perl, Java, assembly (x86/DSP), shells (tsh, bash).
 - System administration: Unix (Solaris, Linux), Windows (98, NT, 2000, XP).
 - Web programming: HTML, Javascript, XML.
- EDA/CAD**
- Languages: VHDL, SystemC, SpecC.
 - Tools: Synopsys (DC, VSS), Cadence, SPICE/HSPICE, Compass.