

KARTHIK GANESAN

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OBJECTIVE

Seeking for an internship in computer architecture specializing in performance evaluation for Summer 2010.

ACADEMIC HIGHLIGHTS

Graduate Level:

Master of Science in **computer engineering**, ECE Department with a **GPA of 3.91 at UT Austin** (Fall' 06 – Fall'08) and continuing with a **Doctorate**.

Relevant Courses:

Computer Architecture, Computer Performance Evaluation and Benchmarking, Superscalar Microprocessors, Distributed Systems, Advance Compiler Techniques, Statistics for Engineers, Data mining and Collaborative software design, Principles of Computer Architecture, Computer Architecture – User System Interplay.

Undergraduate Level:

Bachelor of Engineering (**Computer Science & Engg**), Anna University, Chennai, India (2002-2006). **FIRST CLASS** with **DISTINCTION** with an aggregate of **84%**. Courses like Computer architecture I & II, Interactive Computer Graphics, Parallel computer architecture, Operating Systems, Programming and Data Structures, Compilers, DBMS & System software, Object Oriented Programming & Software Engineering were taken.

Teaching:

Teaching Assistant to the lab course **“Digital design using VHDL”** involving the VHDL coding and FPGA Implementation using Modelsim and Xilinx for Fall '06, Spring '07, Fall '08. Teaching Assistant to **“Superscalar Microprocessor Architectures (ECD)”** course for fall '07.

RESEARCH HIGHLIGHTS

Areas of Interests:

- Multi-core architectures and parallel computing
- Performance evaluation, benchmarking & workload characterization
- Application scheduling & operating system

Research Experience:

Research Intern at IBM T. J. Watson Labs, worked with the BlueGene Team - Summer 2007. Was involved in designing an interface library to access the performance counters of the Next Generation BlueGene/P and published the work in ICPP 2008.

Intern at IBM Austin, worked with the open source Performance Inspector tool – Summer 2008. Was involved in improving the performance of ltrace on the power architecture. Implemented a patented solution for solving the buffer overflow problem by dynamically slowing down the application based on the buffer occupancy.

Undergraduate level part time research trainee at WAran Research FoundaTion (WARFT) from May 2004 –Jul 2006. Was working in the High Performance Architecture Group "VISWAKARMA" in designing a Novel Memory In Processor Architecture.

Undergraduate WARF I Research Thesis:

Thesis titled "**Hierarchical Multihost based Operating System for Simultaneous Multiple Application Execution on Memory In Processor Super Computer On Chip Cluster**" focuses on a novel cluster operating system design for the MIP SCOC cluster.

Select Papers:

- Jungho Jo, Karthik Ganesan, Lizy K John, "Miniaturized Synthetic Benchmarks for SPEC CPU2006 and Implant Bench Suites" in TECHCON 2009, Austin, Texas
 - .Karthik Ganesan. et al "**A Performance Counter Based Workload Characterization on Blue Gene/P** " selected for presentation at the 37th International conference, ICPP 2008 at Portland, Oregon.
 - .Valentina Salapura, Karthik Ganesan, et al "**A Next-Generation Performance Counters: Towards Monitoring Over Thousand Concurrent Events**", presented at 2008 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2008) on 22nd April 2008.
 - Venkateswaran Nagarajan, Karthik Ganesan et al "**Future Generation Supercomputers II: A Paradigm for Cluster Architecture**" published in the Journal ACM SIGARCH Computer Architecture News, Vol. 35, No. 5, December 2007.
 - Venkateswaran Nagarajan, Karthik Ganesan et al "**On the Concepts of Simultaneous Execution of Multiple Applications on the Hierarchically based Cluster and the Silicon Operating System**" selected for presentation at the workshop on Large-Scale Parallel Processing to be held at the 22nd IEEE International Parallel and Distributed Processing Symposium, IPDPS 2008, Miami, in Apr '08.
 - N.Venkateswaran, Karthik.G et al "**High Performance Low Power Single Chip Reconfigurable Supercomputer for High-end Aerospace Applications**" Selected for presentation at the 8th International MAPLD 05 Conference conducted by NASA on Sep 7, 2005. The above given paper was also presented in the **Birds Of Feather Workshop** on Sep 8, 2005 in MAPLD 2005.
 - N.Venkateswaran, Karthik.G et al "Simulation Model for predicting The Multi-Million Neuron Interconnectivity and Evolution of a **Neurophysiologically Inspired Supercomputing Architecture** for Modeling the Respective Brain Regions" Presented at Max Planck Institute of Medical Research Workshop, "Data driven Modeling and Computational Neuroscience" DMCN 2005, Heidelberg, Germany, conducted by Prof Bert Sakmann, Nobel Laureate 1991, *Springer Verlag*.
 - N.Venkateswaran, Karthik.G et al "**Memory and Power Efficient Application Execution In MIP SCOC**" presented Dhi' Yantra 06, the WARFT Workshop on Brain Modeling and Supercomputing, Chennai, India. March, 2006.
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Undergraduate Project:

The final year project titled "**Emulating IBM BlueGene On Linux Mpi Cluster**" won the **BEST PROJECT AWARD** of the CS department of SVCE. The project concentrates on modeling the performance of a 500 node IBM BlueGene cluster by using benchmark applications.

TECHNICAL PROFICIENCY

Programming Languages/Knowledge

• JAVA • C • C++ • PHP • Oracle/SQL • VB 6.0/VB Script

Processor/System Architecture

Alpha/PowerPC embedded assembly • Intel 8085 • Basic to advance user skills in Linux • CUDA GPU programming • Cell Processor programming • Sequoia (parallel programming)

Hardware Description Languages

• VHDL • Verilog

Performance Evaluation & Benchmarking Tools

• PIN • SimpleScalar • HLS • Simics • SPEC CPU 2000/2006 suites • Mibench • ImplantBench

Text Processing & Statistics Tools

• LATEX • MiKTeX • WinEdt • Microsoft Office • JMP

Graphics and Image Processing Tools

• Xfig • SmartDraw • Adobe Photoshop • Sigmaplot

Web Languages

• HTML • JavaScript • DHTML • PHP • XML

Software Tools Developed/Worked on

- Performance Inspector – <http://perfinsp.sourceforge.net/>
- Synthetic Benchmark Generator – synthetic benchmark generation framework for performance analysis