EE 394 V Multiple-input dc-dc converters

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Power Electronics as Efficient Interface in Dispersed Power Generation Systems

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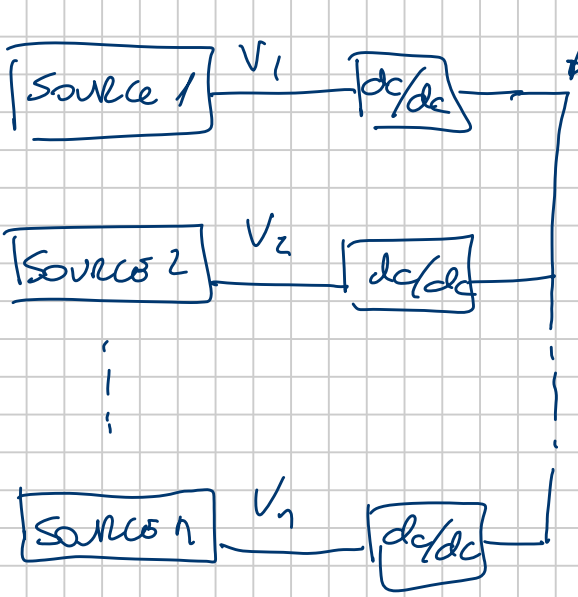
Nice paper but doesn't include multiple-input converters (MICs)
→ More about this later

What are MICs?

To answer the question let's see what is the purpose of MICs

There are several ways to connect multiple dc sources to a common bus:

1)

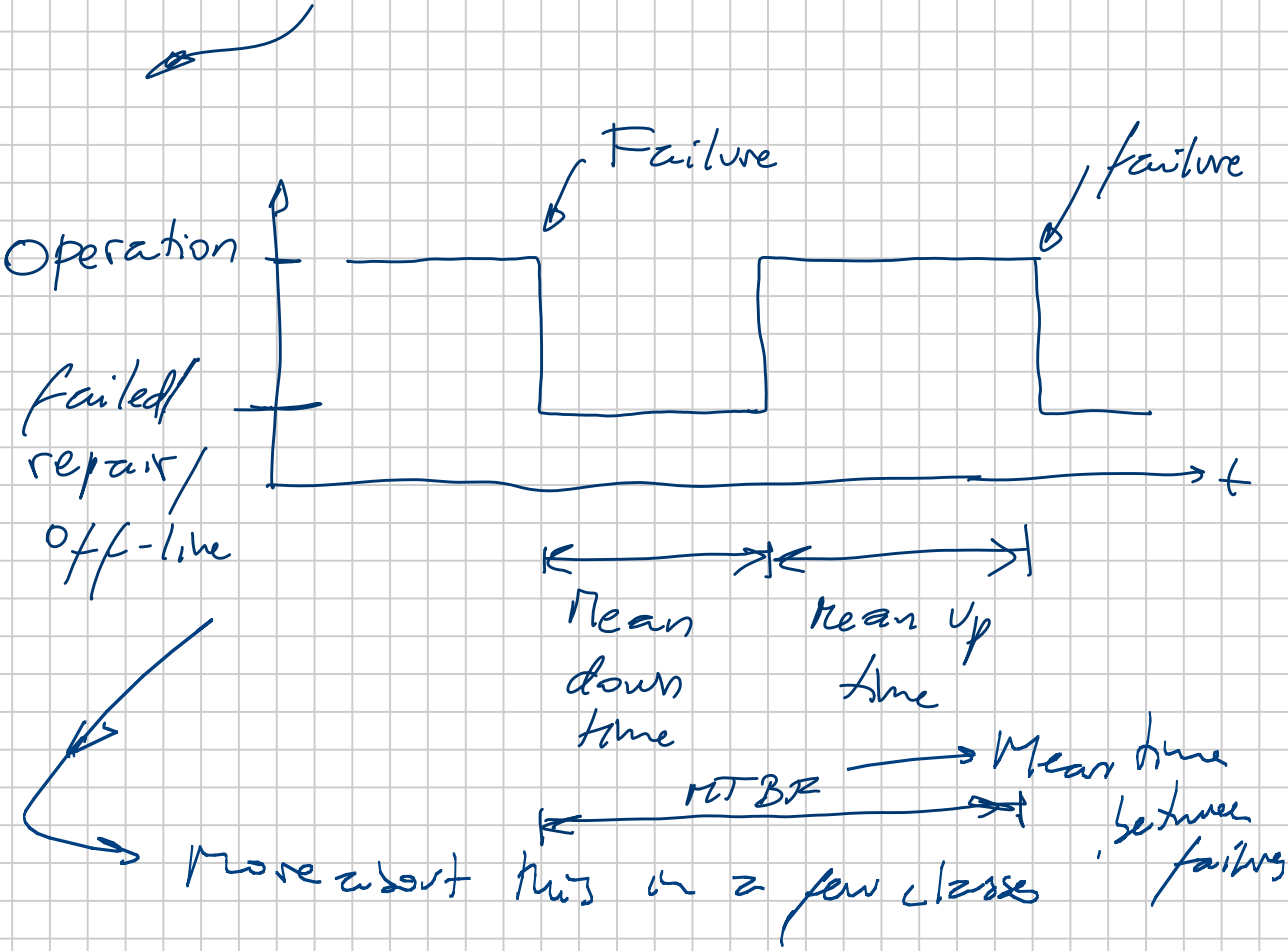


Fully distributed system
→ Cost is higher but the system has higher availability

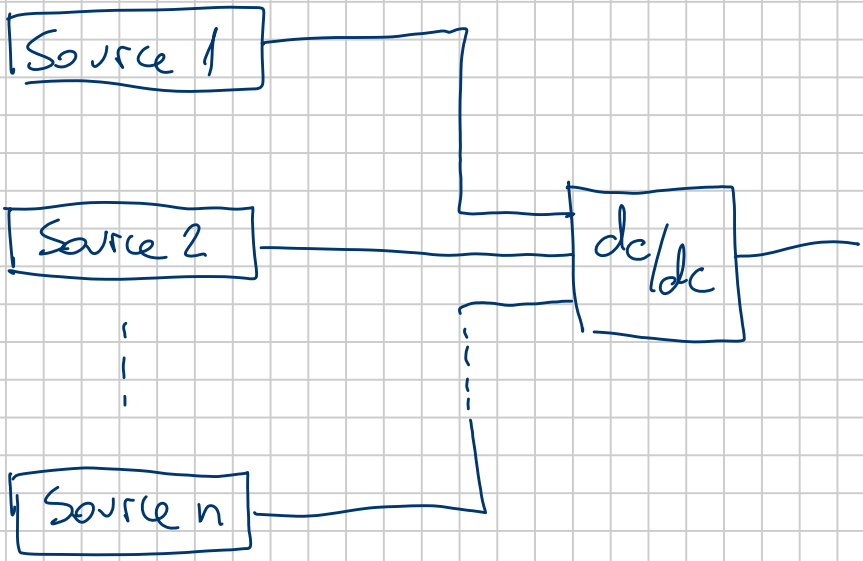
We assume that all voltages are different

Availability (A) = $\frac{\text{Mean up time}}{\text{Mean time between failures}}$

$$A = \frac{MUT}{MTBF}$$



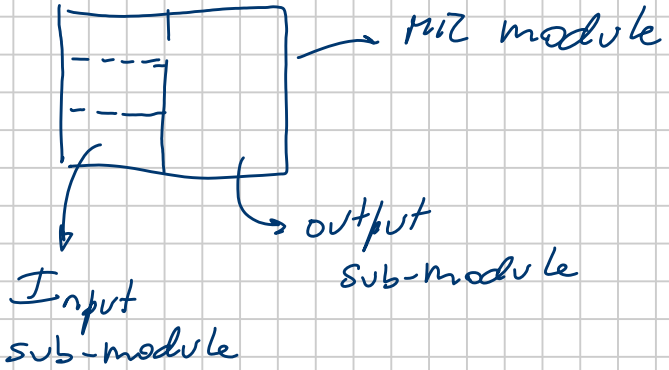
2) Centralized system



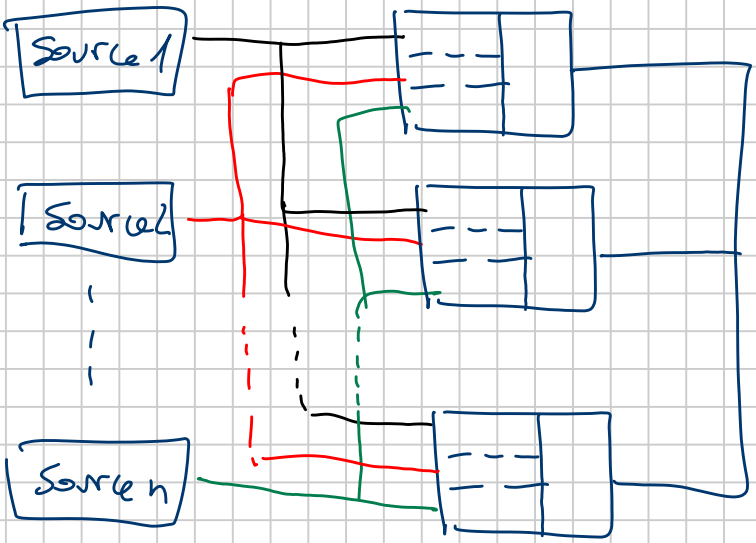
Lower cost but lower availability

- A MiZ is a topology derived from the above to avoid reducing the availability.

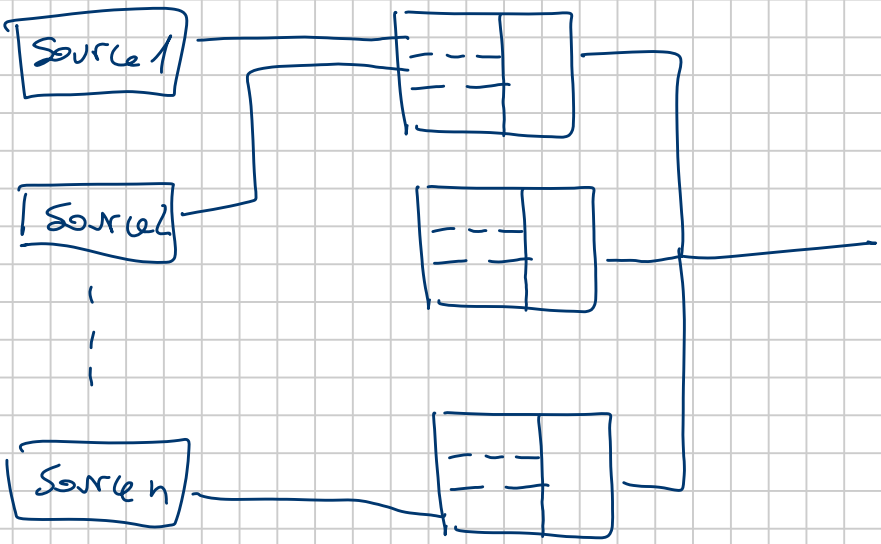
- The difference is to have a modular design



So we can build a modular system:



or.



- Advantages of modular design to avoid reducing the availability → when a module fails I can change it quickly ($< MDT$)
  - → I can implement $n+1$ redundant configurations or other techniques to avoid single point of failures
  - → I have greater flexibility by allowing integration of different sources.

MICs are made from the single-input versions.

There are 2 approaches:

1) Simultaneous input-to-output power transfer
2) No constraints on input-to-output power transfer

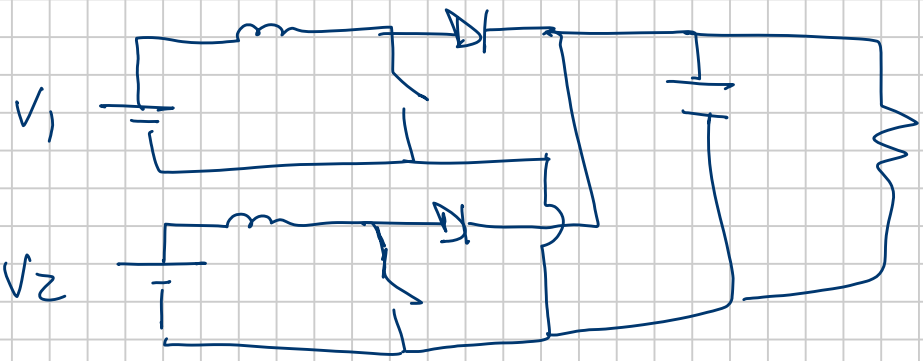
1) Simultaneous input-to-output power transfer

They allow for simultaneous power drawned from each source and injected into the output.

These configurations require more components than the unrestricted cases and often leads to trivial parallel connection of converters sharing only the output capacitor. e.g. MI Boost converter:

Single input Boost:

Multiple input boost:



The switch has no restrictions here.

The problem with this approach is that cost savings are not significant.

Some more information can be found in

A Systematic Approach to Synthesizing Multi-Input DC/DC Converters

Yuan-Chuan Liu and Yaow-Ming Chen

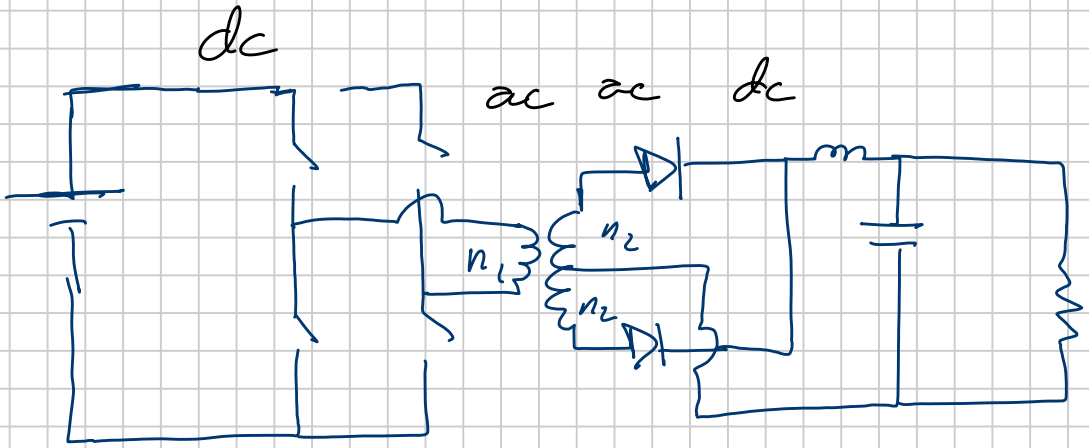
Look in here for additional references

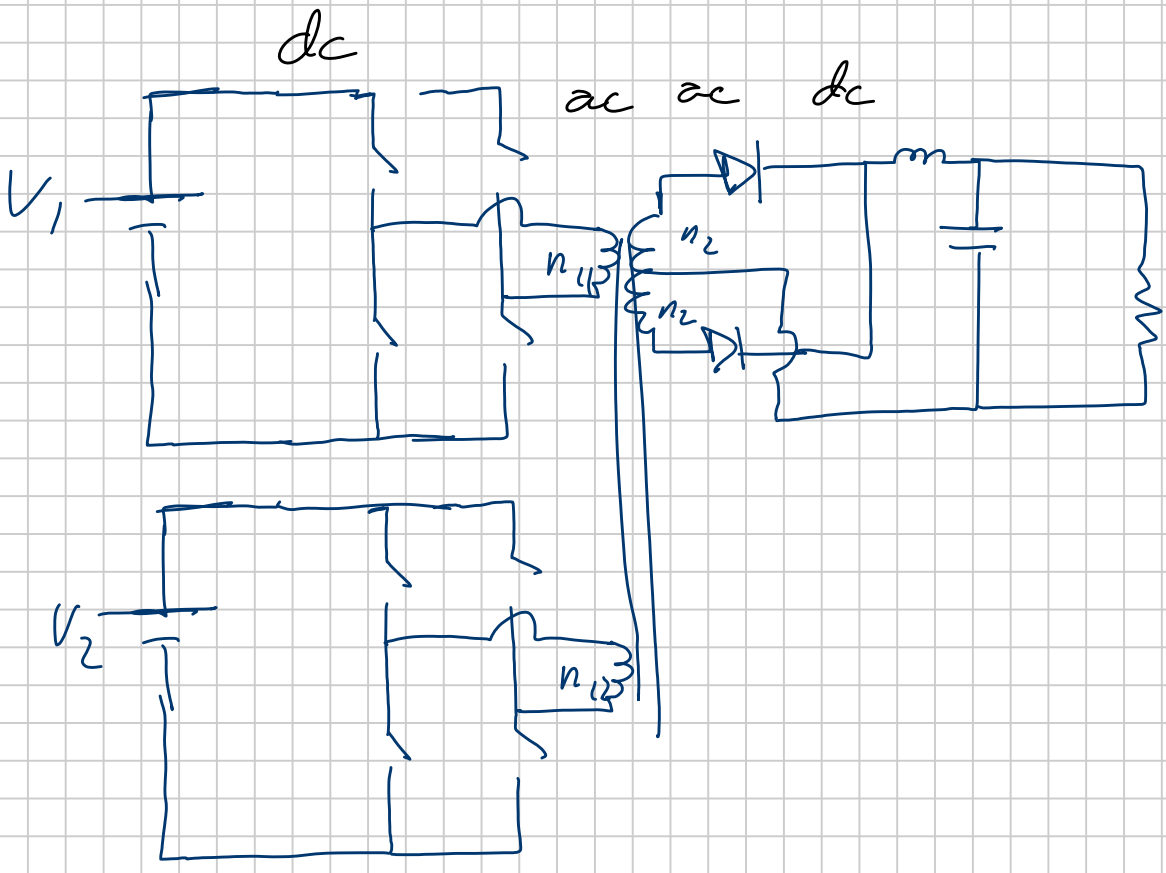
Paper presented in PESC 2007

2) No constraints on input-to-output power transfer

With this approach it is possible to find both cases of non-simultaneous power input and cases allowing simultaneous power drained from sources.

In these cases we can also find some trivial cases in which the inputs are all connected together at the ac intermidiate stage of forward converters.
e.g. full bridge converter.





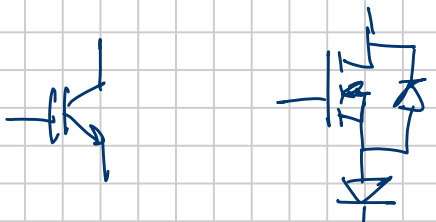
These cases are not going to be discussed further because they are trivial.

Let's see how we synthesize MICS with this approach.

- Assumptions, restrictions and conditions:

1) Power flow is from source to load
2) Total number of components minimization
3) Main switch is FCBB

↳ e.g.



↳ This condition may prevent simultaneous power flow

4) Each of the input voltages are different
5) it should be possible to control each input.

The previous 5 points lead to the following rules

rule #1 Each input cell must contain at least one FCBB switch

↳ this rule is derived from condition #5 above.

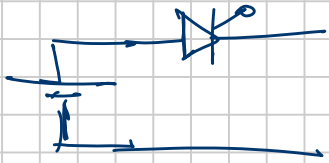
rule #2 The connection of input cell should not lead to redundant switches. I.e., both switch terminals cannot be terminals for the input cell

rule #3 For topologies with center capacitor (e.g. Ćuk and SEPIC) the voltage of this capacitor in the single-input configuration must not depend on the input voltage

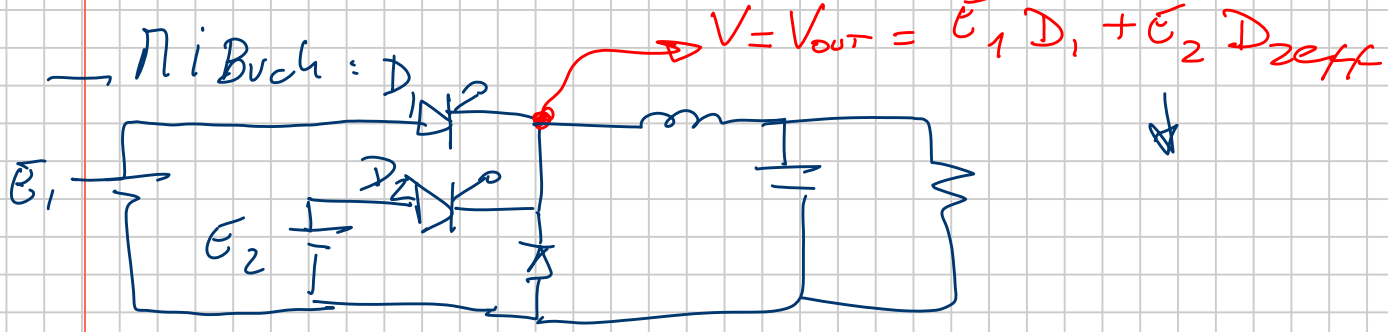
rule #4

Both ends of the input source should not be terminals of the input cell (IC)

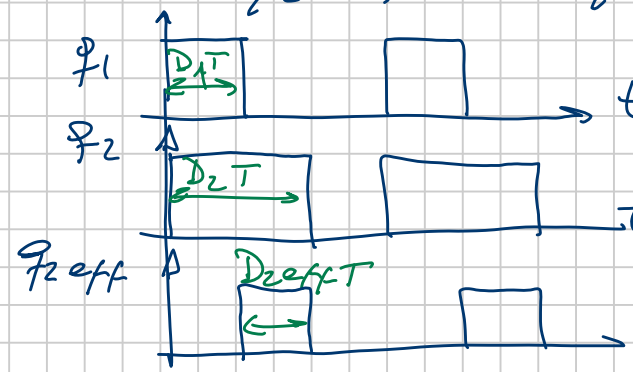
With the above rules and 5 points there is only one feasible input cell:



This is the IC for the Mi Buck and Mi Buck Boost



Assume always that $V_1 > V_2$ and $D_1 < D_2$, the



→ When both Q_1 & Q_2 are closed only Q_1 conducts current.

Hence, the switching period is divided in 3 phases:

1) $D_1 T \rightarrow$ power is taken from source #1

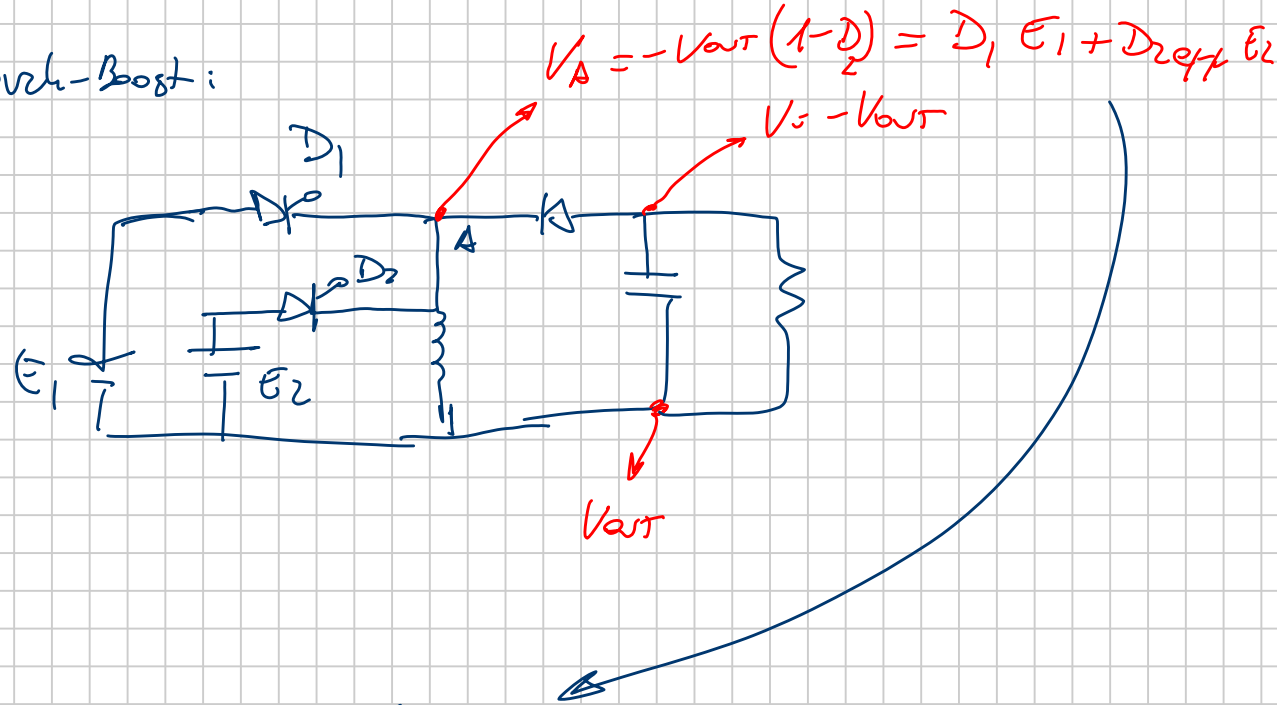
2) $D_{2eff} T \rightarrow$ power is taken from source #2

3) $(1-D_2) T \rightarrow$ Diode conducts

So the power provided by source #2 is limited by the power provided by source #1

$$D_{2eff} = D_2 - D_1$$

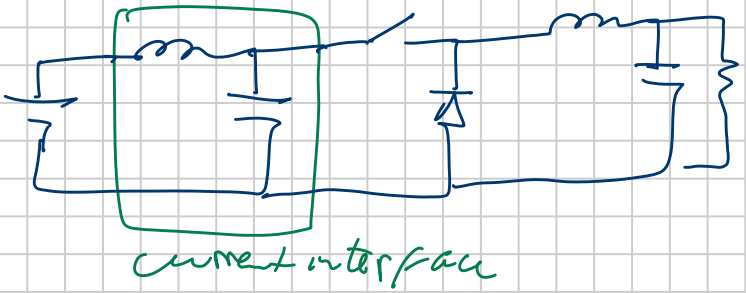
In Buck-Boost:



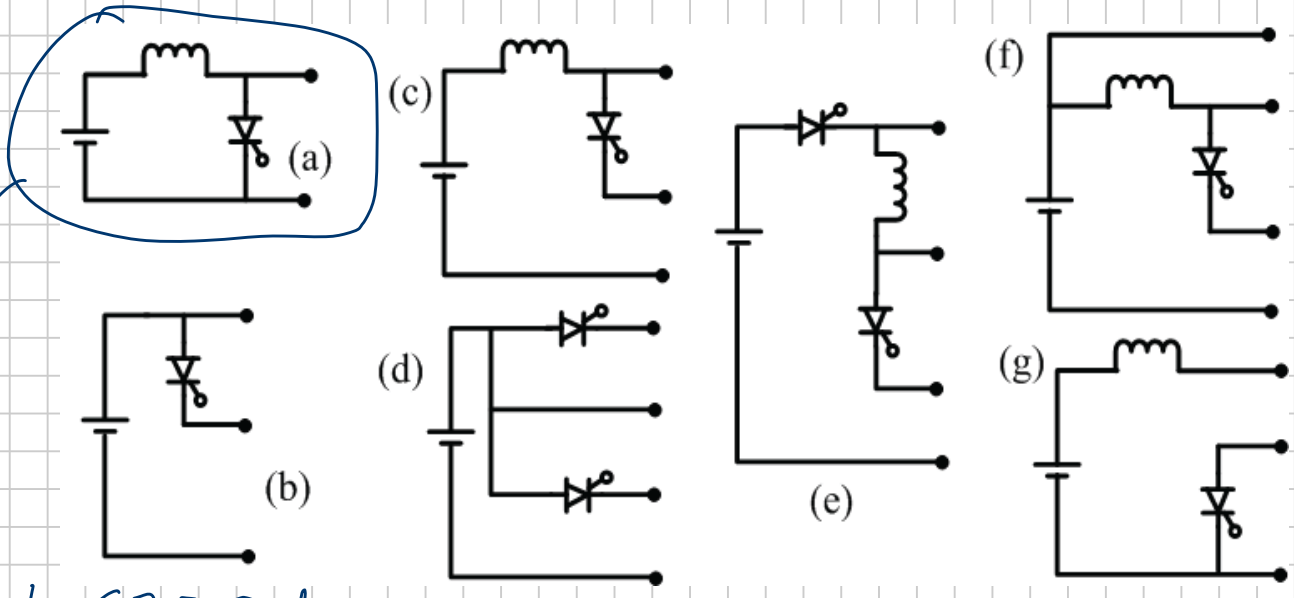
$$V_{out} = -\frac{D_1 E_1 + D_{2eff} E_2}{(1-D_2)}$$

The problem with this IC is that it is not suitable for sources, such as fuel cells, that require low current ripple.

One solution is adding filters:

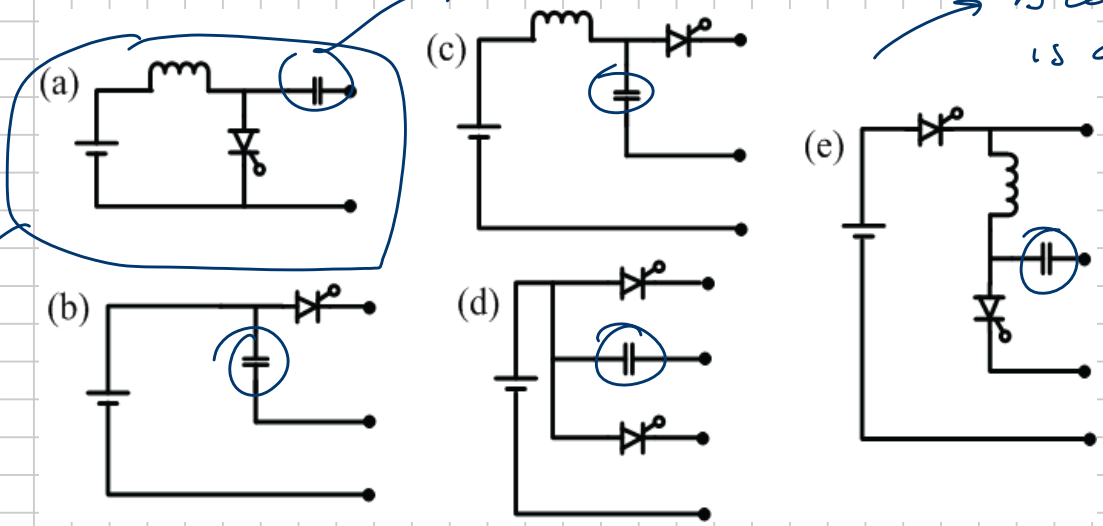


- Unfeasible ICs:



Boost, SEPIC and Cuk input cells

If the condition #2 is relaxed (total number of components minimization) then some new ICs can be realized:

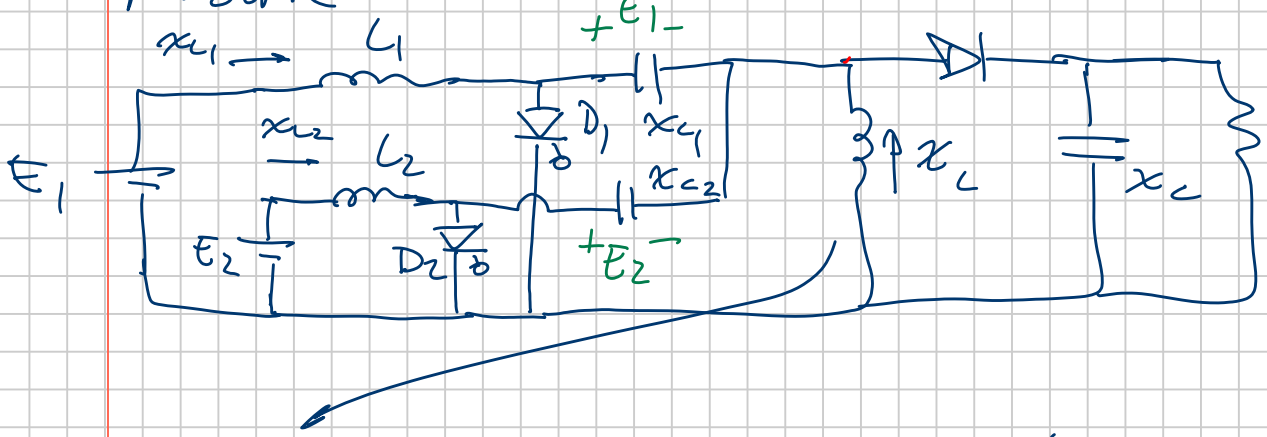


SEPIC & Cuk → Advantages → power is continuously drained from all sources simultaneously

↳ current source input

↳ Disadvantages → Duty cycle in all but one switch depend on the duty cycle of the switch with the highest voltage

MiSEPIC



$$V_{L=0} = -D_1 E_1 - D_{2eff} E_2 + (1-D_2) V_{OUT}$$

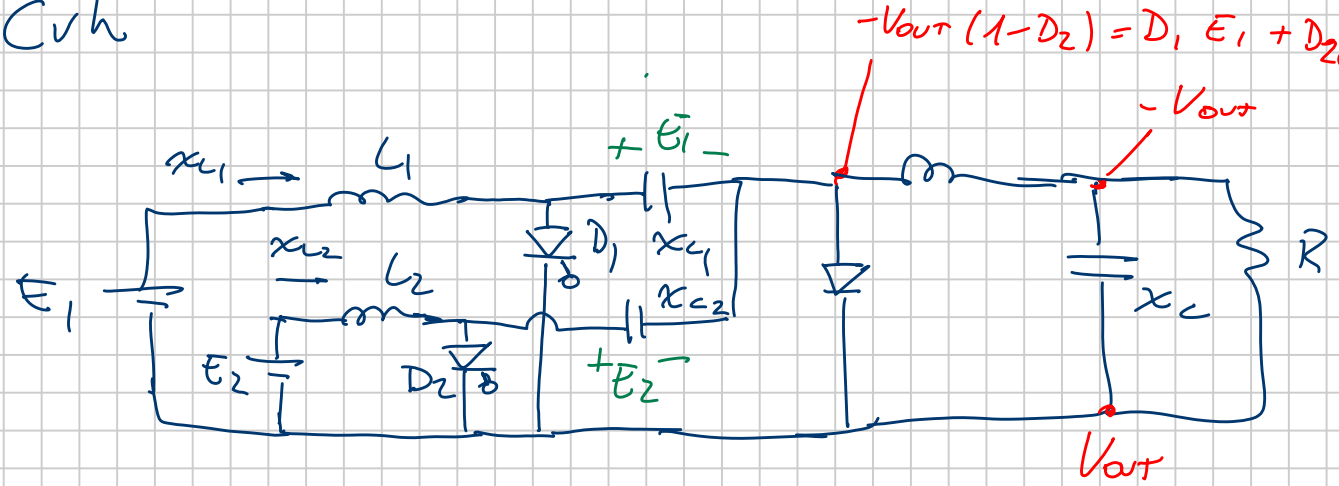
$$V_{OUT} = \frac{D_1 E_1 + D_{2eff} E_2}{(1-D_2)}$$

$q_D = 1 - q_2$

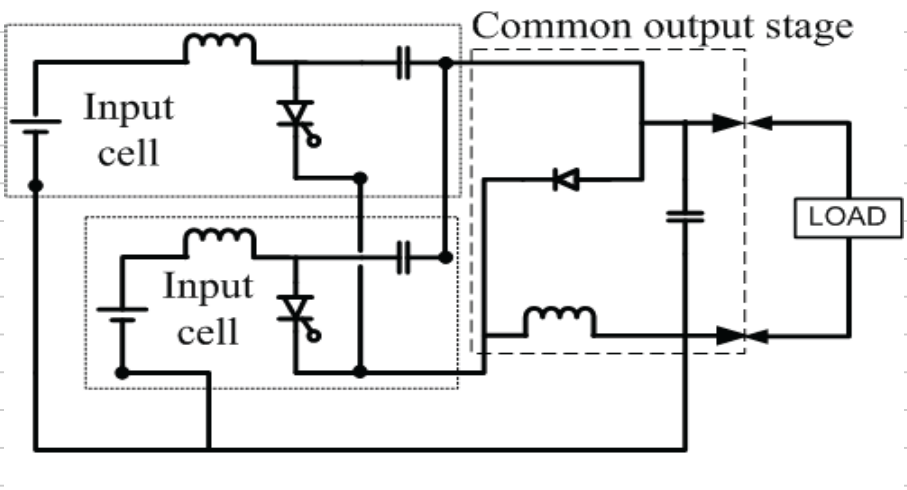
Dynamic equations

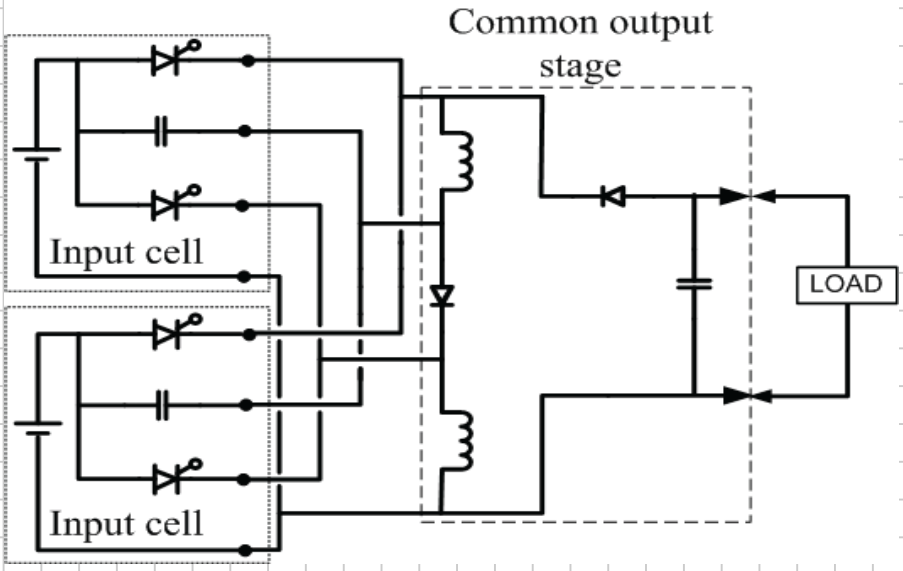
$$\begin{cases} L_1 \dot{x}_{L1} = E_1 - q_{2eff}(x_{C1} - x_{C2}) - q_D (x_C + x_{C1}) \\ L_2 \dot{x}_{L2} = E_2 - q_{1eff}(x_{C2} - x_{C1}) - q_D (x_C + x_{C2}) \\ L \dot{x}_L = q_1 E_1 + q_{2eff} E_2 - q_D x_C \\ C_1 \dot{x}_{C1} = (1-q_1) x_{L1} - q_1 (x_L + x_{L2}) \\ C_2 \dot{x}_{C2} = (1-q_{2eff}) x_{L2} - q_{2eff} (x_C + x_{L1}) \\ C \dot{x}_C = q_D (x_L + x_{L1} + x_{L2}) - \frac{x_C}{R} \end{cases}$$

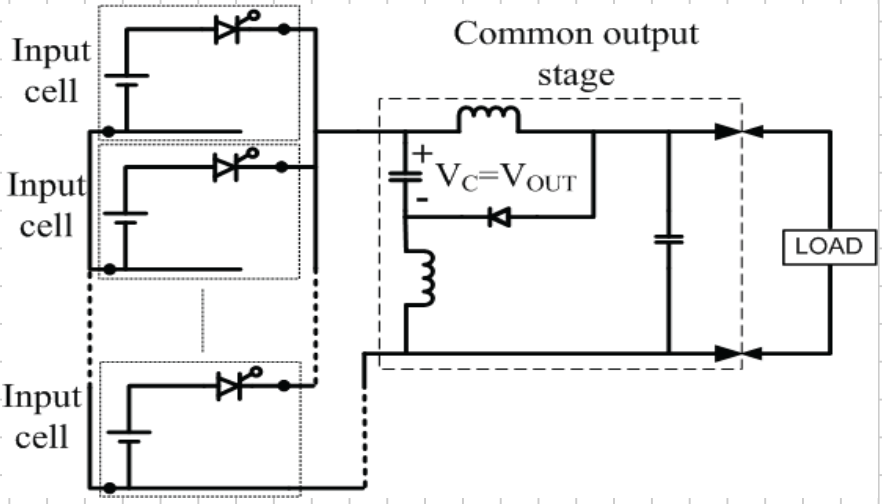
Cuk

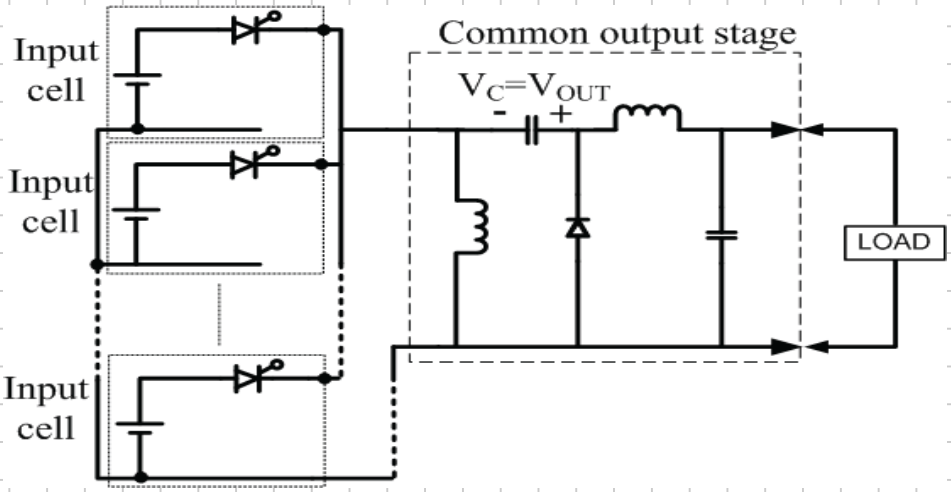


Other topologies



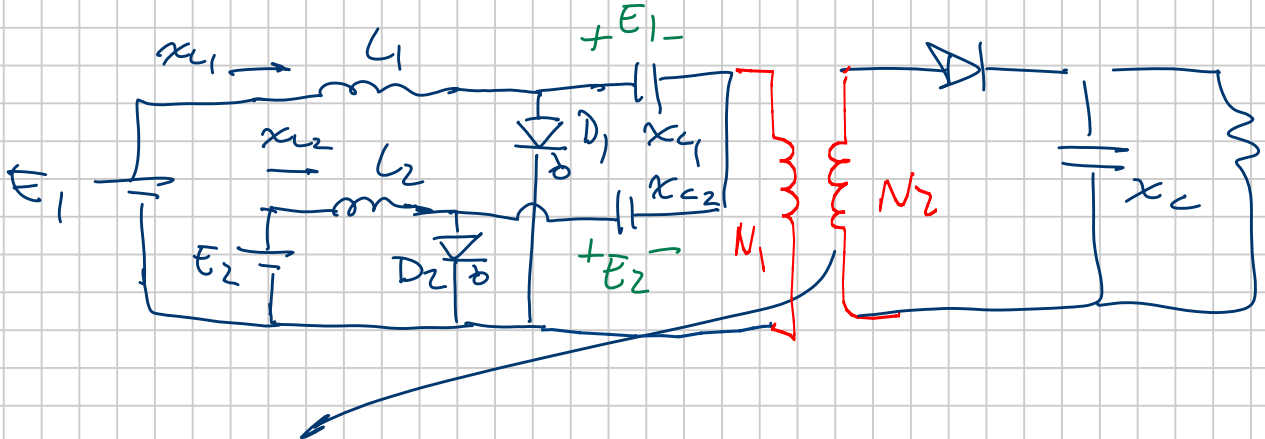






One problem with time shared $N_1:2$ is that there is so much time (T_S) to split among input switches and the output diode which may lead to very small duty cycles for the output diode.

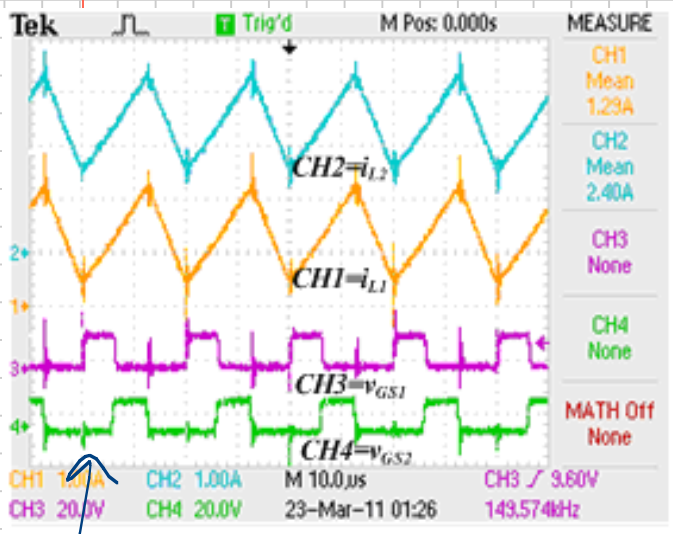
One solution is to add isolation:



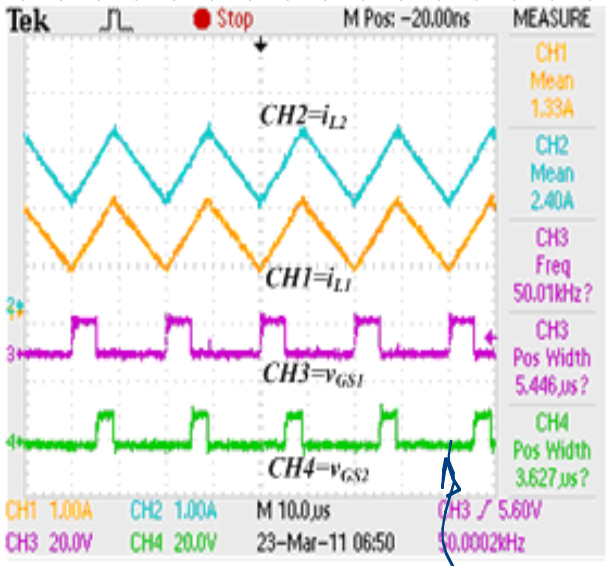
Now $V_{OUT} = \frac{N_2}{N_1} \left(\frac{D_1 E_1 + D_{2eff} E_2}{1 - D_2} \right)$

For $E_1 > E_2$

So same output voltages can be achieved with smaller duty cycle if $N_2 > N_1$



Non isolated



Isolated

$D_{2eff} > D_{2eff\ isolated}$

But same voltages