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1 Overview

SEPICs (Single-Ended Primary-Inductor Converter) make it possible to efficiently convert a dc voltage to either a *lower or higher* voltage. SEPICs are especially useful for photovoltaic-maximum-power-tracking purposes, where the objective is to draw maximum possible power from solar panels at all times, regardless of the load. The drawbacks of SEPICs include the need for an additional inductor and capacitor, a more difficult to control fourth order circuit, and higher current and voltage ratings needed for the MOSFET and diode compared to the Buck and Boost converters. The SEPIC is subject to the same unforgiving safety constraints as the Boost.

2 Theory of Operation

2.1 Relation Between V_{out} and V_{in} in Continuous Conduction

The idealized SEPIC circuit is shown below in Figure 1. Under normal operation, the circuit operates with the inductor currents in continuous conduction (i.e., i_{L1} and i_{L2} are always greater than zero).

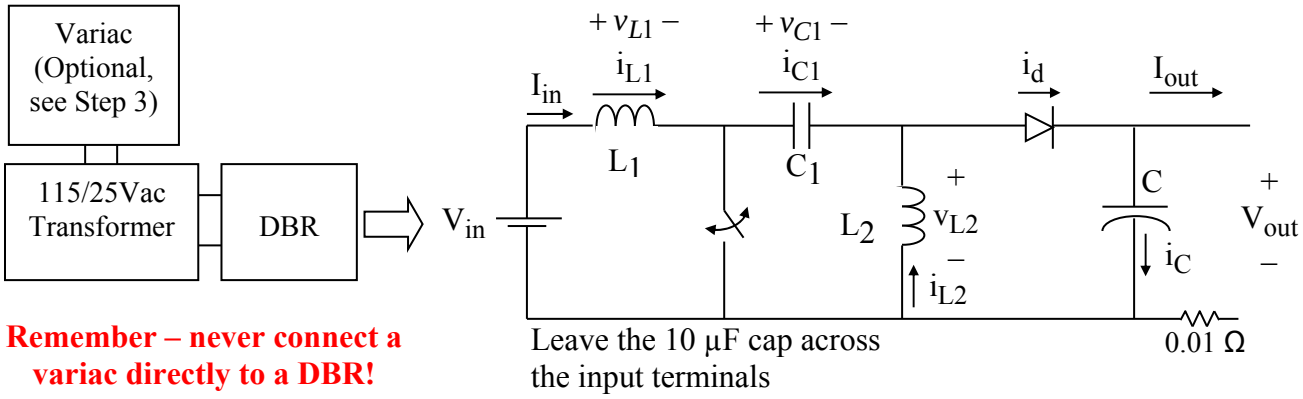


Figure 1. DC-DC SEPIC Circuit

The first important relationship comes from the fact that capacitor C_1 should be large enough so that voltage v_{C1} has low ripple. Applying average KVL around the loop formed by V_{in}, L_1, C_1, and L_2 , and recognizing that the average voltages across L_1 and L_2 are each zero, yields

$$v_{C1,avg} = V_{in} \ . \tag{1}$$

The second important relationship comes by applying KCL in the average sense at the node atop L_2. Since the average currents in C_1 and C are both zero, then

$$i_{L2,avg} = i_{d,avg} = I_{out} \ . \tag{2}$$

Assuming continuous conduction, the circuit has two topologies: switch closed and switch open as shown in Figures 2a and 2b respectively.

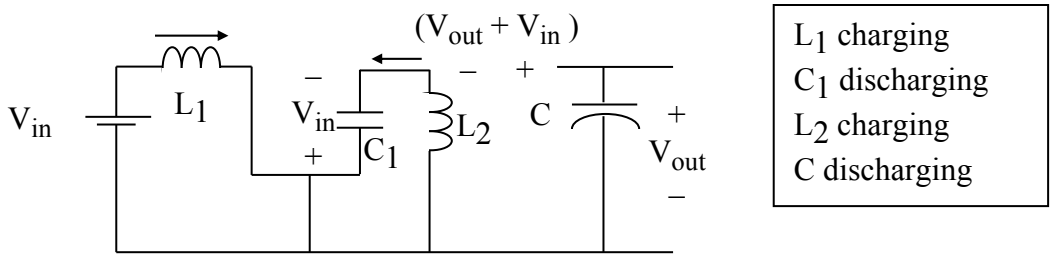


Figure 2a. Switch Closed for DT Seconds

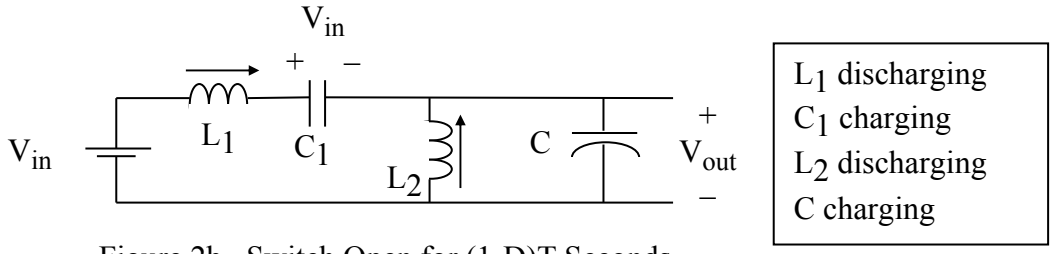


Figure 2b. Switch Open for (1-D)T Seconds

When the switch is closed (Figure 2a), C_1 is in parallel with L_2 and thus begins to charge L_2 as C_1 discharges. The diode can be seen to be reversed biased by a simple KVL check around the loop including C, the diode, and C_1. During this time, L_1 is in parallel with Vin and therefore charges. The current i_{L1} increases at the rate of

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1}, \ 0 \le t \le DT \ , \ \text{[KVL, from left-most loop, Figure 2a.]} \tag{3}$$

so that L_1 is charging. When the switch is open (Figure 2b), the diode is forward biased, and i_{L1} decreases at the rate of

$$\frac{di_{L1}}{dt} = \frac{-V_{out}}{L_1}, \ DT < t < T \ , \ \text{[KVL, from large loop, Figure 2b.]} \tag{4}$$

so that L_1 is discharging. The voltage across L_1 is shown in Figure 3.

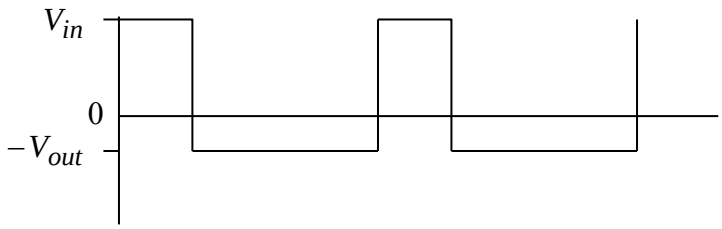


Figure 3. Inductor L_1 Voltage in Continuous Conduction

Because of the steady-state inductor principle, the average voltage across L_1 is zero. Since v_{L1} has two states, both having constant voltage, the average value of v_{L1} is

$$\frac{(V_{in})DT + (-V_{out})(1-D)T}{T} = 0,$$

so that

$$V_{in}D - V_{out} + V_{out}D = 0 \ . \tag{5}$$

Simplifying the above yields the final input-output voltage expression

$$V_{out} = \frac{DV_{in}}{1-D}. \tag{6}$$

Thus, the converter is in "buck" mode for D < 0.5, and in "boost" mode for D > 0.5.

The assumption of a lossless circuit requires input power to equal output power, so

$$I_{out} = \frac{(1-D)I_{in}}{D}. \tag{7}$$

2.2 Inductor Currents in Continuous Conduction

The graph of i_{L1} is shown in Figure 4. For photovoltaic (PV) applications, it is desirable to have low ripple in i_{L1} to keep the solar panel operating at the peak of its maximum power curve.

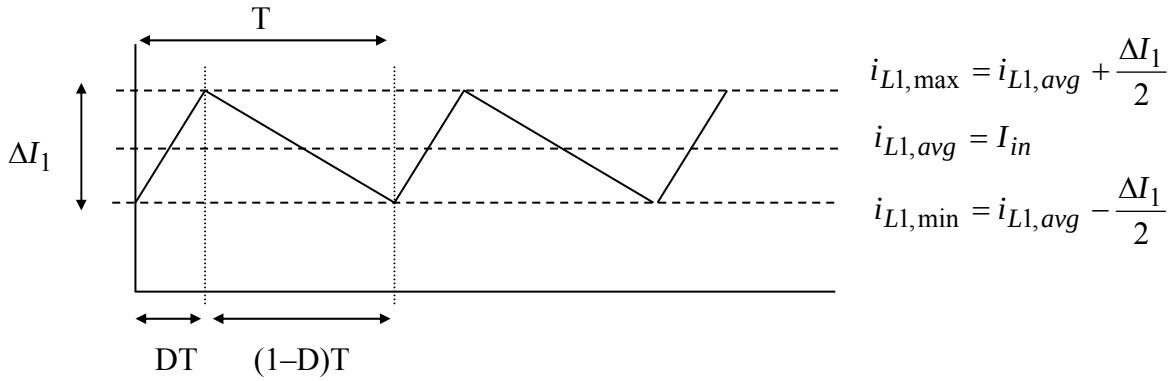


Figure 4. Inductor L_1 Current Waveform for Continuous Conduction

From Figure 4 and Equation (4), when the switch is open (i.e., L_1 is discharging),

$$\frac{di_{L1}}{dt} = \frac{-V_{out}}{L_1},$$

so that

$$\Delta I_1 = \frac{V_{out}}{L_1} \bullet (1-D)T = \frac{V_{out}(1-D)}{L_1 f}, \tag{8}$$

where f is the switching frequency.

The boundary of continuous conduction for L_1 is when $i_{L1,\min} = 0$, as shown in Figure 5.

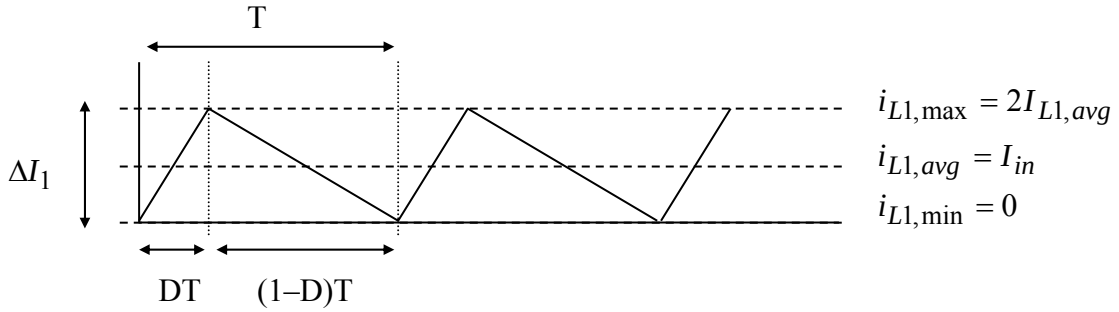


Figure 5. Inductor L_1 Current at the Boundary of Continuous Conduction

Thus, at the boundary,

$$2I_{in} = \frac{V_{out}(1-D)}{L_{1boundary} f}, \tag{9}$$

so that

$$L_{1boundary} = \frac{V_{out}(1-D)}{2I_{in}f} = \frac{DV_{in}}{1-D} \bullet \frac{(1-D)}{2I_{in}f} = \frac{DV_{in}}{2I_{in}f} \quad . \tag{10}$$

As D approaches unity,

$$L_1 > \frac{V_{in}}{2I_{in}f} \tag{11}$$

will guarantee continuous conduction. Note in (10) and (11) that continuous conduction can be achieved more easily when I_{in} and f are large.

The graph of i_{L2} is shown in Figure 6.

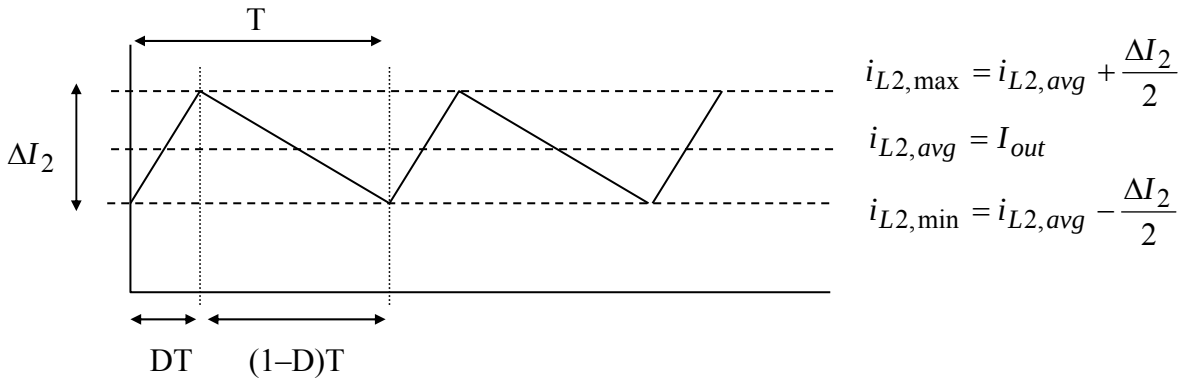


Figure 6. Inductor L_2 Current Waveform for Continuous Conduction

From Figures 2b and 6, when the switch is open (i.e., L_2 is discharging),

$$\frac{di_{L2}}{dt} = \frac{-V_{out}}{L_2} = \frac{\Delta I_2}{(1-D)T},$$

so that

$$\Delta I_2 = \frac{-V_{out}(1-D)T}{L_2} = \frac{-V_{out}(1-D)}{L_2 f} \quad , \tag{12}$$

where f is the switching frequency.

The boundary of continuous conduction for L_2 is when $i_{L2,\min} = 0$, as shown in Figure 7.

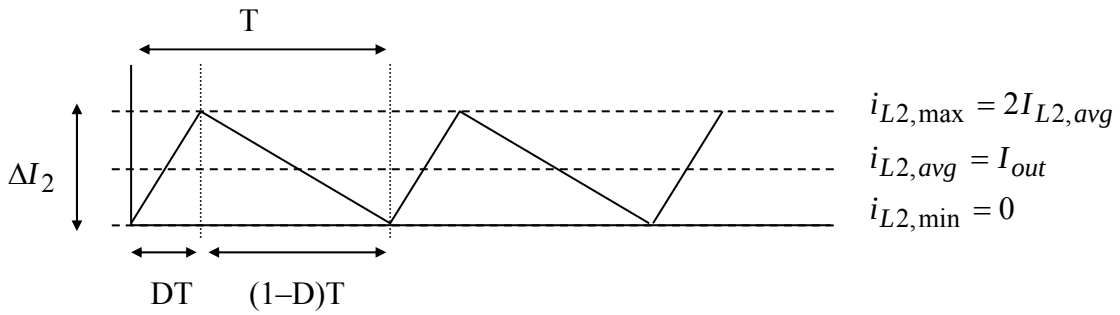


Figure 7. Inductor L_2 Current at the Boundary of Continuous Conduction

Thus, at the boundary,

$$2I_{out} = \frac{V_{out}(1-D)}{L_{2boundary} f}, \tag{13}$$

so that

$$L_{2boundary} = \frac{V_{out}(1-D)}{2I_{out} f} \ . \tag{14}$$

Since the maximum value of (14) occurs at D → 0,

$$L_2 > \frac{V_{out}}{2I_{out} f} \tag{15}$$

will guarantee continuous conduction for L_2 for all D. Note in (14) and (15) that continuous conduction can be achieved more easily when I_{out} and f are large.

2.3 Current Ratings for Continuous Conduction Operation

Continuous current waveforms for the MOSFET, the capacitors, and the diode in continuous conduction are shown in Figure 8 on the following page. Corresponding waveforms for the inductors were shown previously in Figures 4 and 6.

Following the same formulas and reasoning used for the buck converter, conservative current ratings for components L_1, L_2, the MOSFET, and the diode follow.

For L_1, using Figure 5,

$$I_{L1,rms,\max}^2 = I_{in}^2 + \frac{1}{12}(2I_{in})^2 = I_{in}^2\left(1+\frac{1}{3}\right),$$

so that

$$I_{L1,rms,\max} = \frac{2}{\sqrt{3}} I_{in} \ . \tag{16}$$

Similarly, for L_2, using Figure 7,

$$I_{L2,rms,\max} = \frac{2}{\sqrt{3}} I_{out} \ . \tag{17}$$

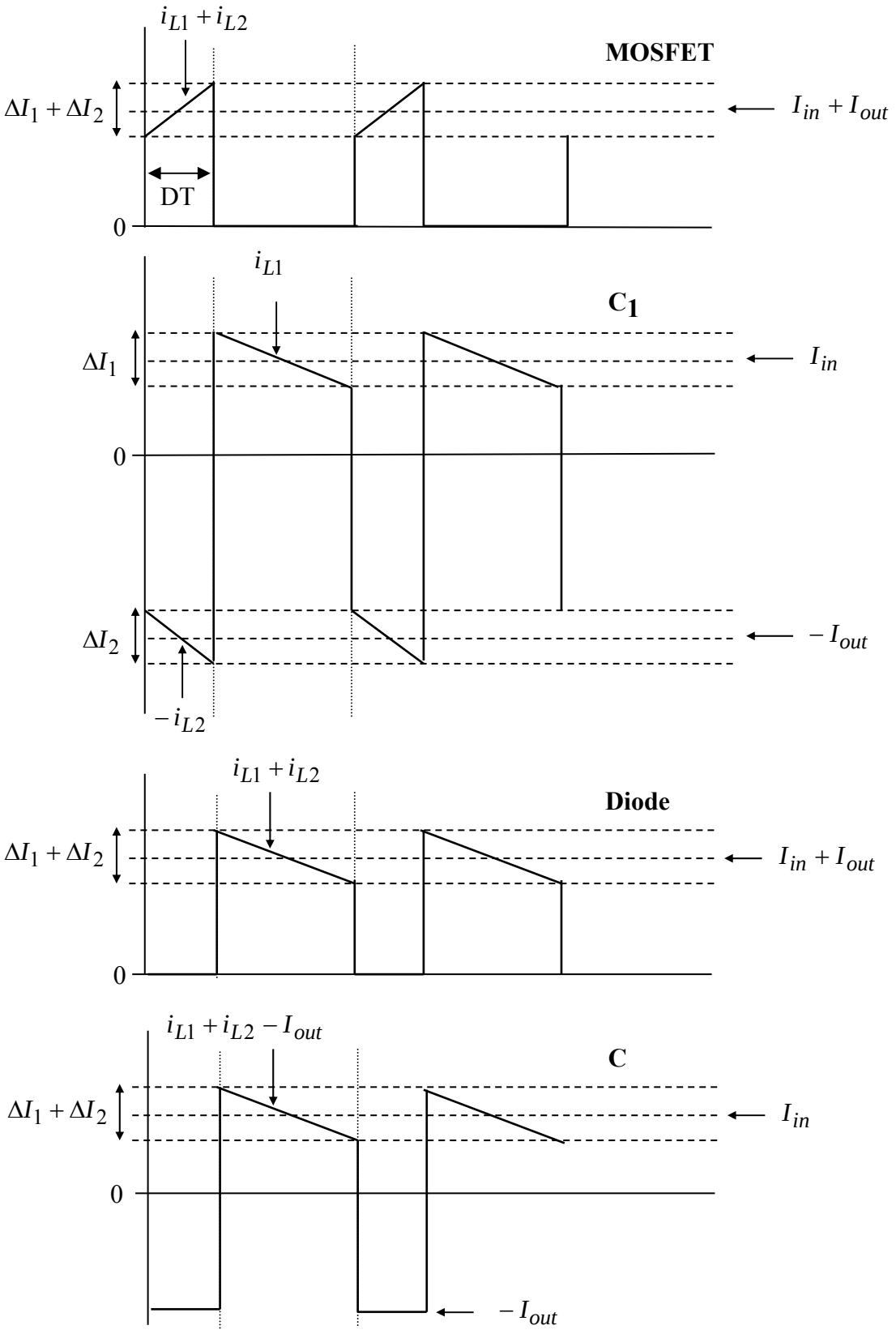


Figure 8. Current Waveforms for MOSFET, Capacitors, and Diode in Continuous Conduction

For the MOSFET and diode, assuming large worst-case D, and using Figure 8,

$$I_{MOSFET,rms,\max} = \frac{2}{\sqrt{3}}\left(I_{in} + I_{out}\right), \tag{18}$$

$$I_{Diode,rms,\max} = \frac{2}{\sqrt{3}}\left(I_{in} + I_{out}\right). \tag{19}$$

For C1 and C, using Figure 8,

$$I_{C1,rms,\max} = \frac{2}{\sqrt{3}} I_{in} \text{ or } \frac{2}{\sqrt{3}} I_{out} \text{ , whichever is larger.} \tag{20}$$

$$I_{C,rms,\max} = \frac{2}{\sqrt{3}} I_{in} \text{ or } I_{out} \text{ , whichever is larger.} \tag{21}$$

2.4 Voltage Ratings for Continuous Conduction Operation

Referring to Figure 2b, when the MOSFET is open, it is subjected to (V_{in} + V_{out}). Because of the usual double-voltage switching transients, the MOSFET should therefore be rated 2(V_{in}+V_{out}).

Referring to Figure 2a, when the MOSFET is closed, the diode is subjected to (V_{in} + V_{out}). The diode should be rated at 2(V_{in}+V_{out}).

Note – "stiff" voltages across capacitors C1 and C will help hold down overshoots on the MOSFET and diode in this circuit.

2.5 Output Capacitor Voltage Ripple

The maximum ripple voltage calculation for output capacitor C follows from Figure 8 and is the same as for the boost converter, namely

$$\Delta V = \left|\frac{\Delta Q}{C}\right| = \frac{I_{out} DT}{C} = \frac{I_{out} D}{Cf}.$$

The maximum peak-to-peak ripple thus occurs as $D \to 1$ and is

$$\Delta V_{\max} = \frac{I_{out}}{Cf}. \tag{22}$$

Comparing the current graphs for C_1 and C in Figure 8 during the DT "switch closed" period, it can be seen graphically that the ripple voltage on C_1 and C are the same, i.e. Equation (22).

3 The Experiment

Note: The SEPIC is subject to the same safety concerns as the Boost converter, namely:

Important Safety Considerations when using a SEPIC:

A) **Never allow D to approach 1, since V_{in} will be short circuited by the switch!!**
(Recall under steady-state dc conditions with the switch fully closed, L_1 → short!!)

B) To avoid high output voltages, always keep a load attached to the SEPIC output when input power is applied. When the switch is open (under CCM) energy stored in the inductors will be passed to the output. Thus, a no load condition will cause the output capacitor voltage to increase, possibly exceeding its rating. Therefore, to avoid excessive output voltages, always keep a load attached to the SEPIC when it is operating. Do not exceed 90 V_{dc} on the converter output.

1. Reconfigure the buck or boost components according to Figure 1 in this document. Secure new components C_1 and L_2. Make all connections. Capacitor C_1 is bipolar *(i.e., not polarized).*

2. Connect the MOSFET Firing Circuit to your converter, **using short leads**. Double check your range of D. **Use your D-Limiter potentiometer to reduce your range of D so that the upper limit is set to be 0.8.**

3. Double-check that the polarity of your output capacitor is correct.

4. Before connecting power, **make sure that a 5 Ω ceramic power resistor is connected as a load.** View V_{GS} on Channel #1, **adjust D to the minimum setting**, and $f \approx 90$ kHz. Connect Channel #2 to view V_{DS}. *(Recall, the ground clip of the Channel #2 probe should not be attached to the circuit, but instead it should be clipped back onto its own lead in-cable so that it does not dangle!)* Set the trigger for Channel #1.

Important Note: The first time you energize your converter, feed the 115:25V transformer through a variac to the DBR, so that you can SLOWLY increase the voltage dial from zero while reading the variac ammeter to detect short circuits before they become serious. A common problem is to have the MOSFET in backward, so that its internal antiparallel diode creates a short circuit. The ammeter on the variac is an excellent diagnostic tool. Once you are convinced that your circuit is working correctly, the variac is then optional. **Remember – your SEPIC requires dc input power from a DBR.**

Does your circuit have a short? If so, do the following:

1. Make sure that your MOSFET is not connected backwards.
2. Observe V_{GS} on the MOSFET as you vary D and f. Does the waveform look correct?
3. Unplug the wall wart. Does the short circuit go away? If not, your MOSFET may be shorted – so, disconnect the MOSFET from the converter, and perform the voltage-controlled resistance test on the MOSFET, or ask a TA for assistance.

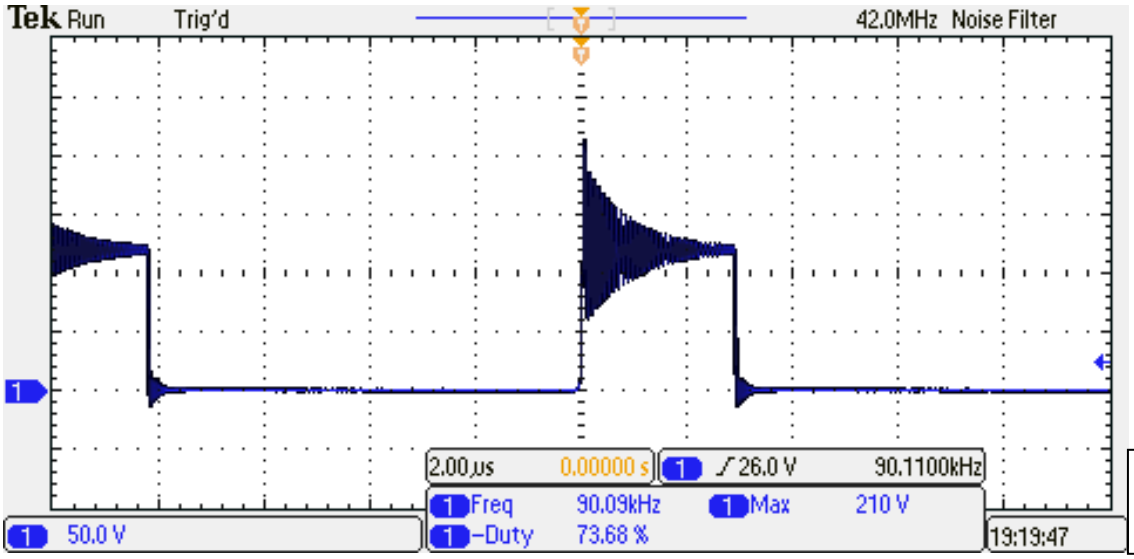
5. Connect a 115:25 V_{ac} transformer to a DBR. Connect the DBR to your SEPIC, **keeping the wires short (i.e., 3" or less)**. Then, energize the 115:25 V_{ac} transformer and DBR. If using a variac, adjust the dial so that the output of the **transformer** is approximately 27-28 Vrms.

Picture 1: SEPIC Laboratory Test Setup

6. With $f \approx 90$ kHz, **slowly** increase D from its smallest value to obtain $\mathbf{V_{out}}$ **= 10, 20** $\mathbf{V_{dc}}$*(within ±2* V_{dc}*)*, while recording D, V_{in} , V_{out}, I_{in} , I_{out}. Note by viewing V_{DS} whether or not the circuit is in continuous current operation. **For the 20 V** condition, compute input and output powers and efficiency. **Do not go above 20 V with the 5 Ω load.**

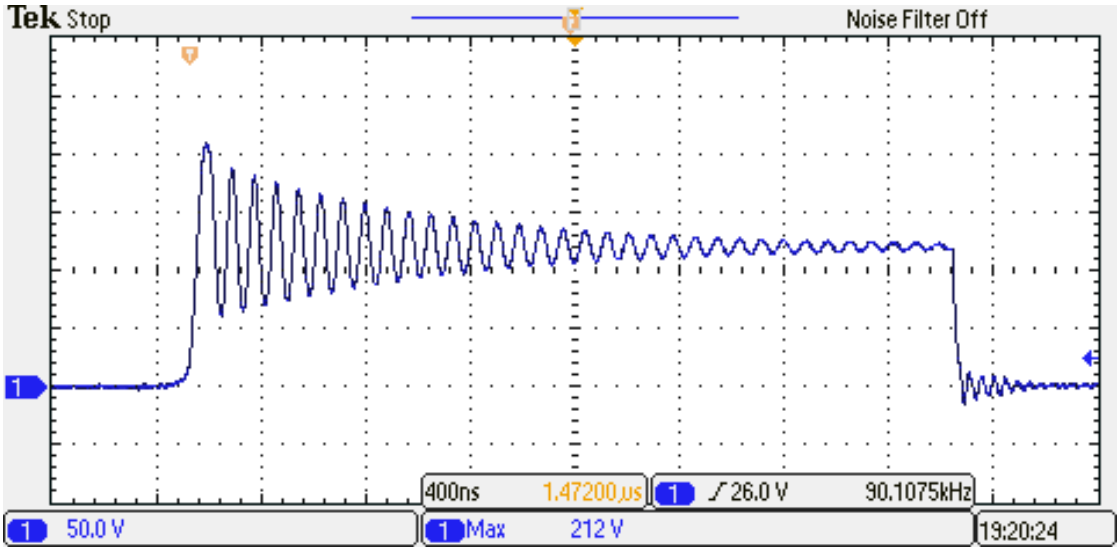
7. Turn off the DBR, and connect a **10 Ω ceramic power resistor** as a load. Continue the experiment as before, adjusting D, and taking D, V_{in} , V_{out}, I_{in} , I_{out} readings with $\mathbf{V_{out}}$ **= 30, 40 V**. **Do not go above 40 V with the 10 Ω load.**

8. Turn off the DBR, and connect a **120 V, 150 W light bulb** as a load. Continue the experiment, adjusting D, taking D, V_{in} , V_{out}, I_{in} , I_{out} readings with $\mathbf{V_{out}}$ **= 50, 60, 70, 80, 90 V**. For the 90 V case, save a screen snapshot of V_{DS} that shows the peak value.



Save screen snapshot #1

Picture 2: V_{DS} for SEPIC at V_{out} = 90 V_{dc}, 90 kHz



Picture 3: V_{DS} for SEPIC at V_{out} = 90 V_{dc}, 90 kHz *(Zoomed-In)*

9. For your report, compute converter efficiencies for the **20 V, 40 V, and 90 V** conditions for V_{out}. Also, plot actual and theoretical V_{out}/V_{in} versus D on one graph.

Optional Section – SEPIC with a Solar PV panel

The following **optional** steps are to be performed with a solar panel pair as the power source and with good sun (i.e., panel short circuit current ≥ 3.5 A, and a clear sky, bright forecast). Please make certain sky conditions are clear. The point of this section is to see how changing D affects your V_{out}. Yet, an unstable V_{in} will also affect V_{out} via Eq (6). *(Recall pictures from the Boost lab showing how quickly changing solar conditions can affect V_{in}).* Thus, you will want to take your data with V_{in} relatively constant (i.e., clear skies) to avoid fluctuations in V_{in}.

Please heed the following warnings if you attempt to do this optional section:

A. If you use the Position #18 work station and connect to your SEPIC using the set of red & black wires already provided, know these wires *bypass* the yellow connection box, ammeter, and the on/off switch. Thus, if sun is shining, these dc voltage wires are live!! ***(****Note: This same safety concern is dealt with by solar PV installers every day, for as they install and wire up solar PV panels, due to daylight, these panel voltages are live!****)***

B. As prior noted for a SEPIC, make certain your D ≤ 0.8 (use your D-limiter potentiometer to reduce your upper limit threshold as a safety measure), and make sure you always have a load connected before you apply an input voltage!

The solar panel voltage that you measure should be at the panel (i.e., the left-most analog voltmeter)

10. Note the sky conditions. Connect a solar panel pair directly to a 120 V, 150 W light bulb. Measure panel voltage, panel current, and compute solar panel output power. (*Note: If you connect to Position #18 via the direct panel wiring provided, to measure I_{panel}, you will need to add an input shunt resistor to your SEPIC circuit.*)

11. Next, insert the SEPIC between the solar panel pair and a 120 V, 150 W light bulb. With $f \approx 90$ kHz, sweep D over its range to measure and plot the I-V and P-V characteristics of the panel pair. Record the maximum power value.

4 Parts List

Parts List

- Series capacitor, Xicon 33 μF, 50 V, high-frequency bipolar (i.e., not polarized), rated 14 A peak-to-peak ripple current (Mouser #140-BPHR50V33)
- Second inductor like the one in the buck converter
- Second heat sink like the one in the buck converter
- Second nylon screw and lock nut like the one in the buck converter
- Two additional, 2-terminal, 30 A terminal blocks (these may not be needed by students who are building minimum footprint circuits)
- 8" nylon cable tie (in student parts bin)

Extra parts

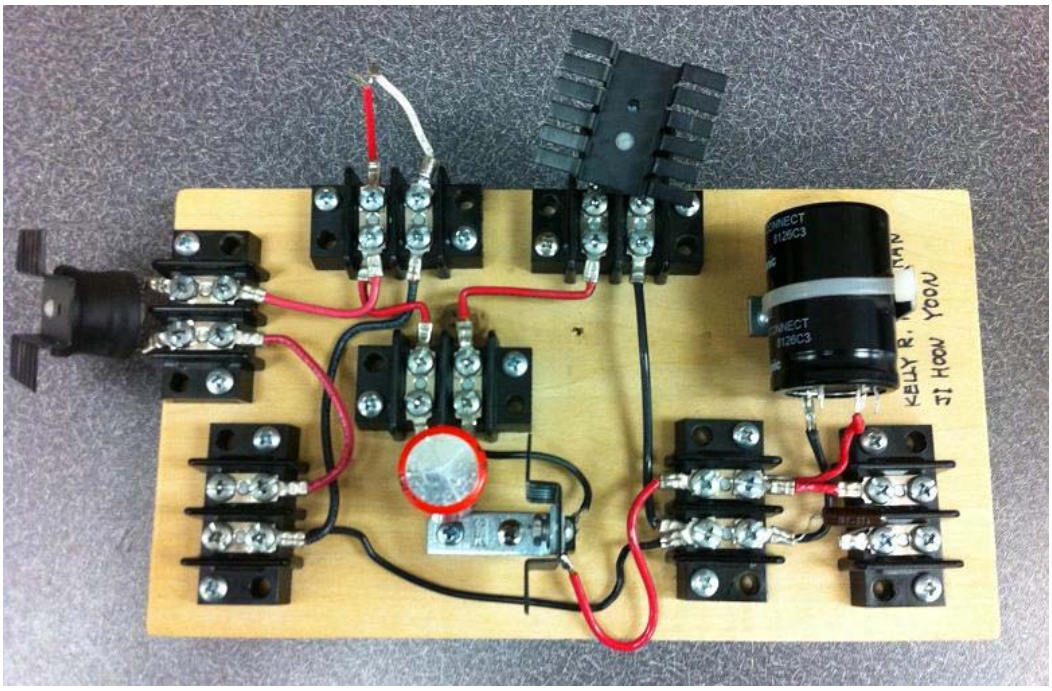
For the student parts bin and screw cabinet, at least

- 5 of the 250 V MOSFETs (individually bagged)
- 5 of the 200 V, 16 A ultrafast rectifiers
- 5 of the dc jacks
- 5 of the 10 kΩ linear taper potentiometers
- 5 of the PWM modulator chips
- 5 of the inverting driver chips
- 5 of the 14-pin sockets
- 5 of the 8-pin DIP sockets
- 5 of the green plugs
- 10 of the #4-40 x 1" flat slotted nylon screws and lock nuts

Plastic bags for parts

- 6"x6", 4mil

5 Circuit Build Photo



Picture 4: SEPIC Circuit Build

6 Appendix: Worst Case Component Ratings

Worst-Case Component Ratings Comparisons for DC-DC Converters

Converter Type	Input Inductor Current (Arms)	Output Capacitor Voltage	Output Capacitor Current (Arms)	Diode and MOSFET Voltage	Diode and MOSFET Current (Arms)
Buck	$\frac{2}{\sqrt{3}} I_{out}$	$1.5 V_{out}$	$\frac{1}{\sqrt{3}} I_{out}$	$2 V_{in}$	$\frac{2}{\sqrt{3}} I_{out}$
Boost	$\frac{2}{\sqrt{3}} I_{in}$	$1.5 V_{out}$	I_{out}	$2 V_{out}$	$\frac{2}{\sqrt{3}} I_{in}$
SEPIC	$\frac{2}{\sqrt{3}} I_{in}$	$1.5 V_{out}$	$\max\left(\frac{2}{\sqrt{3}} I_{in}, I_{out}\right)$	$2(V_{in} + V_{out})$	$\frac{2}{\sqrt{3}}(I_{in} + I_{out})$

Additional Components for SEPIC Converter

Series Capacitor Voltage	Series Capacitor (C_1) Current (Arms)	Series Capacitor (C_1) Ripple Voltage (peak-to-peak)	Second Inductor (L_2) Current (Arms)
$1.5 V_{in}$	$\max\left(\frac{2}{\sqrt{3}} I_{in}, \frac{2}{\sqrt{3}} I_{out}\right)$	$\frac{I_{out}}{C_1 f}$	$\frac{2}{\sqrt{3}} I_{out}$

Comparisons of Output Capacitor Ripple Voltage

Converter Type	Volts (peak-to-peak)
Buck	$\frac{I_{out}}{4Cf}$
Boost	$\frac{I_{out}}{Cf}$
SEPIC	$\frac{I_{out}}{Cf}$

Minimum Inductance Values Needed to Guarantee Continuous Current

Converter Type	For Continuous Current in the Input Inductor	For Continuous Current in L2
Buck	$L > \frac{V_{out}}{2I_{out}f}$	–
Boost	$L > \frac{V_{in}}{2I_{in}f}$	–
SEPIC	$L_1 > \frac{V_{in}}{2I_{in}f}$	$L_2 > \frac{V_{out}}{2I_{out}f}$