Condensed CV
Lizy Kurian John

EDUCATION: *(Year, Degree, Institution, major)*

1993	PhD	The Pennsylvania State University, Computer Engineering
1989	MS	The University of Texas at El Paso, Computer Engineering
1984	BS	The University of Kerala, India, Electronics and Communication

EXPERIENCE: *(Institution, rank(s), beginning and ending dates for each rank)*

The University of Texas at Austin	B. N. Gafford Professor in Electrical Engr	2009 - date
The University of Texas at Austin	Professor and Centennial Teaching Fellow	2007-2009
The University of Texas at Austin	Assoc Professor and Centennial Teaching Fellow	2001-2007
The University of Texas at Austin	Assistant Professor	1996-2001
The University of South Florida	Assistant Professor	1993-1996

HONORS AND AWARDS:

2011 Outstanding Engineering Alumnus of the Pennsylvania State University
2009 IEEE Fellow
2005 IBM University Partnership Award
2002 Advisor of the George H. Mitchell Undergraduate Student Achievement Award winner
2001 IBM Austin Center for Advanced Studies (CAS) Fellow
1996 NSF CAREER Award
1996 Oak Ridge Junior Faculty Enhancement Award

Best Paper Awards
2016 ACM Design Automation Conference (DAC)
2015 IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation
2009 IEEE International Conference on Parallel Processing (ICPP)
1999 IEEE International Performance Conference on Computing and Communication (IPCCC)

Best Paper Runner Up:
2015 IEEE International Conference on Parallel Processing (ICPP)

Best Paper Nominations:
2011 IEEE/ACM Supercomputing Conference (SC'11)
2011 IEEE/ACM Micro conference (MICRO '11)
2010 IEEE International Symposium on High Performance Computer Architecture (HPCA)

UT Austin Awards:
2004 TEXAS Alumni Association (Texas EXES) Teaching Award
2001 Engineering Foundation Faculty Award, College of Engineering, UT Austin
1999 Halliburton, Brown and Root Engineering Foundation Young Faculty Award, College of Engr

Other Honors:
1989 Graduate School Marshal for the December 1989 commencement at The University of Texas at El Paso
1977 National Talent Search Scholarship, NCERT INDIA, 1977-1984
1984 3rd Rank in the Kerala University B.Sc. Engineering Degree Exam
1979 Ist Rank, 1st out of 70,462 students in the Kerala University Pre Degree Exam, India
1977 2nd rank, 2nd out of 275,554 students in the Kerala State Higher Secondary School Exam, India

Keynotes/Plenary Talks:

2015 Samsung SARC Technical Forum Invited Speech, "Machine Learning for Power Modeling and Prediction"
2015 Huawei Strategic Workshop, Shenzhen, China, "Many Big, Many Little: Who will crunch all the Big Data?
2014 Keynote Speech, BPOE Workshop in conjunction with ACM ASPLOS, Salt Lake City, Utah

2013 Invited Speech, ACM Supercomputing Conference, Performance Evaluation for Large Scale Systems: (Host: Bill Kramer, UIUC)
2011 ACM International Conference on Performance Engineering (ICPE) Keynote Talk, Karlsruhe, Germany
2008 Keynote speech, IBM Center for Advanced Studies (CAS) Conference
2004 Workshop on Commercial Workload Characterization (CAECW), Madrid, Spain

PATENTS:

1. U. S. Patent 9,235,397, Method and Apparatus for increasing task execution speed, January 12, 2016
2. U. S. Patent 9,038,039, Apparatus and Method for Accelerating Java Translation, May 19, 2015
3. U. S. Patent 8,359,597, "Workload-guided application scheduling in multi-core system based at least on application branch transition rates, Jan 22, 2013
4. US Patent 8,250,350, "Computer System with non-volatile write-protected memory based operating system and secure system architecture, Aug 21, 2012
5. US Patent 8,230,407, "Apparatus and method for accelerating Java translation", July 24, 2012
6. US Patent 8,214,629, Computer system with secure instantly available applications using non-volatile write-protected memory", July 3, 2012
7. US patent 8,041,931, "Branch prediction apparatus, systems, and methods", Granted Oct 18, 2011 (Patent has been licensed by UT)
8. U S Patent 7,370,183,"Branch Predictor comprising a split branch history shift register". Patent has been licensed by UT.
9. U S Patent 7,107, 434, " System, Method and Apparatus for Allocating Hardware Resources using Pseudo Random Sequences". Patent has been licensed by UT
10. U S Patent 5,867,422 " Computer Memory Chip with field Programmable Memory Cell Arrays", Granted Feb 1999.

BOOKS AUTHORED:

1. Digital Systems Design Using VHDL, Charles Roth and Lizy K. John, 3rd edition (Cengage Publishers, 2016, Book in Production Stage)
2. Digital Systems Design Using Verilog, Charles Roth, Lizy K. John, and Byeong Kil Lee, Cengage Publishers, 2014, 581 pages)
3. Digital Systems Design Using VHDL, Charles Roth and Lizy K. John, 2nd edition (Thompson Engineering, 2006-2007, 580 pages)

BOOKS EDITED:

1. Computer Performance Evaluation and Benchmarking, CRC Press, 2005 (289 pages) (with L. Eeckhout)
2. Workload Characterization of Emerging Computer Applications, Kluwer Academic Publishers, 2001, ISBN 0-7923-7315-4
3. Workload Characterization for Computer System design, edited by L. K. John and A. M. Maynard, Kluwer Academic Publishers, 2000, 209 pages, ISBN 0-7923-7777-x.
4. Workload Characterization: Methodology and Case Studies, edited by L. John and A. M. Maynard, IEEE Computer Society, 153 pages, ISBN 0-7695-0452-3

RESEARCH CONTRIBUTION SUMMARY:

Lizy John is a leader in the areas of performance/power modeling of computer systems, and workload characterization. She has contributed to the design and evaluation of microprocessors with her innovative methodologies for early design stage power and performance evaluations. Her contributions include proxy benchmarks for pre-silicon performance evaluation, synthetic proxies for database, Java and web server workloads , performance-event based power models, automatically generated stress benchmarks for finding realistic maximum power, etc. Her research developed methodologies to characterize applications at an abstract level, which allowed to identify the generic properties of the application in terms of its memory access behavior, locality, branch behavior, instruction level parallelism, etc. Utilizing the abstract metrics of program behavior, a machine-independent program

behavior model was generated. Her group's workload characterization led to program similarity/dissimilarity studies and clustering techniques that have been used in benchmark selection and subsetting by the SPEC, a consortium of companies such as IBM, Intel, Oracle, HP, etc. Currently, she is working on emerging workloads including cloud computing, big data workloads, trying to create meaningful and manageable benchmarking strategies for these types of contemporary and emerging workloads.

Power modeling

Prof. John was one of the first to show how power models can be built using performance metrics as a proxy. She showed how a processor power model can be built with just 2 performance counters. Google Scholar shows that her SIGMETRICS 2003 paper on this topic has been cited 224 times. Her "trickle down" power estimation research developed a methodology to estimate power of the system including memory and disk utilizing events at the core. This work [ISPASS 2007 paper] has 155 citations. Recently her team has developed a cross-platform performance/power model using machine learning, which won the DAC Best Paper award in 2016. Prof. John's research in performance evaluation and workload characterization has had a profound impact on academia and the industry. Digital power meters that use processor events as a proxy has become very common now including in processors from Intel, AMD and Samsung.

1. Tao Li and Lizy Kurian John, "Run-time Modeling and Estimation of Operating System Power Consumption", In Proceedings of the International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), 2003, pp. 160-171. (224 citations)
2. William Lloyd Bircher and Lizy K. John, Complete System Power Estimation: A Trickle-Down Approach Based on Performance Events, ISPASS (IEEE International Symposium on Performance Analysis of Systems and Software) April 2007 (155 citations)
3. Lloyd Bircher and Lizy K. John, Complete System Power Estimation using Processor Performance Events, **IEEE Transactions on Computers**, Vol. 61, No. 4, pp. 563-577, April 2012 (103 citations)
4. W. Lloyd Bircher and Lizy K. John, " Analysis of Dynamic Power management on Multi-Core Processors", Proceedings of the International Conference on Supercomputing (ICS), 2008, pp/ 327-338, (37 accepts/ 140 submissions) (69 citations)
5. Wooseok Lee, Sunwoo, A. Gerstlauer, and L. K. John, "PowerTrain: A Learning-based Calibration of McPAT Power Models", ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2015
6. W. Lloyd Bircher, M. Valluri, J. Law and L. John, "Runtime Identification of Microprocessor Energy Saving Opportunities", International Symposium on Low Power Electronics and Design (ISLPED), Aug 2005, pp. 275-280. (Acceptance rate: 53 accepted/233 submissions = 23%)
7. Jian Chen and Lizy K. John, "Program Scheduling for Heterogeneous Multicore Processors", Proceedings of the 46th Design Automation Conference (DAC) July 2009 (75 citations)
8. Sudhanva Gurumurthi, Anand Sivasubramaniam, Mary Jane Irwin, Narayanan Vijaykrishnan, Mahmut Kandemir, Tao Li, and Lizy Kurian John, "Using Complete Machine Simulation for Software Power Estimation: The SoftWatt Approach", In Proceedings of the 2002 International Symposium on High Performance Computer Architecture (HPCA), Feb 2002, pp. 141-150. (Acceptance rate: 26 accepted/130 submissions = 20%) (220 citations)

Use of Machine Learning in Performance/Power/Reliability Evaluation

Estimating the power and thermal characteristics of a processor is essential for designing its power delivery system, packaging, cooling, and power/thermal management schemes. Power models that estimate the power consumption of each functional unit/hardware component from first principles are slow and tedious to build. Dr. John's research used machine learning can be used to create power models that are fast and reasonably accurate, and to calibrate analytical models that estimate power. Dr. John's research also crafted a very important application for machine learning - to create max power stressmarks. Manually developing and tuning so called stressmarks is extremely

tedious and time-consuming while requiring an intimate understanding of the processor. Dr. John's research created a framework that uses machine learning for the automated generation of stressmarks. Yet another application for machine learning in Dr. John's research is in cross-platform performance and power prediction. If one model is slow to run real-world benchmarks/workloads, is it possible to predict/estimate the performance/power by using runs on another platform? Are there correlations that can be exploited using machine learning to make cross-platform performance and power predictions?

1. Xinnian Zheng, Lizy K. John, and Andreas Gerstlauer, Accurate Phase Level Cross-Platform Power and Performance Estimation, DAC 2016 (accepted) (Best Paper award)
2. Arun Nair, Stijn Eyerman, Lizy K. John, Lieven Eeckhout, A First-Order Mechanistic Model for Architectural Vulnerability Factor, ACM International Symposium on Computer Architecture (ISCA) 2012, pp. 273-284
3. Karthik Ganesan and Lizy K. John. MAximum Multicore POwer (MAMPO) - An Automatic Multithreaded Synthetic Power Virus Generation Framework for Multicore Systems, Best paper finalist in the SuperComputing Conference (SC 2011), Seattle, WA, Nov 2011
4. Youngtaek Kim, Lizy Kurian John, "Automated di/dt stressmark generation for microprocessor power delivery networks," *International Symposium on Low Power Electronics and Design(ISLPED)*, pp. 253-258, Aug. 2011.
5. Arun Arvind Nair, Lizy Kurian John, and Lieven Eeckhout, " AVF Stressmark: Towards an Automated Methodology for Bounding the Worst-Case Vulnerability to Soft Errors", Proceedings of the Annual International Symposium on Microarchitecture (MICRO-2010), December 2010
6. K. Ganesan, Jungho Jo, W. Lloyd Bircher, D. Kaseridis, Zhibin Yu, and Lizy K. John, SYMPO: A Systematic Approach for Escalating System-Level Power Consumption using Synthetic Benchmarks", Proceedings of the 19th International Conference on Parallel Architectures and Compilation Techniques (PACT), Vienna, Austria, September 11-15, 2010.
7. A. Joshi, L. Eeckhout, L. K. John, and C. Isen, "Automated Microprocessor Stressmark Generation", Proceedings of the IEEE International High Performance Computer Architecture (HPCA) Symposium, 2008, pp. 229-239.

Pre-silicon performance evaluation

Modern microprocessors contain hundreds of millions of transistors and are built using millions of lines of VHDL/Verilog code. Pre-silicon estimation of performance and power of such designs for real-world workloads is important to identify good design points early in the design process. Lizy John applied workload characterization to create abstract models of workloads and synthetic test sequences, which became very instrumental in pre-silicon performance/power modeling. Her research has been able to create synthetic clones of real applications and benchmarks which act as performance/power proxies but without any functionality. The IBM POWER processor performance models have been validated using the synthetic benchmark approach created by her research. Lockheed Martin found these techniques useful to clone proprietary applications. The Semiconductor Research Consortium funded her research to develop pre-silicon design evaluation techniques. AMD, Freescale and Intel found these techniques extremely valuable in early stage design evaluation.

1. Lieven Eeckhout, Robert Bell Jr., Bastiaan Stougie, Koen De Bosschere, Lizy K. John, "Control Flow Modeling in Statistical Simulation for Accurate and Efficient Processor Design Studies", Proceedings of the International Symposium on Computer Architecture (ISCA), Munich, Germany, June 2004, pp. 350-361. (Acceptance rate: 31accepted/217 submissions = 14%) (116 citations)
2. Robert H. Bell, Rajiv R. Bhatia, Lizy John, Jeff Stuecheli, Ravel Thai, John Griswell, Paul Tu, Louis Capps, Anton Blanchard, "Automatic Testcase Synthesis and Performance Model Validation for High-Performance PowerPC Processors", Proceedings of the International Symposium on Performance Analysis of Systems and Software (ISPASS), March 2006, pp. 154-165. (Acceptance rate: 24 accepted/81 submissions = 30%)
3. Zhibin Yu, Lieven Eeckhout, Tao Li, Lizy K. John, , "GPGPU-MiniBench: Accelerating GPGPU Micro-Architecture Simulation", IEEE Transactions on Computers, 2015, Vol. 64, Issue 11, pp. 3153-3166

4. Arun Nair, Stijn Eyerman, Jian Chen, Lizy John, Lieven Eeckhout, "Mechanistic Modeling of Architectural Vulnerability Factor", **ACM Transactions on Computer Systems**, 2015, Vol. 32, Issue 4

5. Karthik Ganesan and Lizy K. John, Automatic Generation of Miniaturized Synthetic Proxies for Target Applications to Efficiently Design Multicore Processors, **IEEE Transactions on Computers**, Vol. 63, No. 4, pp. 833-846, April 2014

Performance Impact of Emerging Workloads and Contemporary Programming Paradigms:

Workload characterization and identification of bottlenecks allows computer architects to design computer systems that yield high performance, energy-efficient operation and reliability. Many emerging workloads contain thick software stacks with several layers of complex software accessing databases or various libraries and interacting with complex hardware. The suitability of various hardware features for the specific requirements of the software cannot be visualized intuitively any more. Understanding the nature of programs and the workload behavior leads to the design of improved computer architectures. Lizy John's research group focuses on workload characterization of emerging application domains and emerging processor architectures. In past research, Lizy John has characterized Java workloads, multimedia workloads, smart phone apps, data base workloads (SQL and NoSQL) and identified bottlenecks during the execution of these types of workloads.

1. R. Radhakrishnan, N. Vijayakrishnan, L. K. John, A. Sivasubramaniam, J. Rubio, and J. Sabarinathan, "Java Runtime Systems: Characterization and Architectural Implications", **IEEE Transaction on Computers**, Feb 2001, Vol.50, No. 2, pp. 131-146 (82 citations)
2. Deepu Talla, Lizy John, and Doug Burger, "Bottlenecks in multimedia processing with SIMD style extensions and architectural enhancements", **IEEE Transactions on Computers**, Volume 52, Number 8, ISSN 0018-9, Aug 2003, pp. 1015-1031 (130 citations)
3. R. Radhakrishnan, N. Vijaykrishnan, L. K. John and A. Sivasubramaniam, "Architectural Issues in Java Runtime Systems", Proceedings of the IEEE International Symposium on High Performance Computer Architecture (HPCA-2000), Toulouse, France, Jan 2000, pp. 387-398. (Acceptance rate: 35 accepted/163 submissions = 21%) (56 citations)
4. L. Tao, L. K. John, N. Vijayakrishnan, A. Sivasubramaniam, A. Murthy, and J. Sabarinathan, "Using Complete System Simulation to Characterize SPECjvm98 Benchmarks", Proceedings of the ACM International Conference on Supercomputing (ICS 2000), Santa Fe, New Mexico, May 2000, pp. 22-33. (Acceptance rate: 33 accepted/122 submissions = 28%) (53 citations)

Benchmarking:

Selecting benchmarks have largely remained an art. However, Dr. John's research demonstrated the use of clustering methodology and benchmark characterization techniques to understand similarity and dissimilarity between benchmarks and to create a suite that achieves the highest coverage of the design space. Her techniques were used by SPEC, the industry standard computer performance evaluation corporation (www.spec.org) in the creation of the SPEC 2006CPU benchmark suite (See Henning's article Computer Architecture News, March 2007, pp. 119). She showed how principal component analysis (PCA) and clustering can be used to select benchmarks increasing the coverage of the workload space the suite covers. Her group's research received the best paper award at the 2006 SPEC workshop. This technique is also being used by SPEC currently for creation of their upcoming SPEC CPU benchmark suite. Her work is cited frequently; for example, her 2005 ISPASS paper on program similarity has been cited 138 times and her 2007 ISCA paper on benchmark clustering is cited 130 times.

1. A. Phansalkar, A. Joshi and L. K. John, " Analysis of Redundancy and Program Balance in SPEC CPU 2006", ISCA 2007, San Diego, June 2007, pp. 412-423 (46 accepts/204 submissions) (138 citations)
2. J H Ryoo, S. Quirem, and L. K. John, "GPGPU Benchmark Suites: How well Do They Sample the Performance Spectrum", IEEE International Conference on Parallel Processing (ICPP) 2015 (Best Paper Runner Up)

3. Aashish Phansalkar, Ajay Joshi, Lieven Eeckhout, and Lizy K. John, "Measuring Program Similarity", Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 05), April 2005, pp. 10-20. (Acceptance rate: 27 accepted/92 submissions = 29%)
4. H. Nguyen and L. John, "Exploiting SIMD Parallelism in DSP and Multimedia Algorithms Using the AltiVec Technology", Proceedings of the ACM International Conference on Supercomputing (ICS 99), Greece, June 1999, pp. 11-20. (Acceptance rate: 57 accepted/180 submissions = 32%) (103 citations)
5. Ajay Joshi, Aashish Phansalkar, Lieven Eeckhout, and Lizy K. John, "Measuring Benchmark Similarity Using Inherent Program Characteristics", **IEEE Transactions on Computers**, Vol. 55, No. 6, June 2006, pp. 769-782. (101 citations)
6. Kenneth Hoste, Aashish Phansalkar, Lieven Eeckhout, Andy Georges, Lizy K. John and Koen De Bosschere, "Performance Prediction based on Inherent Program Similarity", Proceedings of Parallel Architectures and Compilation Techniques (PACT), Sept. 2006. (100 citations)
7. R. Bhargava, L. K. John, B. L. Evans, and R. Radhakrishnan, "Evaluating MMX Technology using DSP and Multimedia Applications", Proceedings of the IEEE Symposium on Microarchitecture (MICRO-31), Dallas, Texas, Dec 1998, pp. 37-46. (Acceptance rate: 28 accepted/108 submissions = 26%) (125 citations)
8. Byeong Kil Lee and Lizy K. John, "NpBench: A Benchmark Suite for Control Plane and Data Plane Applications for Network Processors", ICCD 2003, pp. 226-233. (Acceptance rate: 61 accepted/233 submissions = 26%) (70 citations)

Architectural Enhancement:

She has conducted excellent workload characterization in fields such as multimedia and Java processing. Her Micro 98 paper on MMX has 125 citations and her 2002 IEEE Transactions paper devising the MediaBreeze architecture has 130 citations. When the industry was focusing on exploiting more parallelism in the SIMD part of the code, her workload characterization showed that the serial code on the host processor was the bottleneck. Acceleration techniques for the serial part of the code were devised in the MediaBreeze architecture. Her student who worked on the MediaBreeze architecture (Deepu Talla) is now VP at NVIDIA. Her workload characterization has continually exposed bottlenecks which were quite non-intuitive.

1. Muhammad Umar Farooq, Khubaib, and Lizy K. John Store-Load Branch (SLB) Predictor: A Compiler Assisted Branch Prediction for Data Dependent Branches The 19th IEEE International Symposium on High Performance Computer Architecture (HPCA), 2013
2. Dimitris Kaseridis, Jeffrey Stuecheli, and Lizy K. John. Minimalist Open-page: A DRAM Page-mode Scheduling Policy for the Many-core Era (Best Paper Nominee), 44th IEEE/ACM International Symposium on Microarchitecture (MICRO'44) . December 2011. (71 citations)
3. R. Radhakrishnan, N. Vijayakrishnan, L. K. John, A. Sivasubramaniam, J. Rubio, and J. Sabarinathan, "Java Runtime Systems: Characterization and Architectural Implications", **IEEE Transaction on Computers**, Feb 2001, Vol.50, No. 2, pp. 131-146. (82 citations)
4. Deepu Talla, Lizy John, and Doug Burger, "Bottlenecks in multimedia processing with SIMD style extensions and architectural enhancements", **IEEE Transactions on Computers**, Volume 52, Number 8, ISSN 0018-9, Aug 2003, pp. 1015-1031 (130 citations)
5. J. Stuecheli, D. Kaseridis, D. Daly, H. Hunter, L. K. John, "The Virtual Write Queue: Coordinating DRAM and Last-Level Cache Policies", Proceedings of the International Symposium on Computer Architecture (ISCA) 2010, pp. 72-82 (79 citations)
6. Lizy Kurian John and Eugene B. John, "A Dynamically Reconfigurable Interconnect for Array Processors", **IEEE Transactions on VLSI**, March 1998, Vol. 6, No. 1, pp. 150-157. (80 citations)
7. R. Shalem, E. John and L. K. John, "A Novel Low Power Static Energy recovery Full Adder Cell", Proceedings of the 1999 IEEE Great Lakes Symposium on VLSI, Michigan, March 1999, pp. 380-383. (193 citations)

8. D. Burger, S. Keckler, K. S. McKinley, M. Dahlin, L.K. John, C. Lin, C. R. Moore, J. Burrill, R. G. McDonald, W. Yoder and the TRIPS team, "Scaling to the End of Silicon with EDGE architectures", **IEEE Computer**, July 2004, pp. 44-55. (325 citations)

SERVICE TO PROFESSION:

ACM SIGMICRO Vice Chair, 2006-2008
ACM SIGMICRO Member at large, 2005-2008
ACM SIGMICRO Public Relations Director 2002-03, 2001-02
Committee Member, ACM Trans on Architecture and Code Optimization (TACO) Editor In Chief Search, '08-'09

Founded the IEEE International Symposium on Workload Characterization (IISWC)
Co-founded IEEE International Symposium on Performance Analysis of Systems and Software (lSPASS)

Associate Editor, IEEE Transactions on Computers, 2009 - 2014
Associate Editor, IEEE Transactions on VLSI, 2003 December-August 2007
Editorial Board, IEEE MICRO, 2005 - date
Editorial Board, International Journal on Embedded Systems, 2005-2014

SPEC Dissertation Award Committee Chair, 2016
IEEE Fellows Selection Committee (Computer Society), 2015
IEEE Fellows Selection Committee (Computer Society), 2013
DOE Panelist/Proposal reviewer, various years, 2010-2014
NSF Panelist/Proposal reviewer, various years 1997-2015
Steering Committee Member, SPEC RESEARCH, 2013-2014
Steering Committee Member, SPEC RESEARCH, 2012-2013
Steering Committee Member, SPEC RESEARCH, 2011-2012
Steering Committee Member, SPEC RESEARCH, June 2010-2011
Member, Industrial and Professional Advisory Council (IPAC), Penn State College of Engineering, 2008-2015
Member, IEEE Senior Member Selection Panel, October 2007
Member, External Advisory Board, ECE Department, UT El Paso, 2008-
Member, External Advisory Board, University of North Texas, 2008-
Steering Committee, SPEC workshops, 2005-2007
Registration Chair - ACM International Symposium on Microarchitecture, MICRO-31, Dallas, TX, Dec 1998
Travel Awards Chair, International Symposium on Parallel Architectures and Compilation techniques (PACT 2003)
Reviewer for Addison Wesley (1997)
Kluwer Academic Publishers Book Proposal Reviewer, 2001

General Chair

ACM International Conference on Performance Engineering (ICPE) 2015
IEEE International Symposium on Workload Characterization (IISWC) 2005
IEEE International Symposium on Performance Analysis of Systems and Software, ISPASS 05
IEEE Intl Workshop on Workload Characterization (WWC), 1998-2005

Steering Committee Chair

IISWC (IEEE International Symposium on Workload Characterization), 2005-2007
ISPASS (IEEE International Symposium on Performance of Software and Systems), 2008-2013

Program Committee Chair ICPP 2013 Performance Track, **ACM** ICPE 2012 Program co-Chair (SPEC side)**,** SPEC Workshop 2006, Program co-chair**,** ISPASS 2004 (IEEE International Symposium on Performance Analysis of Systems and Software), ICCD Architecture track 1999 etc.

Technical Program Committee Member, ISCA 2015, SC'15, ISCA 2012, IPSASS'12, SC '11, ICS'11, PACT 2010, PACT 2009, VEE 2008, SC'2007, HPCA 2005, HPCA 2002, MICRO TOP PICKS 2006, MICRO TOP PICKS 2009, etc

Steering Committee Member, IISWC (IEEE International Symposium on Workload Characterization), 2007-present, ISPASS (IEEE International Symposium on Performance of Software and Systems), 2001-present, Workshop on Workload Characterization (WWC) (Since inception 1998 till it became IISWC 2006)

UT Austin Service: UT Austin Financial Aid Committee Chair 2012-2013, Cockrell School Honors Committee Chair and member various years, ECE Faculty Evaluation committee, ECE faculty search committee, Computer Architecture track Ph. D Coordinator, ECE Appeals committee, various years, Circuit design program Minority Liaison 2006-2009, Computer Engineering Ph. D coordinator 2007-2014

Local Schools Service: Technology Club Organizer, Spelling Coach, Science Fair Judge, Speaker, etc.

GRANTS AND CONTRACTS: (Co-principal investigators (if any), title of grant, sponsoring agency, total dollar value, beginning and ending dates)

Co-Investigators	Title	Agency	Grant Total	Grant Period

w/Gerstlauer	Power-Aware System Compilation	Intel	100,000	6/15-5/16
Sole	A Methdology to Identify Application Memory Access Patterns for Efficien Hierarchical Memory Subsystem	Oracle Corporation	$97,283	01/16-01/18
w/Gerstlauer	Big Data Workloads, A Computer Architect's perspective	Samsung GRO	$99,985	09/15-08/16
w/Gerstlauer	Scalable Network/System Co-Simulation For Power and Performance Aware Network of Systems Design	Samsung GRO	$99,985	6/14-5/15 6/14-5/15 1/14-
Sole	Big Data Workload Energy Characterization	Huawei	$110,000	12/16
Sole	A Methodology to Generate Miniature Proxies for Database workloads	Oracle	$60,000	9/13-8/16
Sole	Workload characterization for Big Data	SRC	$240,000	9/13-8/15
w/Biros, Gerstlauer, vandeGeijn	XPS: Algorithms and Architectures for Multiresolution Applications	NSF	$749,801 ($224K-my share)	10/13-9/15
w/Gerstlauer	Power-Aware System Compilation	Intel	200,000	6/13-5/15
Sole	Decomposition of Large Data Analytics into Hierarchical Models	AMD	50,000	6/13-5/14
Sole	A Methodology to Identify Application Memory Access Patterns for Efficient Hierarchical Caching	Oracle	60,000	09/12-08/15
w/Janapa Reddi	SHF: Sustainable and Reliable Multicore and Many-Core Computing via Cross-Layer Solutions	NSF	300,000	05/12-04/15
w/Gerstlauer	Multi-dimensional Modeling, Design and Exploration of Multi-core SoCs,	SRC	345,000	04/12-03/13
None	Automatic Generation of Multicore Proxy Workloads and Stressmarks	AMD	50,000	05/11-04/12
None	Multicore Stressmarks	AMD	50,000	09/11-08/14
None	SHF: Small: Workload Characterization and Benchmark Synthesis for Emerging Computing Systems	NSF	425,000	08/10-08/11
None	Stress-testing Multicore Processors for Worst-Case Power Consumption and Voltage Emergencies	AMD	50,000	
Dan Tamir, Apan Qasem	Power Consumption Based Multicore Task Scheduling and Load Balancing	SRC	360,000 (my share: 175,500)	04/11-03/14
None	Intel Corporation Product Donation for EE316 Logic Design Lab, June, 2009,	Intel	34,361	2009 June
None	Performance Cloning for Dissemination of Proprietary Applications to Hardware Vendors	Lockheed Martin	100,000	2008-2009
None	Benchmark Synthesis for Performance and Power Modeling	Sun Microsystems	45,000	2008-2009
None	IBM Faculty Award	IBM	15,000	2008-2009
R. Figueiredo, etc	Collaborative Research Archer: Seeding a Community Based computing Infrastructure for Computer Architecture Research and Education	NSF	(my share 67,631)	2008-
None	Computer Architecture Research	AMD	8,000	Dec 07-Dec 08
None	Intel Equipment Grant for research	Intel	35,056	Sep 2008

Tao Li	Automatic Benchmark Synthesis for Validation of Performance and Power Models of High Performance Processors	SRC	330,000 (my share: 165,000)	04/08-03/11
None	Simplifying Performance Evaluation using Workload Characterization	NSF	300,000	09/07-08/11
None	Faculty Partnership Award	IBM	$25,000	06/07
None	Computer Architecture Research	AMD	$5000	11/06
None	CAS Award – Faculty Partnership Award	IBM	$7,500	06/06
None	Computer Architecture Research	AMD	$5000	11/05
None	Java Accelerators	Samsung	$128,000	2/05-8/06
None	CAS Award	IBM	$25,000	6/05
None	Statistical Techniques for Computer Performance Evaluation	NSF	$200,000	2004-2008
None	Computer Architecture Research	AMD	$5000	2/05
None	Performance Evaluation Research	IBM	$500	12/04
None	CAS project- Statistical Techniques in Performance Evaluation and Benchmarking	IBM	$25,000	7/04
None	Computer Architecture Research	Hewlett Packard	$800	6/04
None	Equipment Grant	Intel	$42,000 (approx.)	Spring 2004
None	Performance Impact of Emerging Workloads on Intel Processors	Intel	$35,000	March 2004
None	Research in Computer Architecture and Workload Characterization	AMD	$3,000	Dec 2003
None	IBM Faculty Partnership Award Project: Developing a Methodology for Predicting Characteristics of Future/Emerging Workloads	IBM	$25,000	June 2003
None	Performance Impact of Emerging Workloads on Intel Processors	Intel	$35,000	May 2003
	IBM SUR grant	IBM	$60,000 (approx.)	Fall 2002
None	IBM Faculty Partnership Award- Developing a Methodology for Predicting Characteristics of Future/Emerging Workloads	IBM	$25,000	June 2002
None	Equipment Support- Performance Impact of Emerging Workloads on Intel Processors	Intel	$10,000	Summer 2002
None	Research in Computer Architecture and Workload Characterization	AMD	$5,000	May 2002
None	Performance Impact of Emerging Workloads on Intel Processors	Intel	$35,000	March 2002
None	Intel Equipment (8-way server + 5 workstations)	Intel	$65,000 (approx.)	Spring 2002
None	Development and Characterization of Control-Plane Network Workloads	Motorola	$50,000	Jan 2002
None	Computer Architecture Research	AMD	$5,000	Dec 2001
	IBM SUR Grant	IBM	$100,00 (approx.)	Fall 2001
None	Designing Microprocessors and Computer Systems for Emerging Workloads	NSF	$265,000	2001-2004
	Intel Equipment (10 workstations)	Intel	$40,000 (approx.)	2000-2001
None	IBM Faculty Partnership Award- Effectiveness of Out of Order Microarchitectural techniques for web server workloads	IBM	$30,000	May 2001
None	UT Research Internship Program	Univ. of TX, at Austin	$15,500	2001-2002

	Computer Architecture Seminar Series	AMD	$15,000	
None	Understanding and Optimizing e-Business workloads and the underlying infrastructure	Tivoli	$30,000	Aug 2000
None	IBM Center for Advanced Studies Partnership Award- Effectiveness of Out of Order Microarchitectural Techniques for web server workloads	IBM	$25,000	March 2000
	Workshop on Workload Characterization 2000	AMD	$2,500	2000
None	Career Award- Improving the Access-Execute Balance and Concurrency in High Performance Processors	NSF	$315,000	1996-2000
None	UT Co-op Book Subvention Grant	Univ. of TX, at Austin	$2,500	Aug 1999
None	DELL-LARIAT grant- Characterization of Multimedia Application and Analysis of their Performance Impact	Dell	$32,127	July 1999
None	Workshop on Workload Characterization	Intel	$4,000	July 1999
None	Computer hardware grant- Characterization of Multimedia Workloads and Analysis of their Performance Impact	Intel	$4,181	July 1999
None	Software donation- Web Server Characterization Studies on the Pentium Platforms	Microsoft	$3,814	Jan 1999
None	Web Server Characterization Studies on the Pentium Platforms	Intel	$15,320	Dec 1998
None	UT research Internship Program	Univ. of TX, at Austin	$15,000	1998-1999
None	UT Endowed Lecturer Program	Univ. of TX, at Austin	$1,100	Spring 1998
None	Summer Research Assignment Award	Univ. of TX, at Austin	$11,000	Summer 1997
None	Junior faculty Enhancement Award	Oak Ridge Associated Universities	$5,000	1996-1997
None	Matching Award to Oak Ridge Junior Faculty Enhancement Award	UT Austin	$5,000	Fall 1996
None	Matching Award to NSF CAREER Equipment	UT Austin	$10,000	Fall 1996
None	Startup Grant	Univ. of TX, at Austin	$55,000	Fall 1996
None	Microprocessor Performance Evaluation System - Advanced Micro Devices (proprietary equipment given for UT research. Dollar equivalent not specified by AMD)	AMD	Not Specified	Dec 1997
S. Keckler, D. Burger, L. Alvisi, M.D. Dahlin, C. Lin, C.R. Moore, K. McKinley, and H. Vin	"TRIPS: The Tera-op Reliable Intelligently adaptive Processing System Implementation for Polymorphous Computing Architectures (PCA),"	Defense Advanced Research Projects Agency	$7,617,912 $100,000 (approx./ my share)	2003-2005
Steve Keckler, D. Burger, L. Alvisi, M.D. Dahlin, C. Lin, K. McKinley, and H. Vin	TRIPS: The Tera-op Reliable Intelligently adaptive Processing System	Defense Advanced Research Projects Agency	$3,027,48 $400,000 (approx./ my share)	6/01-5/03

Prof. E. Swartzlander and Prof. E. John	ATP Grant- High Performance MultiMedia Processors Principal Investigator	State of Texas Advanced Technology Program	$157,800 $72,806 (my share.)	1/00-12/01
Prof. C. Chase	Impact of Contemporary Programming Paradigms and Workloads Principal Investigator	NSF	$356,314 $256,314 (my share)	1998-2001
Prof. E. Swartzlander	ATP Grant- High Performance Digital Signal Processors Principal Investigator	State of Texas Advanced Technology Program	$134,640 80,784 (my share)	1/98-12/99
Prof. Yale Patt	Equipment Donation	Intel	$136,640	Nov 1999
Prof. Yale Patt	Software Donation	Microsoft	$61,039	Sept 1999
Prof. Evans	TMS320C62x Development Tools	Texas Instruments	Not Specified	1998
Prof. J. C. Browne of Computer Science, co-PIs: L. John, Prof. C. Chase and Prof. P. Teller at the University of Texas at El Paso	IBM- SUR Grant- End-to-End Measurement, Modeling and Simulation of Parallel/Distributed Computer Systems	IBM	$100,000	Oct 1997
Dr. Pete Maurer and Dr. N. Ranganathan of the University of South Florida, Tampa, Florida	NSF CISE Infrastructure Grant * This was an award to Univ. of S. Florida while Lizy John was faculty there. This grant was not transferred to UT, however, I continued to participate in the project until 1998	NSF	$373,524 $100,00 (approx./ my share)	1995-1998
None	FPGA lab hardware and software donation (while faculty at University of Southern Florida)	Xilinx	$40,000 (approx.)	1994-1995
None	International Faculty Travel grant	University of South Florida	$1,500	1995
None	Office of Sponsored research	University of South Florida	$5,500 (approx.)	1994
None	Startup grant	University of South Florida	$10,000	1993

PH.D. SUPERVISIONS COMPLETED: *(Name, *title, year, major dept, name of institution)*
(May want to add another column for titles.)

M. Faisal Iqbal	Aug 2013	Multicore Communication Processors	ECE	UT
Youngtaek Kim	May 2013	Stressmarks for Voltage Emergencies (Intel)	ECE	UT
M. Umar Farooq	Dec 2013	Value Based Branch Prediction (ARM)	ECE	UT
Arun Arvind Nair	May 2012	Modeling of Soft Errors (AMD)	ECE	UT
Karthik Ganesan	Dec 2011	Automatic Generation of Synthetic Workloads for Multicore Systems (Oracle)	ECE	UT
Jian Chen	May 2011	Resource Management for Efficient Single-ISA Heterogeneous Computing (Intel)	ECE	UT
Ciji Isen	May 2011	The Use of Memory State Knowledge to Improve Computer Memory System Organization (AMD)	ECE	UT
Jeff Stuecheli	May 2011	Coordinated Memory Scheduling (IBM)	ECE	UT
Dimitris Kaseridis	May 2011	Memory-subsystem Resource Management for the Many-core Era (ARM Corporation)	ECE	UT
Lloyd Bircher	Dec 2010	Predictive Power Management for Multi-Core Processors (AMD)		
Ajay Joshi	Dec 2007	Constructing Adaptable and Scalable Synthetic Benchmarks for Microprocessor Performance Evaluation (ARM Corporation)	ECE	UT
Aashish Phansalkar	May 2006	Similarity Analysis and Benchmark Subsetting (Employed at Intel)	ECE	UT
Rob Bell Jr.	Dec 2005	Automatic Workload Synthesis for Early Design Studies and Performance Model Validation (Employed at IBM)	ECE	UT
Byeong Kil Lee	Aug 2005	Network Processor Design: Benchmarks and Architectural Alternatives (Employed at Texas Instruments)	ECE	UT
Shiwen Hu	Dec 2005	Effective Adaptive Computing Environment Management via Dynamic Optimization, (Employed at Freescale)	ECE	UT
Yue Luo	Aug 2005	Improving Sampled Microprocessor Simulation (Microsoft)	ECE	UT
Madhavi Valluri	May 2005	A Hybrid-Scheduling Approach for Energy-Efficient Superscalar Processors (Employed at IBM)	ECE	UT
Juan Rubio	Aug 2004	Exploring the Potential of a Hierarchical Computing Model for a Commercial Server (Employed at IBM Austin Research Lab)	ECE	UT
Tao Li	Aug 2004	OS-aware Architecture for Improving Microprocessor Performance and Energy Efficiency, (Assistant Professor University of Florida)	ECE	UT
Ravi Bhargava	Aug 2003	Instruction History Management for High-Performance Microprocessors (Employed at AMD)	ECE	UT
Deepu Talla	Aug 2001	Architectural Techniques to Accelerate Multimedia Applications on General-Purpose Processors, August 2001 (Employed at Texas Instruments)	ECE	UT
Ramesh Radhakrishnan	Aug 2000	Microarchitectural Techniques to Enable Efficient Java Execution (Employed at Dell)	ECE	UT

M.S. SUPERVISIONS COMPLETED: *(Name, year, major department, name of institution (May want to add another column for titles.)*

Alex Schulyak	Dec 2016	Electrical and Computer Engineering	Univ of Texas at Austin
Jee Ho Ryoo	May 2014	Electrical and Computer Engineering	Univ of Texas at Austin
Darshan Gandhi	May 2014	Electrical and Computer Engineering	Univ of Texas at Austin
Abhishek Tondon	Dec 2013	Electrical and Computer Engineering	Univ of Texas at Austin
Don Owen	May 2013	Electrical and Computer Engineering	Univ of Texas at Austin
Ankita Garg	May 2013	Computer Sciences	Univ. of Texas at Austin
Bhargavi Narayanasetty	May 2011	Electrical and Computer Engineering	Univ. of Texas at Austin
Chaitanya Nayak	May 2011	Electrical and Computer Engineering	Univ. of Texas at Austin
Rengarajan	2010	Electrical and Computer Engineering	Univ. of Texas at Austin
Karthik Ganesan	Dec 2008	Electrical and Computer Engineering	Univ. of Texas at Austin
Rajiv Bhatia	Aug 2008	Electrical and Computer Engineering	Univ. of Texas at Austin
Justin Friesenhahn	Dec 2007	Electrical and Computer Engineering	Univ. of Texas at Austin
Jason Matalka	Aug 2006	Electrical and Computer Engineering	Univ. of Texas at Austin
Kathryn Stacer	May 2006	Electrical and Computer Engineering	Univ. of Texas at Austin
Lloyd Bircher	May 2006	Electrical and Computer Engineering	Univ. of Texas at Austin
Diego Vila	May 2006	Electrical and Computer Engineering	Univ. of Texas at Austin
Brijesh Patel	2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Jenson Lam	2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Brian Gaide	2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Jignesh Gondalia	2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Saket Kumar	May 2004	Electrical and Computer Engineering	Univ. of Texas at Austin
Michael Arunkumar	Dec 2003	Electrical and Computer Engineering	Univ. of Texas at Austin
Michael Lance Karm	Dec 2003	Electrical and Computer Engineering	Univ. of Texas at Austin
Patrick James Peters	Dec 2003	Electrical and Computer Engineering	Univ. of Texas at Austin
Mike Clark	May 2003	Electrical and Computer Engineering	Univ. of Texas at Austin
Anand Sunder Rajan	2003	Electrical and Computer Engineering	Univ. of Texas at Austin
James Yang	2002	Electrical and Computer Engineering	Univ. of Texas at Austin
Ravi Bhargava	Aug 2000	Electrical and Computer Engineering	Univ. of Texas at Austin
Vikram Godbole	May 2000	Electrical and Computer Engineering	Univ. of Texas at Austin
Sanjeev Ghai	May 2000	Electrical and Computer Engineering	Univ. of Texas at Austin
Srikanth Kannan	May 2000	Electrical and Computer Engineering	Univ. of Texas at Austin
Jyotsna Sabarinathan	Dec 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Jody Joyner	Dec 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Juan Rubio	May 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Poorva Murarka	May 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Purnima Vasudevan	May 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Roy Shalem	Aug 1998	Electrical and Computer Engineering	Univ. of Texas at Austin
Dachih-Tang	Aug 1998	Electrical and Computer Engineering	Univ. of Texas at Austin
Yin Teh	Dec 1997	Electrical and Computer Engineering	Univ. of Texas at Austin
Ramesh Radhakrishnan	Aug 1997	Computer Science and Engineering	Univ. of South Florida
Vijay Kammila	1996	Computer Science and Engineering	Univ. of South Florida
Vinod Reddy	Dec 1996	Computer Science and Engineering	Univ. of South Florida
Amudha Muthiah	1996	Computer Science and Engineering	Univ. of South Florida
Raghuveer Reddy	1995	Computer Science and Engineering	Univ. of South Florida