THE UNIVERSITY OF TEXAS AT AUSTIN
College of Engineering
Standard Resume

FULL NAME: Lizy Kurian John **TITLE:** Cullen Trust for Higher Education

Endowed Professor

DEPARTMENT: Electrical and Computer Engineering

CITIZENSHIP: U.S.

EDUCATION: *(Institution, major, degree, dates)*

The Pennsylvania State University	Computer Engineering	PhD	August 1993
The University of Texas at El Paso	Computer Engineering	MS	December 1989
The University of Kerala, India	Electronics and Communication	BS	August 1984

PROFESSIONAL REGISTRATION:

Texas Professional Engineer (PE) License, Since 2001

CURRENT AND PREVIOUS ACADEMIC POSITIONS: *(Institution, rank(s), beginning and ending dates for each rank)*

The University of Texas at Austin	Cullen Trust for Higher Education Professor No. 3	Fall 2018 - present
The University of Texas at Austin	B. N. Gafford Professor in Electrical Engineering	Fall 2009 - Summer 2018
The University of Texas at Austin	Professor and Centennial Teaching Fellow	Fall 2007-Summer 2009
The University of Texas at Austin	Associate Professor and Centennial Teaching Fellow	Fall 2001-Summer 2007
The University of Texas at Austin	Assistant Professor	Fall 1996-Summer 2001
The University of South Florida, Tampa	Assistant Professor	Fall 1993-Summer 1996

(The order of the categories below this point is optional)

OTHER PROFESSIONAL EXPERIENCE: *(Name of company, position, beginning and ending dates)*

Penn State, Electrical Engineering Dept	Research Assistant	8/90 - 8/93
Penn State, Electrical Engineering Dept	Teaching Assistant	1/90 - 5/90
University of Texas at El Paso, Electrical Engineering Dept	Teaching Assistant	8/88 -12/89
Indian Space Research Organization, Trivandrum, India	Scientist/Engineer	8/84 - 8/88

***CONSULTING:** *(Names of companies, beginning and ending dates)*

Texas Digital and MultiMedia Systems	May 2008-date

EcoViv Inc.	June 2008-date
SmoothStone	June 2008-June 2011

HONORS AND AWARDS: *(Include dates)*

- Jacome Prize for Outstanding Dissertation won by student Reena Panda's dissertation in UT ECE, May 2018
- Graduate Fellowship for Ph. D Student 2018-2019, UT Austin
- **Best Paper Award,** DAC 2016 (53rd DAC) (2 awards out of nearly 700 submissions), June 2016
- Best Paper Nominee, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2017
- Graduate Fellowship for Ph. D Student 2017-2018, UT Austin
- **Best Paper Award**, IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), 2015
- SPEC Dissertation Award Honorable Mention, won by student Karthik Ganesan (2012)
- **Best Paper Nominee**, Paper with student Karthik Ganesan, Supercomputing Conference (SC) 2011 (1 of 4 nominees), Nov 2011
- **Best Paper Nominee**, Paper with students Jeff Stuecheli and Dimitris Kaseridis, IEEE/ACM MICRO conference, 2011 (1 of 4 nominees), December 2011
- **Best paper award nominee**, (1 of 4 nominees), IEEE High Performance Computer Architecture (HPCA) 2010
- Outstanding Engineering Alumnus of the Pennsylvania State University, 2011
- **IEEE Fellow, Class of 2009**
- B. N. Gafford Professor in Electrical Engineering, September 2009-present
- Graduate Fellowship for Ph. D Student 2010-2011, UT Austin
- **Best Paper Award**, IEEE International Conference on Parallel Processing (ICPP) 2009
- SPEC Benchmark workshop 2006, The K. Dixit award for best paper won by student Ajay Joshi
- TEXAS EXES Teaching Award, Feb 2004
- Engineering Foundation Faculty Award, College of Engineering, UT Austin, Fall 2001
- UT Austin Engineering Foundation Centennial Teaching Fellowship in Electrical Engineering No. 2, Sept 2000- present
- Halliburton, Brown and Root Engineering Foundation Young Faculty Award, College of Engineering, UT Austin, Fall 1999
- IBM Austin Center for Advanced Studies (CAS) or University Partnership Award- 2001-2008
- Best Paper Award, Computer Track, IEEE International Performance Conference on Computing and Communication, Feb 1999
- Elevated to Senior Membership of IEEE (Electrical and Electronics Engineers), 1997
- National Science Foundation CAREER Award, 1996-2001
- $1000 award for being Advisor of the student who won the University Level George H. Mitchell Undergraduate Student Achievement Award, April 2002 (Student Pattabi Seshadri won the $2000 award)
- Oak Ridge Junior Faculty Enhancement Award, 1996-1997
- Outstanding Young Investigator, College of Engineering, University of South Florida, 1995-1996
- Outstanding Undergraduate Teaching Award, University of South Florida, Tampa, 1994-1995.
- Best Paper Award, ASEE Gulf Southwest Conference, March 1998
- Graduate School Fellowship, awarded by the Graduate School, The Pennsylvania State University, 1991-1992
- George Krutilek Fellowship awarded by the Graduate School, The University of Texas at El Paso, 1988-1989
- Graduate School Marshal for the December 1989 commencement at The University of Texas at El Paso
- Schellenger Research Scholarship awarded by the Electrical Engineering Department, Univ. of Texas El Paso, Summer 1989
- Selected by NCERT (National Council of Educational Research and Training), New Delhi, Govt. of India, on the basis of a National Examination, for the National Talent Search Scholarship for 1977-1984
- **3rd Rank in Kerala University** B.Sc. Engineering Degree Exam, 1984

- **Ist rank** (Ist out of 70,462 students) in the Kerala University Pre Degree Exam, India, 1979
- **2nd rank** in the state of Kerala (2nd out of 275,554 students) in the Kerala State Higher Secondary School Exam (SSLC), India, 1977

***MEMBERSHIPS IN PROFESSIONAL AND HONORARY SOCIETIES:**

- IEEE Fellow, Class of 2009
- Senior Member, IEEE, 1997- 2008
- Member, IEEE Computer Society, 1989-present
- Member, ACM (Association of Computing Machinery), ACM - SIGARCH, since 1990
- Member ACM SIGMICRO since 2001
- Member Eta Kappa Nu (Class of 1989), Tau Beta Pi (Class of 1989), Phi Kappa Phi (Class of 1992)

PROFESSIONAL SOCIETY AND MAJOR GOVERNMENTAL COMMITTEES: *(Include dates)*

- **Editor-In-Chief-Elect,** IEEE MICRO, 2019-2021
- **Editorial Board,** IEEE MICRO, 2005 - 2018
- **Associate Editor**, IEEE Computer Architecture Letters, 2016 – 2018
- **Associate Editor**, IEEE Transactions on Computers, 2009 – 2014
- **Associate Editor**, IEEE Transactions on Sustainable Computing, 2016-
- **Associate Editor**, ACM Transactions on Architecture and Code Optimization (TACO), 2016-2018
- **Search Committee Member**, ACM Transactions on Architecture and Code Optimization (TACO) Editor In Chief Search , 2008-2009
- **Associate Editor,** IEEE Transactions on VLSI, 2003 December-August 2007
- **Editorial Board**, International Journal on Embedded Systems, 2005-2014
- **Member**, National Science Foundation Workshop on Computer Performance Evaluation Techniques, December 2001, Austin TX
- **Member**, National Science Foundation Proposal Review Panel, 2017, 2000, 1998, 1997
- **Member,** DOE Office of Science Proposal Review Panel, May 2010, 2014

UNIVERSITY COMMITTEE ASSIGNMENTS: *(Include major departmental, college, and university assignments, including administrative assignments, with beginning and ending dates)*

University-	**Information Technology Committee Chair-Elect**	**2018-2019**
	Information Technology Committee	2017-2018
	Information Technology Committee	2016-2017
	University Financial Aid Committee co-chair	2012-2013
	University Financial Aid Committee Member	2011-2012
	Circuit Design Masters Program Minority Liaison	2007 -
	Circuit Design Masters Program Minority Liaison	2006
	Circuit Design Master Program Minority Liaison	2005
College-	Cockrell School of Engineering Honors Committee Member	2014-2015
	Cockrell School of Engineering, Honors Committee Chair	**2010-2014**
	College of Engineering Honors Committee, Member	2005-2008
	College of Engineering Hocott Awards Committee	2006, 2007, 2008
	College of Engineering Equal Opportunity in Engineering Committee	2005-08
	College of Engineering Honors Committee	2004-05
	College of Engineering Equal Opportunity in Engineering Committee	2004-05
	College of Engineering Honors Committee	2003-04
	College of Engineering Equal Opportunity in Engineering Committee	2003-04
	College of Engineering Honors Students Committee	2002-03

	College of Engineering Honors Students Committee, chaired by Prof. Bill Rossen	1997-98, 1998-99, 1999-2000, 2000-01, 2001-02
Departmental-	ECE Junior Faculty Recruiting Committee (Chair: Dimakis)	2018-2019
	ECE Faculty Evaluation Committee	2017-2018
	Senior Faculty Search Committee (Chair: Shakkottai)	2017-2018
	ACSES Track Ph. D Coordinator	2013-2018
	ECE Faculty Evaluation Committee	2016-2017
	Faculty Search Committee (Chair Ed Yu)	2016-2017
	Faculty Search Committee (Chair Ed Yu)	2015-2016
	ECE Faculty Evaluation Committee	2014-2015
	ECE Faculty Evaluation Committee	2013-2014
	ECE Faculty Evaluation Committee	2012-2013
	Faculty Search Committee (Chair Ed Yu)	2012-2013
	ECE Faculty Evaluation Committee	2012-2013
	ECE Faculty Expectations Committee	2012-2013
	Computer Engineering Ph. D Coordinator	2011-2012
	Computer Architecture and Embedded Processing Track Ph. D Coordinator	2011-2012
	Faculty Search Committee (Chair de Veciana)	2010-2011
	Faculty Search Committee (Chair Al Bovik)	2011-2012
	Computer Architecture and Embedded Processing Track Ph. D Coordinator	2011-2012
	Computer Engineering Ph. D Coordinator	2010-2011
	Computer Engineering Ph. D Coordinator	2011
	ECE Faculty Evaluation Committee	2011-2012
	ECE Faculty Expectations Committee	2009-2010
	Computer Engineering Ph. D Coordinator	2008-2009
	Computer Engineering Ph. D Coordinator	2007-2008
	Computer Engineering Ph. D Coordinator Curriculum Reform Subcommittee	2008
	ECE ABET Committee	2003-2007
	ECE Appeals Committee	1999-2003
	ECE Awards Committee	2001-04
	ECE Hiring Subcommittee, Computer Architecture Position	2001-06
	Department of ECE, Appeals Committee	April 2000-Mar 2001, April 2001-March 2002
	Department of ECE, Computer Engineering Faculty Committee	September 1996-present
	Department of ECE Subcommittee on Computer Engineering Graduate Admissions	1997-2006
	Department of ECE, Graduate Studies Committee,	September 1996-present
	Department of ECE, Undergraduate Software Curriculum Committee	Sept 1996-2001
	Department of ECE, Undergraduate Digital Systems Curriculum Committee	Sept 1996-2001

***COMMUNITY ACTIVITIES:**

- SPEC Dissertation Award Committee Chair, 2016
- IEEE Fellows Selection Committee (Computer Society), 2018
- IEEE Fellows Selection Committee (Computer Society), 2017
- IEEE Fellows Selection Committee (Computer Society), 2015

- IEEE Fellows Selection Committee (Computer Society), 2013
- DOE Panelist, 2014
- NSF Panelist, 2013, 2017
- Steering Committee Member, SPEC RESEARCH, 2013-2014
- Steering Committee Member, SPEC RESEARCH, 2012-2013
- Steering Committee Member, SPEC RESEARCH, 2011-2012
- Steering Committee Member, SPEC RESEARCH, June 2010-2011

Other Committees/Positions:

- Member, Industrial and Professional Advisory Council (IPAC), Penn State College of Engineering, 2008-2009, 2009-2010, 2010-2011, 2011-
- Member, IEEE Senior Member Selection Panel, October 2007
- Member, External Advisory Board, ECE Department, UT El Paso, 2008-2012
- Member, External Advisory Board, University of North Texas, 2008-2012
- ACM SIGMICRO Vice Chair, 2006-2008
- ACM SIGMICRO Member at large, 2005-2008
- Steering Committee, SPEC workshops, 2005-date
- Steering Committee, IISWC, 2005-present
- Steering Committee, ISPASS, 2000-present
- ACM SIGMICRO Public Relations Director 2002-03, 2001-02
- Travel Awards Chair, IEEE International Symposium on Parallel Architectures and Compilation techniques (PACT 2003)
- Tutorials/Workshop Chair, IEEE International Symposium on Performance Analysis of Systems and Software, ISPASS, March 2003
- 2000 IEEE International Conference on Computer Design, Special Sessions Chair
- Finance Chair, IEEE Workshop on Workload Characterization, 1998-2004
- Finance Chair, IEEE International Performance Conference on Computing and Communication, (IPCCC 2000)
- Panel Chair, IEEE International Performance Conference on Computing and Communication, Feb 1999
- Registration Chair - IEEE International Symposium on Microarchitecture, MICRO-31, Dallas, TX, Dec 1998

Other Workshops Organized:

1. 1st Workshop on Integrating Design and Design Automation into Undergraduate Computer Science and Engineering Curriculum.
   For: University Faculty from around the country.
   Partially funded by: The National Science Foundation
   August 5-8, 1996 Tampa, Florida, 33620.

2. 2nd Workshop on Integrating Design and Design Automation into Undergraduate Computer Science and Engineering Curriculum.
   Partially funded by: National Science Foundation
   August 4-7, 1997 Tampa, Florida, 33620.

Workshop Sessions/Seminars/Tutorials Organized:

1. Workshop Session on High Performance Processors organized at: Workshop title: IEEE Computer Society 1996 Annual Workshop on VLSI
   Held: Nov. 3-6, 1996
   Location: Clearwater, Florida

2. Half-day Tutorial Presentation:

At the Workshop of Microelectronic Systems Education, July 1997, Arlington, Virginia. Tutorial Topic: Rapid Prototyping using FPGAs, July 23, 1997

3. Half-day Seminar presented:
In the AUSTIN INNOVATION SERIES, Aug 27, 1997 at IBM, Austin
Topic: Improving the Memory Access Performance of Programs

Steering Committee Chair

- IISWC (IEEE International Symposium on Workload Characterization), 2005-2007
- ISPASS (IEEE International Symposium on Performance of Software and Systems), 2008-2013

Steering Committee member

- IISWC (IEEE International Symposium on Workload Characterization), 2007-present
- ISPASS (IEEE International Symposium on Performance of Software and Systems), 2001-present
- WWC (Since inception 1998 till it became IISWC 2006)

General Chair

- ACM International Conference on Performance Engineering (ICPE) 2015
- IEEE International Symposium on Workload Characterization (IISWC) 2005
- IEEE International Symposium on Performance Analysis of Systems and Software, ISPASS 05
- IEEE Intl Workshop on Workload Characterization (WWC), 1998-2005

Program Chair

- IEEE International Conference on Parallel Processing (ICPP) 2013 Performance Track Chair
- International Workshop on Performance Analysis of Workload Optimized Systems (FastPath) 2014
- International Workshop on Performance Analysis of Workload Optimized Systems, FastPath 2013
- ACM International Conference on Performance Engineering (ICPE) 2012 Program co-Chair
- SPEC Workshop 2006, Program co-chair
- ISPASS 2004 (IEEE International Symposium on Performance Analysis of Systems and Software)
- ICCD 1999 Architecture Track Program co-chair (IEEE International Conference on Computer Design)
- ISPASS 2000 Workload Characterization Track (IEEE International Symposium on Performance of Software and Systems)
- WWC (Workshop on Workload Characterization), 1998-2004
- ODES 2003-2005 (Optimizations for DSP and Embedded Systems Workshop), (held in conjunction with the CGO symposium) (co-chair)

Program Committee Member

1. IEEE High Performance Computer Architecture Symposium (HPCA) 2018
2. IEEE International Symposium on Workload Characterization (IISWC) 2018
3. IEEE International Parallel and Distributed Symposium (IPDPS) 2018
4. ACM/IEEE International Symposium on Computer Architecture (ISCA) 2017
5. IEEE High Performance Computer Architecture Symposium (HPCA) 2017
6. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2017
7. IEEE International Parallel and Distributed Symposium (IPDPS) 2017
8. ACM International Conference on Performance Engineering ICPE 2016
9. IEEE Workshop on Emerging Parallel and Distributed Runtime Systems and Middleware (IPDRM), 2016
10. ACM/IEEE International Symposium on Computer Architecture (ISCA) 2015
11. ACM Supercomputing, SC'15, Performance Track, 2015
12. International Workshop on High-Performance Big Data Computing (HPBDC) 2015
13. IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing, (CCGrid) 2014
14. ACM/IEEE International Symposium on Computer Architecture (ISCA) 2012

15. IEEE High Performance Computer Architecture (HPCA) Symposium 2012
16. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2012
17. Network and Parallel Computing (NPC) 2011
18. Supercomputing 2011 (Performance track)
19. ICS (International Conference on Supercomputing), 2011
20. IEEE Conference on Parallel Architectures and Compilation techniques (PACT) 2010
21. SPEC WOSP/SIPEW 2010
22. IEEE MICRO TOP PICKS 2009
23. IEEE International Conference on Computer Design (ICCD) 2009
24. SPEC Workshop 2009
25. Virtual Execution Environments (VEE) 2008
26. IEEE Parallel Architectures and Compilation techniques (PACT) 2009
27. IEEE International Parallel and Distributed Processing Symposium, 2009
28. SPEC Workshop 2008
29. IEEE International Conference on Computer Design (ICCD) 2008
30. 2007 Supercomputing Conference, Performance Track
31. IEEE MICRO TOP PICKS 2006
32. IEEE Symp on High Performance Computer Architecture (HPCA 2005)
33. IEEE-Symp on High Performance Computer Architecture (HPCA 2002)
34. Parallel Architectures and Compilation techniques (PACT 2003)
35. IEEE-International Symposium on Microarchitecture (MICRO-33), 2000
36. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2001)
37. IEEE International Performance Conference on Computing and Communication (IPCCC 2000)
38. IEEE International Conference on Computer Design, Architecture Track (ICCD 1999)
39. IEEE International Performance Conference on Computing and Communication (IPCCC 1999)
40. 1998 IEEE International Conference on Computer Design (ICCD), Architecture Track
41. International Performance and Dependability Symposium (IPDS), held along with DSN 2002
42. North Atlantic Test Symposium, 1997
43. Workshop on Workload Characterization (1998-2004)
44. MoBS workshop 2005 (held with ISCA)
45. Value Prediction Workshop, 2004
46. MRE 2004 (Managed RunTime Environment), 2003 (held with CGO)
47. INTERACT-6, Workshop on Interaction between Architectures and Compilers, in conjunction with IEEE-International Symposium on High Performance Computer Architecture (HPCA-8), 2002
48. Workshop on Hardware Support for Objects and Microarchitectures for Java (in conjunction with IEEE International Conference on Computer Design 2001)
49. Workshop on Decoupled Access Execute Architectures (MEDEA) in conjunction with PACT2001
50. Workshop on Hardware Support for Objects and Microarchitectures for Java (in conjunction with IEEE International Conference on Computer Design ICCD 2000)
51. Workshop on Decoupled Access Execute Architectures (in conjunction with PACT 2000)
52. Workshop on Media Processors and Digital Signal Processors, Nov 1999 (in conjunction with 32nd IEEE International Symposium on Microarchitecture Micro-32)
53. Workshop on Hardware Support for Objects and Microarchitectures for Java (in conjunction with IEEE International Conference on Computer Design 1999)

External Review Committee (ERC) Member

1. ACM International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2017
2. IEEE High Performance Computer Architecture Symposium, HPCA 2017
3. ACM/IEEE International Symposium on Microarchitecture (Micro) 2016
4. IEEE High Performance Computer Architecture Symposium, HPCA 2016
5. ACM/IEEE International Symposium on Microarchitecture (Micro) 2015
6. IEEE High Performance Computer Architecture Symposium, HPCA 2015

Technical Reviewer:

Technical reviewer for several journals, conferences, and workshops, various years, including but not limited to

HPCA, ISCA, ASPLOS, MICRO, IEEE Micro Top Picks
ACM TACO
ACM TOMACS
IEEE Transactions on Computers
IEEE Transactions on Parallel and Distributed Systems
The Computer Journal
The Journal of VLSI
Microprocessors and Microsystems
IEE Journal of Computers and Digital Techniques
IEEE Computer
IEEE Micro Magazine
IEEE Concurrency
IEEE/ACM International Symposium on Computer Architecture (ISCA)
IEEE Intl High Performance Computer Architecture Symposium (HPCA)
IEEE International Symposium on Microarchitecture (MICRO)
PACT (Parallel Architectures and Compilation Techniques) Conf., 2001
IEEE Workshop on Hardware Support for Objects and Microarchitectures for Java (in conjunction with IEEE International Conference on Computer Design)
IEEE International Performance Conference on Computing and Communication 1999, 2000
IEEE Workshop on Workload Characterization
Workshop on Media Processors and Digital Signal Processors, Nov 1999 (in conjunction with IEEE Micro-32)
IEEE International Conference on Computer Design (ICCD) 1998, 1999
North Atlantic Test Symposium 1997
Reviewer for McGraw Hill 2001-2002
Reviewer for McGraw Hill, 2000
Reviewer for Prentice Hall USA (1995), Prentice Hall UK (1999)
Reviewer for Addison Wesley (1997)
Kluwer Academic Publishers Book Proposal Reviewer, 2001
Reviewer for IEEE Computer's Special Issue on Billion Transistor Processors, 1997
Member, Focus Group on IEEE Spectrum and its Web Site, Tammadge Market Research Group, May 1998

Other Activities:

1. Robotics Club, West Lake High School, Team Manager, 2016-2017
2. **Technology Club Organizer**: St. Ignatius Martyr School, Austin, TX, 2012-2013
3. **Elementary School PSIA Math Coach, 2012**
4. **Elementary School PSIA Spelling Coach, 2011**
5. **Elementary School PSIA Spelling Coach, 2010**
6. **Judge**: Texas High School State Science and Engineering Fair, April 2001
7. **Judge:** Florida High School Science Fair, 1994

PUBLICATIONS: **In listing publications, please use the following format: author's name(s), title of paper, journal name, volume number, page numbers, month and year.)*

A. Refereed Archival Journal Publications

1. Han, Rui, Lizy Kurian John, and Jianfeng Zhan. "Benchmarking Big Data Systems: A Review." IEEE Transactions on Services Computing, May/June 2018, Vol. 11, Issue 3, pp. 580-597, ISSN: 1939/1374, DOI: 10.1109/TSC.2017.2730882
2. Xinnian Zheng; Lizy K. John; Andreas M Gerstlauer , "LACross: Learning-based Fine-grained Analytical Cross-Platform Performance and Power Prediction", International Journal of Parallel Programming (IJPP), preprint Jan 2017
3. Zhuoran Zhao, Andreas Gerstlauer, Lizy K. John, "Source-Level Performance, Energy, Reliability, Power and Thermal (PERPT) Simulation," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 36, no. 2, pp. 299-312, Feb 2017
4. Faisal Iqbal and Lizy K. John, Dynamic Core Allocation and Packet Scheduling in Multi Core Network Processors", IEEE Transactions on Computers, 2016
5. Zhibin Yu, Lieven Eeckhout, Tao Li, Lizy K. John, , "GPGPU-MiniBench: Accelerating GPGPU Micro-Architecture Simulation", IEEE Transactions on Computers, 2015, Vol. 64, Issue 11, pp. 3153-3166
6. Arun Nair, Stijn Eyerman, Jian Chen, Lizy John, Lieven Eeckhout, "Mechanistic Modeling of Architectural Vulnerability Factor", **ACM Transactions on Computer Systems**, 2015, Vol. 32, Issue 4
7. Youngtaek Kim, Sanjay Pant, Srilatha Manne, Michael Schulte, Lloyd Bircher, Madhu Saravana Sibi Govindan, and Lizy K. John, "Automating Stressmark Generation for testing Processor Voltage Fluctuations", **IEEE Micro**, July/August, pp. 66-75, 2013
8. Karthik Ganesan and Lizy K. John, Automatic Generation of Miniaturized Synthetic Proxies for Target Applications to Efficiently Design Multicore Processors, **IEEE Transactions on Computers**, Vol. 63, No. 4, pp. 833-846, April 2014
9. Jian Chen, Arun Nair, and Lizy K. John, Predictive Heterogeneity-Aware Application Scheduling for Chip Multiprocessors, **IEEE Transactions on Computers**, Vol. 63, No.2, pp. 435-447, February 2014.
10. Dimitris Kaseridis, Muhammad Faisal Iqbal, and Lizy K. John, Cache Friendliness Aware Management of Last-level Caches for High Performance Multi-core Systems, **IEEE Transactions on Computers**, Vol. 63, No. 4, pp. 874-887, April 2014.
11. Lloyd Bircher and Lizy K. John, Complete System Power Estimation using Processor Performance Events, **IEEE Transactions on Computers**, Vol. 61, No. 4, pp. 563-577, April 2012
12. Lloyd Bircher and Lizy K. John, Core-Level Activity Prediction for Multi-Core Power Management, **IEEE Journal** on Emerging and Selected Topics in Circuits and Systems (JETCAS), September 2011, pp. 218-227.
13. J. Stuecheli, D. Kaseridis, L. K. John, D. Daly and H. C. Hunter, "Coordinating draM and Last –Level Cache Policies with the Virtual Write Queue", Virtual Write Queue: " **IEEE MICRO TOP Picks**, 2011 *v. 31*, 90--98, Published by the IEEE Computer Society, 2011
14. Byeong Kil Lee and Lizy K. John, "Hardware acceleration for media / transaction applications in Network Processors", vol. 17, No. 12, pp. 1691-1697, **IEEE Transactions on VLSI**, December 2009
15. Ajay Joshi, Lieven Eeckhout, Robert H. Bell Jr. and L. K. John, Distilling the Essence of Proprietary Workloads into Miniature Benchmarks. **ACM Transactions** on **Architecture and Code Optimization** (**TACO**), Vol. 5, Issue 2, August 2008, pp.10:1-10:33
16. Yue Luo, Ajay Joshi, Aashish Phansalkar, Lizy K. John, and Joydeep Ghosh, "Analyzing and Improving Clustering Based Sampling for Microprocessor Simulation". Accepted at International **Journal of High Performance Computing and Networking**, To appear 2008

17. Ajay Joshi, Yue Luo and Lizy John, Applying Statistical Sampling for Fast and Efficient Simulation of Commercial Workloads, **IEEE Transactions on Computers**, Vol. 56, No. 11, November 2007
18. C. Isen, H. Angepat, L. John, J. P Choi, H. J. Song, "Embedded Java Benchmark Analysis on the ARM Processor", **International Journal on Embedded Systems**, Vol. 4, Issue 1, 2009, pp. 40-53
19. Tao Li , Lizy Kurian John , Anand Sivasubramaniam , N. Vijaykrishnan , Juan Rubio, OS-Aware Branch Prediction: Improving Microprocessor Control Flow Prediction for Operating Systems, **IEEE Transactions on Computers**, Vol. 56, No. 1, January 2007, pp. 2-17
20. Joshua J. Yi , Lieven Eeckhout , David J. Lilja , Brad Calder , Lizy K. John , James E. Smith The Future of Simulation: A Field of Dreams, **IEEE Computer**, November 2006, pp. 22-29
21. Ajay Joshi, Aashish Phansalkar, Lieven Eeckhout, and Lizy K. John, "Measuring Benchmark Similarity Using Inherent Program Characteristics", **IEEE Transactions on Computers**, Vol. 55, No. 6, June 2006, pp. 769-782.
22. Madhavi Valluri, Lizy John and Heather Hanson, "Hybrid-Scheduling: A Technique to Exploit Static Schedules for Reduced Energy Consumption in High-Performance Processors. **IEEE Transactions on VLSI**. Vol. 14, No. 9, September 2006, pp. 1039-1043
23. Byeong Kil Lee, L. K. John and E. B. John, "Architectural Enhancements for Network Congestion Control Applications". **IEEE Transactions on VLSI**, VOL.14, NO. 6, pp. 609-615, JUNE 2006
24. Shiwen Hu, Madhavi Valluri, and Lizy K. John, "Effective Adaptive Computing Environment Management via Dynamic Optimization", **ACM Transactions** on **Architecture and Code Optimization (TACO)**, Vol. 3, No. 4, Dec 2006, pp. 477-501
25. Tao Li and Lizy Kurian John, "Operating System Power Minimization through Run-time Processor Resource Adaptation". Accepted at **Journal of Microprocessor and Microsystems**, Volume 30, Issue 4, page 173-224, June 2006
26. Juan Rubio and Lizy K. John, "Reducing Server Data Traffic using a Hierarchical Computation Model", **IEEE Transactions on Parallel and Distributed Systems**, Oct 2005, 933-943.
27. Byeong Kil Lee and Lizy K. John, "Implications of Executing Compression and Encryption Applications on General Purpose Processors", **IEEE Transactions on Computers**, July 2005, Vol. 54, No. 7, pp. 917-922.
28. Tao Li, Ravi Bhargava, L. K. John, "Adapting Branch-Target Buffer to Improve the Target Predictability of Java Code", **ACM Transactions** on Architecture and Code Optimization (TACO), Vol. 2, No. 2, June 2005, pp. 109-130.
29. L. Eeckhout, Y. Luo, K. Bosschere, and Lizy K. John, "BLRL: Accurate and Efficient Warmup for Sampled Processor Simulation," **The Computer Journal**. Vol. 48. No. 4, May 2005, pp. 451-459.
30. Yue Luo and Lizy K. John, "Efficiently Evaluating Speedup Using Sampled Processor Simulation, **Computer Architecture Letters**, vol 3, Sept 2004, pp. 22-25.
31. D. Burger, S. Keckler, K. S. McKinley, M. Dahlin, L.K. John, C. Lin, C. R. Moore, J. Burrill, R. G. McDonald, W. Yoder and the TRIPS team, "Scaling to the End of Silicon with EDGE architectures", **IEEE Computer**, July 2004, pp. 44-55.
32. Yue Luo and Lizy John, "Locality Based On-Line Trace Compression", **IEEE Transactions on Computers**, Volume 53, Number 6, June 2004, pp. 723-731.
33. Shiwen Hu, Ravi Bhargava, and Lizy K. John, "The Role of Return Values in Exploiting Speculative Method-Level Parallelism", **The Journal of Instruction-Level Parallelism** (**JILP**), Vol. 5. November 2003.
34. Deepu Talla, Lizy John, and Doug Burger, "Bottlenecks in multimedia processing with SIMD style extensions and architectural enhancements", **IEEE Transactions on Computers**, Volume 52, Number 8, ISSN 0018-9, Aug 2003, pp. 1015-1031.

35. Yue Luo, Pattabi Seshadri, Juan Rubio, Lizy John and Alex Mericas, "Benchmarking Internet Servers on Superscalar Machines", **IEEE Computer**, Feb 2003, pp. 34-40.
36. Tao Li and L. John, "ADirpNB: A cost-effective way to Reduce Directory Memory Overhead for Full Map Directory Based Cache Coherence Protocols", **IEEE Transactions on Computers**, Sept 2001, Vol. 50, No. 9, pp. 921-934.
37. R. Radhakrishnan, N. Vijayakrishnan, L. K. John, A. Sivasubramaniam, J. Rubio, and J. Sabarinathan, "Java Runtime Systems: Characterization and Architectural Implications", **IEEE Transaction on Computers**, Feb 2001, Vol.50, No. 2, pp. 131-146.
38. Lizy Kurian John, "Data Placement Schemes to Reduce Conflicts in Interleaved Memories", **The Computer Journal**, Vol. 43, No. 2, 2000.
39. Lizy Kurian John, "Memory Chips with Adjustable Configurations", **The VLSI Design Journal**, Gordon Breach Publishers, Vol. 10(2), 1999, pp. 203-215.
40. L. K. John, Tao Li and A. Subramanian, "Annex Cache: A Cache Assist to implement Selective Caching", **Microprocessors and Microsystems Journal,** December 1999, Volume 23 Nos 8-9, Elsevier Publications, pp. 537-551.
41. Lizy Kurian John and Eugene B. John, "A Dynamically Reconfigurable Interconnect for Array Processors", **IEEE Transactions on VLSI**, March 1998, Vol. 6, No. 1, pp. 150-157.
42. Lizy Kurian John, Yu-cheng Liu, "Performance Model for a Prioritized Multiple-Bus Multiprocessor System", **IEEE Transactions on Computers**, Vol. 45, No. 5, May 1996, pp. 580-588.
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1. Rob Bell Jr. and L. K. John, "Improved Automatic Test Case Synthesis for Performance Model Validation and the Role of Statistical Simulation". Submitted to **IEEE Transactions on Computers**.
2. Tao Li, Lizy Kurian John, "OS-aware Tuning: Improving I-Cache Energy Efficiency on the System Workloads". Submitted to **IEEE Transactions on Computers**.

B. Refereed Conference Proceedings

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114. Tao Li and Lizy Kurian John, "Run-time Modeling and Estimation of Operating System Power Consumption", In Proceedings of the International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), 2003, pp. 160-171. (Acceptance rate: 26 accepted/222 submissions = 12%)

115. Ravi Bhargava and Lizy K. John, "Improving Dynamic Cluster Assignment for Clustered Trace Cache Processors", In Proceedings of the 30th International Symposium on Computer Architecture (ISCA 2003), June 2003, pp. 264-274. (Acceptance rate: 36 accepted/184 submissions = 20%)

116. Robert H. Bell, Jr. and Lizy Kurian John, "Interface Design Techniques for Single Chip Systems", In Proceedings of the Sixteenth IEEE Conference on VLSI Design, January 2003, pp. 388-394. (Acceptance rate: 84 accepted/210 submissions = 40%)

117. Tao Li, Lizy John, Anand Sivasubramaniam, Narayanan Vijaykrishnan and Juan Rubio, "Understanding and Improving Operating System Effects in Control Flow Prediction", In Proceedings of the Tenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-X), 2002, pp. 68-80. (Acceptance rate: 24 accepted/130 submissions = 18%)

118. Tao Li, Lizy John and Robert H. Bell, Jr., "Modeling and Evaluation of Control Flow Prediction Schemes Using Complete System Simulation and Java Workloads", In Proceedings of the tenth IEEE/ACM International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS), 2002, pp. 391-400. (Acceptance rate: 51 accepted/180 submissions = 28%)

119. Tao Li, Ravi Bhargava and Lizy John, "Rehashable BTB: An Adaptive Branch Target Buffer to Improve the Target Predictability of Java Code", In Proceedings of the International Conference on High Performance Computing (HiPC), 2002, pp. 597-608. (Acceptance rate: 57 accepted/145 submissions = 39%)

120. Eugene B. John, Stefan Petko, Lizy John and Jason Law, "Access Time and Energy Tradeoffs for Caches in High Frequency Microprocessors", In Proceedings of 45th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Tulsa, Oklahoma, Aug 2002, pp. 421- 424 (vol.3).

121. Byeong Kil Lee, Lizy John, "Implications of Programmable General Purpose Processors for Compression/Encryption Applications", IEEE 13th International Conference on Application-specific Systems, Architectures and Processors (ASAP 2002), San Jose, California, July 2002, pp. 233-242.

122. Ravi Bhargava and Lizy John, "Latency and Energy Aware Value Prediction for High-Frequency Processors", In Proceedings of 16th ACM International Conference on Supercomputing (ICS), June 2002, pp. 45-56. (Acceptance rate: 31 accepted/144 submissions = 22%)

123. Sudhanva Gurumurthi, Anand Sivasubramaniam, Mary Jane Irwin, Narayanan Vijaykrishnan, Mahmut Kandemir, Tao Li, and Lizy Kurian John, "Using Complete Machine Simulation for Software Power Estimation: The SoftWatt Approach", In Proceedings of the 2002 International Symposium on High Performance Computer Architecture (HPCA), Feb 2002, pp. 141-150. (Acceptance rate: 26 accepted/130 submissions = 20%)

124. Robert H. Bell, Jr., Chang Yong Kang, Lizy John, Earl E. Swartzlander, Jr., "CDMA as a Multiprocessor Interconnect Strategy", Proceedings of the Thirty-Fifth Asilomar Conference on Signals, Systems, and Computers, Nov 2001, pp. 1246-1250 (vol. 2).

125. Y. Luo and L. John, "Workload Characterization of multithreaded Java Servers", International Symposium on Performance Analysis of Software and Systems (ISPASS), 2001, pp. 128-136. (Acceptance rate: 20 accepted/68 submissions = 29%)

126. Tao Li and L. John, "Understanding the Control Flow Transfer and its Predictability in Java Processing", International Symposium on Performance Analysis of Software and Systems (ISPASS), 2001, pp. 65-76. (Acceptance rate: 20 accepted/68 submissions = 29%)

127. D. Talla and L. John, "Cost-effective Hardware Acceleration of Multimedia Applications", International Conference on Computer Design (ICCD 2001), Sept 2001, pp. 415-424. (Acceptance rate: 61 accepted/181 submissions = 34%)

128. R. Radhakrishnan, R. Bhargava, and L. K. John, "Improving Java Performance using Hardware Translation", Proceedings of the International Conference on Supercomputing (ICS 2001), Italy, June 2001, pp. 427-439. (Acceptance rate: 45 accepted/133 submissions = 34%)

129. Serene Banerjee, Lizy K. John, and Brian L. Evans, "The EASE Branch Predictor", Proceedings of the International Conference on Communications, Computers & Devices, Dec 2000. (Acceptance rate: 69 accepted/181 submissions = 38%)

130. S. Banerjee, H. R. Sheikh, L. K. John, B. L. Evans, and A. C. Bovik, "VLIW DSP vs. Superscalar Implementation of a Baseline H.263 Video Encoder", Proc. IEEE Asilomar Conf. on Signals, Systems, and Computers, vol. 2, Pacific Grove, CA, Oct 29-Nov 1, 2000, pp. 1665-1669.

131. D. Talla, L. John, V. Lapinskii and B. Evans, "Evaluating Signal Processing and Multimedia Applications on SIMD, VLIW and Superscalar Architectures", In Proceedings of the IEEE International Conference on Computer Design (ICCD 2000), Sept 2000, pp. 163-172. (Acceptance rate: 69 accepted/181 submissions = 38%)

132. R. Radhakrishnan, D. Talla, L. John, "Allowing for ILP in an Embedded Java Processor", Proceedings of the ACM/IEEE International Symposium on Computer Architecture (ISCA2000), Vancouver, Canada, June 2000, pp. 294-305. (Acceptance rate: 29 accepted/166 submitted = 17%)

133. L. Tao, L. K. John, N. Vijayakrishnan, A. Sivasubramaniam, A. Murthy, and J. Sabarinathan, "Using Complete System Simulation to Characterize SPECjvm98 Benchmarks", Proceedings of the ACM International Conference on Supercomputing (ICS 2000), Santa Fe, New Mexico, May 2000, pp. 22-33. (Acceptance rate: 33 accepted/122 submissions = 28%)

134. R. Bhargava and L. K. John, "Issues in the Design of Store Buffers in Dynamically Scheduled Processors", In Proceedings of IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2000), Austin, TX, April 24-25 2000, pp. 76-87.

135. D. Talla and L. K. John, "Execution Characteristics of Multimedia Applications on a Pentium II Processor", Proceedings of the IEEE International Performance, Computing and Communications Conference (IPCCC), Phoenix, AZ, Feb 2000, pp. 516-523.

136. R. Radhakrishnan, N. Vijaykrishnan, L. K. John and A. Sivasubramaniam, "Architectural Issues in Java Runtime Systems", Proceedings of the IEEE International Symposium on High Performance Computer Architecture (HPCA-2000), Toulouse, France, Jan 2000, pp. 387-398. (Acceptance rate: 35 accepted/163 submissions = 21%)

137. D. Talla, S. Rao and L. John, "An Evolutionary Computation Embedded IIR LMS Algorithm", International Conf on Signal Processing Applications and Technology (ICSPAT), Orlando, FL, Nov 1999.

138. M. Clark and L. K. John, "Performance Evaluation of Configurable Hardware Features on the AMD-K5", In Proceedings of the IEEE International Conference on Computer Design (ICCD 99), Oct 1999, pp. 102-107. (Acceptance rate: 71 accepted/220 submissions = 32%)

139. S. Srivatsan, and L. John, "On the Use of Pseudorandom Sequences for High Speed Resource Allocators in Superscalar Processors", Proceedings of the IEEE International Conference on Computer Design (ICCD 99), Oct 1999, pp. 124-130. (Acceptance rate: 71 accepted/220 submissions = 32%)

140. R. Radhakrishnan, J. Rubio and L. John, "Characterization of Java Applications at ByteCode and UltraSPARC Machine Code Levels", ICCD 1999, Oct 1999, pp. 281-284. (Acceptance rate: 71 accepted/220 submissions = 32%)

141. G. E. Allen, B. L. Evans, and L. K. John, "Real-Time High-Throughput Sonar Beamforming Kernels Using Native Signal Processing and Memory Latency Hiding Techniques", Proc. IEEE Asilomar Conf on Signals, Systems and Computers, Pacific Grove, CA, Oct 24-27, 1999, pp. 137-141.

142. D. Talla and L. John, "Quantifying Effectiveness of MMX in Native Signal Processing", IEEE Midwest Symposium on Circuits and Systems, Aug 1999.

143. H. Nguyen and L. John, "Exploiting SIMD Parallelism in DSP and Multimedia Algorithms Using the AltiVec Technology", Proceedings of the ACM International Conference on Supercomputing (ICS 99), Greece, June 1999, pp. 11-20. (Acceptance rate: 57 accepted/180 submissions = 32%)

144. R. Radhakrishnan and L. John, "A Performance Study of Modern Web Server Applications", Euro-Par 1999, Lecture Notes in Computer Science, Springer, pp. 239-247. (Acceptance rate: 188 acccepted/343 submissions = 55%)

145. D. Talla and L. K. John, "Performance Evaluation and Benchmarking of Native Signal Processing", Euro-Par 1999, Lecture Notes in Computer Science, Springer, pp. 266-270. (Acceptance rate: 188 acccepted/343 submissions = 55%)

146. R. Shalem, E. John and L. K. John, "A Novel Low Power Static Energy recovery Full Adder Cell", Proceedings of the 1999 IEEE Great Lakes Symposium on VLSI, Michigan, March 1999, pp. 380-383.

147. B. Grayson, L. John and C. Chase, "The Effects of Memory-Access Ordering on Multiple-Issue Uniprocessor Performance", Proceedings of the IEEE Performance, Computers and Communications Conference (IPCCC), Feb 1999, pp. 293-302.

148. R. Bhargava, L. K. John and F. Matus, "Accurately Modeling Speculative Instruction Fetching in Trace-Driven Simulation", Proceedings of the IEEE Performance, Computers and Communications Conference (IPCCC), Feb 1999, pp. 65-71.

149. D. Tang, A. M. G. Maynard and L. K. John, "Contrasting Branch Characteristics and Branch Predictor Performance of C++ and C Programs", Proceedings of the IEEE Performance, Computers and Communications Conference (IPCCC), Feb 1999, pp. 275-283.

150. S. Srinivasan, P. Chabra, P. Jaini, A. Aziz and L. John, "Formal Verification of Snoop-based Cache Coherence Protocol using Symbolic Model Checking", in the Proceedings of the 12th International Conference on VLSI Design (Published by IEEE Computer Society), India, Jan 1999, pp. 288-293. (Acceptance rate: 75 accepted/194 submissions = 39%)

151. R. Bhargava, L. K. John, B. L. Evans, and R. Radhakrishnan, "Evaluating MMX Technology using DSP and Multimedia Applications", Proceedings of the IEEE Symposium on Microarchitecture (MICRO-31), Dallas, Texas, Dec 1998, pp. 37-46. (Acceptance rate: 28 accepted/108 submissions = 26%)

152. R. Radhakrishnan and L. John, "Execution Characteristics of Object Oriented Programs on the UltraSPARC-II", Proceedings of the 5th International Conference on High Performance Computing (Published by IEEE Computer Society), Dec 1998, pp. 202-211. (Acceptance rate: 62 accepted/104 submissions = 60%)

153. L. John, Y. Teh, F. Matus and C. Chase, "Code Coalescing Unit: A Mechanism to Facilitate Load Store Data Communication", Proceedings of IEEE International Conference on Computer Design, Oct 1998, pp. 550-557. (Acceptance rate: 69 accepted/189 submissions = 36%)

154. G. Beers and L. John, "A Novel Memory Bus Driver/Receiver Architecture for Higher Throughput", Proceedings of the International Conference on VLSI Design (Published by IEEE Computer Society), Jan 1998, pp. 259-264. . (Acceptance rate: 57 accepted/123 submissions = 46%)

155. A. Kulkarni, N. Chander, S. Pillai, L. John, "Modeling and Analysis of the Difference-Bit Cache", Proceedings of the Great Lakes Symposium on VLSI, 1998, pp. 140-145.

156. E. John, F. Hudson and L. K. John, "Hybrid Tree: A Salable Optoelectronic Interconnection Network for Parallel Computing", Proceedings of the Hawaii International Conference on System Sciences, Jan 1998, Vol. VII, pp. 466-474. (Acceptance rate: 75 accepted/181 submissions = 41%)

157. L. John and A. Subramanian, "Design and Performance Evaluation of a Cache Assist to implement Selective Caching", Proceedings of the IEEE International Conference on Computer Design, Oct 1997, pp. 510-518. (Acceptance rate: 91 accepted/175 submissions = 52%)

158. Lizy Kurian-John and R. Radhakrishnan, "Improving the Parallelism and Concurrency in Decoupled Architectures", Proceedings of the IEEE Symposium on Parallel and Distributed Processing, New Orleans, Oct 1996, pp. 130-137. (Acceptance rate: 84 accepted/217 submissions = 39%)

159. L. K. John, "VaWiRAM: A Variable Width Random Access Memory Module", Proceedings of the 9th International Conference on VLSI Design, Jan 1996, pp. 219-224. (Acceptance rate: 75 accepted/137 submissions = 55%)

160. L. K. John, R. Reddy, V. Kammila, and P. Maurer, "Investigating the Use of Cache as a Local Memory", Proceedings of the International High Performance Computing Conference (HiPC), Dec 1995, pp. 117-122. (Acceptance rate: 126 accepted/213 submissions = 59%)

161. L. K. John, V. Reddy, P. Hulina and L. Coraor, “Program Balance and its Impact on High Performance RISC Architectures”, Proceedings of the International Symposium on High Performance Computer Architecture (HPCA), Jan 1995, pp. 370-379. (Acceptance rate: 36 accepted/190 submissions = 19%)

162. L. Kurian, D. Brewer, and E. John, “Design of a Highly Reconfigurable Interconnect for Array Processors”, Proceedings of the 8th International Conference on VLSI Design, Jan 1995, pp. 321-325. (Acceptance rate: 77accepted/139 submissions = 55%)

163. L. K. John, V. Reddy, P. T. Hulina and L. D. Coraor, “A Comparative Evaluation of Software Techniques to Hide Memory Latency”, Proceedings of the 28th Hawaii International Conference on System Sciences (HICSS), Jan 1995, Vol. I, 229-238.

164. L. Kurian and Y. Liu, “Performance Model for a Prioritized Multiple-Bus Multiprocessor System", Proceedings of the IEEE Symposium on Parallel and Distributed Processing (IPDPS), Oct 1994, pp. 577-584.

165. L. Kurian, B. Choi, P. T. Hulina, and L. D. Coraor, “Module Partitioning and Interlaced Data Placement Schemes to Reduce Conflicts in Interleaved Memories", Proceedings of the 23rd International Conference on Parallel Processing, Aug 1994, Vol. I, pp. 212 - 219.

166. L. Kurian, P. T. Hulina and L. D. Coraor, “Memory Latency Effects in Decoupled Architectures with a Single Data Memory Module", Proc. of the 19th Intl. Symposium on Computer Architecture (ISCA), Australia, May 1992, pp. 236-245.

167. L. Kurian and M. J. Thazhuthaveetil, “Effect of Hot Spots on Multiprocessor Systems using Circuit Switched Interconnection Networks", Proceedings of the 20th International Conference on Parallel Processing, Aug 1991, Vol. I, pp. 554 - 557.

168. L. Kurian, P. T. Hulina, L. D. Coraor and D. N. Mannai, “ Classification and Performance Evaluation of Instruction Buffering Techniques", Proceedings of the 18th International Symposium on Computer Architecture (ISCA), Toronto, Canada, May 1991, pp. 150-159

C. Other Major Publications

Invited Conference Papers:

1. Juan Rubio and Lizy K. John, “ Understanding the Execution of a Radar Motion Indication Application”, Proceedings of International Conference on Parallel and Distributed Systems (ICPADS) 2004.
2. Deepu Talla and Lizy John, “Facts and myths about media processing on general-purpose processors”, In Proceedings of IEEE International Conference on Information Technology: Research and Education (Special Session on Technology and Trends in Media Processing), Newark, NJ, Aug 10-13: 2003

Other Conference and Workshop Papers:

1. Wooseok Lee, Dam Sunwoo, Christopher D. Emmons, Andreas Gerstlauer and Lizy K. John, “ Exploring Heterogeneous-ISA Core Architectures for High Performance Energy-Efficient Mobile SoCs (Poster), IEEE Great Lakes Symposium on VLSI (GLSVLSI), May 2017
2. Reena Panda and Lizy K. John, Proxy Benchmarks for Emerging Workloads, Poster Paper at ISPASS April 2017
3. Shuang Song, Andreas Gerstlauer and Lizy K. John Fine-grained Power Analysis of Emerging Graph Processing Workloads for Cloud Operations Management, IEEE Big Data 2016 Workshop, Dec 2016
4. Alexander C. Schulyak and Lizy K. John, Identifying Performance Bottlenecks in Hive: Use of Processor Counters, IEEE Big Data 2016 Workshop, Dec 2016
5. Jiajun Wang, Ahmed Khawaja, George Biros, Andreas Gerstlauer and Lizy K. John, “ Optimizing GPGPU Kernel summation for Performance Energy Efficiency”, ICPP Workshop on Heterogeneous and Unconventional Cluster Architectures and applications (HUCAA), August 2016
6. Reena Panda, Yasuko Eckert, Nuwan Jayasena, Onur Kayiran, Michael Boyer, Lizy Kurian John, “Prefetching Techniques for Near-memory Throughput processors”, SRC Tech CON, Sep 2016

7. Rui Han, Shulin Zhan, Chenrong Shao, Junwei Wang, Lizy K. John, Jiangtao Xu, Gang Lu, and Lei Wang. *BigDataBench-MT: A Benchmark Tool for Generating Realistic Mixed Data Center Workloads*. In: 2015 ACM Symposium on Cloud Computing (SoCC 2015), Hawai'i, USA. Poster paper.
8. TECH CON paper, September 2015 Michael LeBeane, Shuang Song and Lizy K. John, WattWatcher: Fine-Grained Power Estimation For Emerging Workloads, SRC TECH CON
9. TECH CON paper, Xinnian Zheng, A. Gerstlauer, and Lizy K. John, "Learning-based Analytical Cross-Platform Performance Prediction", SRC TECH CON, Sept 2015
10. Jee Ho Ryoo Michael LeBeane, Muhammad Faisal Iqbal, Lizy John Control Flow Behavior of Cloud Workloads, IEEE International Symposium on Workload Characterization, 2014, poster paper.
11. Z. Zhao, D. Lee, A. Gerstlauer and L. John, "Host-Compiled reliability Modeling for fast Estimation of Architectural Vulnerabilities", SELSE, April 2015
12. Reena Panda, Christopher Erb, and Lizy K. John, "Big versus Little: Who will trip?", SELSE 2015 poster, Austin, Texas, April 2015
13. M. F. Iqbal and L. K. John, "LAPS: Locality Aware Packet Processing", SRC TechCon 2013
14. Zhibin Yu, Lieven Eeckhout, Nilanjan Goswami, Tao Li, Lizy K. John, Hai Jin, Chengzhong Xu, Accelerating GPGPU Architecture Simulation, SIGMETRICS 2013 poster
15. Don Owen Jr., The Feasibility of Memory Encryption and Authentication, Fast Path Workshop, Held in conjunction with ISPASS April 2013, Austin, Texas
16. Muhammad Faisal Iqbal and Lizy K. John, Efficient Traffic Aware Power Management for Multicore Communications Processors **SRC TECHCON 2012**
17. M. Faisal Iqbal and Lizy K. John, "Power and Performance Analysis of Network Traffic Prediction Techniques", IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) April 2012
18. Youngtaek Kim and Lizy K. John, Impact of compiler optimizations on voltage droops and reliability of an SMT, multi-core processor, The 1st International Workshop on Secure and Resilient Architectures and Systems (SRAS) in conjunction with PACT 2012. September 2012
19. Youngtaek Kim, Lizy Kurian John, "Automated di/dt stressmark generation for microprocessor power distribution networks," *IEEE Workshop on Silicon Errors in Logic-System Effects(SELSE)*, Mar. 2012.
20. Lizy K. John, Jungho Jo and Karthik Ganesan, "Workload Synthesis for a Communications SoC", Workshop on SoC Architectures, Accelerators and Workloads (SAW) in conjunction with HPCA, February 12, 2011, San Antonio
21. J. Jo, L. K. John, M. Reese, and J. Holt "Validation of Synthetic Benchmarks by Measurement", Workshop on Unique Chips and Systems (UCAS), 2010.
22. F. Iqbal and L. K. John, "Confusion by All Means", Workshop on Unique Chips and Systems (UCAS), 2010.
23. Ciji Isen and Lizy John, A Tale of Two Processors: Revisiting the RISC-CISC Debate,. 2009 SPEC Benchmark Workshop. January 2009, Springer LNCS 5419, pp.57-76
24. Karthik Ganesan, Deepak Panwar, and Lizy John, Generation,Validation and Analysis of SPEC CPU2006 Simulation Points Based on Branch, Memory, and TLB Characteristics,. 2009 SPEC Benchmark Workshop. January 2009, Springer LNCS 5419, pp. 121-137
25. Dimitris Kaseridis and Lizy John, Performance Analysis of Multiple Threads/Cores Using the UltraSPARC T1", Workshop on Unique Chips and Systems (UCAS-4), April 20th, 2008, Austin

26. Ajay Joshi, Lieven Eeckhout, Lizy John, and Ciji Isen. Stressing Microarchitectures Through Custom Benchmark Synthesis, *IBM Center for Advanced Studies (IBM CAS)*, 2008.
27. Ajay Joshi, Lieven Eeckhout, and Lizy John. The Return of Synthetic Benchmarks. *Standard Performance Evaluation Corporation Benchmark Workshop*, January 2008.
28. Ciji Isen, Lizy K. John, On the Object Orientedness of C++ Programs in SPEC CPU 2006, *Standard Performance Evaluation Corporation Benchmark Workshop*, January 2008.
29. Sarah Bird, Aashish Phansalkar, Lizy K. John, Alex Mericas, Rajeev Indukuru , Characterization of Performance of SPEC CPU Benchmarks on Intel's Core Microarchitecture based Processor, SPEC Workshop January 2007
30. Ajay Joshi, Lieven Eeckhout, Robert H. Bell Jr., and Lizy John, Performance Cloning: A Technique for Disseminating Proprietary Applications as Benchmarks, 8th annual IBM CAS Conferences, March 2007
31. Sarah Bird, Aashish Phansalkar, Lizy K. John, Performance Characterization of SPEC CPU Benchmarks on Intel's Core Microarchitecture based processor, 8th Annual IBM CAS Conference March 2, 2007
32. Jian Chen, Nidhi Nayyar, and Lizy K. John, Mapping of Applications to Heterogeneous Multi-cores Based on Micro-architecture Independent Characteristics, Third Workshop on Unique Chips and Systems (UCAS), Held in conjunction with IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), April 2007.
33. Dimitris Kaseridis and Lizy K. John. CMP/CMT Scaling of SPECjbb2005 on UltraSPARC T1 Tenth Workshop on Computer Architecture Evaluation using Commercial Workloads, February 2007
34. Brian Gaide and Lizy John, A High Throughput Self-Timed FPGA Core Architecture, Digest of UCAS-2 (Workshop on Unique Chips and Systems), held in conjunction with ISPASS 2006, March 2006
35. Ajay Joshi, Rob Bell Jr., and Lizy K. John, "Capturing Locality of Reference and Branch Predictability of Programs in Synthetic Workloads", IBM Center for Advanced Studies (CAS) Conference, Feb 2006.
36. Rob Bell, Jr., Rajiv R. Bhatia, Lizy K. John, Jeff Stuecheli, John Griswell, Paul Tu, Louis Capps, Anton Blanchard, Ravel Thai, "Automatic Testcase Synthesis and Performance Model Validation for High-Performance PowerPC Processors", IBM Center for Advanced Studies (CAS) Conference, Feb 2006.
37. Aashish Phansalkar and Lizy K. John, "Performance Prediction using Program Similarity", SPEC workshop, Jan 2006.
38. Joshua J. Yi, Ajay Joshi, Resit Sendag, Lieven Eeckhout, and David J. Lilja, "Analyzing the Processor Bottlenecks in SPEC CPU 2000" 2006 SPEC Benchmark Workshop, Jan 2006.
39. W. L. Bircher, J. Law, M. Valluri and Lizy K. John, "Effective Use of Performance Monitoring Counters for Run-Time Prediction of Power", Poster in IBM Austin Conference on Energy-Efficient Design (ACEED) 2005 IBM, Austin, March 2005.
40. A. Phansalkar, A. Joshi, L. Eeckhout and L. John, "Measuring Program Similarity: Experiments with SPEC CPU benchmark suites", Proceedings of the IBM Center for Advanced Studies (CAS) Conference, Austin, TX, Feb 2005.
41. R. Bell Jr and L. K. John, "Capturing the Essence of Benchmarks: A New Approach to benchmark Synthesis", Proceedings of the IBM Center for Advanced Studies (CAS) Conference, Austin, TX, Feb 2005.
42. Robert H. Bell Jr., Lieven Eeckhout, Lizy K. John, and Koen De Bosschere, "Deconstructing and Improving Statistical Simulation in HLS", Third Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD), along with ISCA June 2004.
43. Madhavi Valluri and Lizy John, "Hybrid-Scheduling: A Compile-Time Approach for Energy-Efficient Superscalar Processors", Poster in IBM Austin Conference on Energy-Efficient Design (ACEED) 2004 IBM, Austin, TX, March 2-4, 2004.
44. Yue Luo and Lizy John, "Using Statistical Theory to Study Issues in Microprocessor Simulation", Proceedings of the Fifth Annual Austin Center for Advanced Studies Conference (CAS), Feb 2004.

45. Ravi Bhargava and Lizy K. John, “Performance and Energy Impact of Instruction-Level Value Predictor Filtering”, In Proceedings of the First Value-Prediction Workshop (VPW1) [held with ISCA 03], June 2003.
46. Shiwen Hu, Ravi Bhargava, and Lizy K. John, “The Role of Return Values in Exploiting Speculative Method-Level Parallelism”, In Proceedings of the First Value-Prediction Workshop (VPW1) [held with ISCA'03], June 2003.
47. Shiwen Hu, Lizy John, “Comparison of JVM Phases on Data Cache Performance”, In the First Workshop on Managed Run Time Workloads, San Francisco, CA, March 2003.
48. Yue Luo and Lizy K. John, “Automatically Selecting Representative Traces for Simulation Based on Cluster Analysis of Instruction Address hashes”, IBM CAS Conference, Feb 2003.
49. Pattabi Seshadri, Lizy John and Alex Mericas, “Workload Characterization of Java Server Applications on Two PowerPC Processors”, In Proceedings of the Third Annual Austin Center for Advanced Studies Conference, Austin, TX, Feb 15, 2002.
50. Lizy John, “Contemporary Performance Evaluation: Overwhelming Effort? Irrelevant Results? “Position paper, NSF workshop, Dec 2001.
51. Deepu Talla and Lizy John, “A decoupled architecture for accelerating multimedia applications, Proceedings of Workshop on Memory Access Decoupled Architectures” in conjunction with IEEE International Conference on Parallel Architectures and Compilation Techniques, Barcelona, Spain, Sept 8, 2001. (Selected as one of 2 best papers)
52. P. Sheshadri and L. K. John, “Characterization of Web Server Workloads on Three Generations of IBM PowerPC Microarchitectures”, IBM Center for Advanced Studies Conference, Feb 2001.
53. Mike Clark, Ajaya Durg, Kevin Lienenbrugger, and Lizy John, “Evaluation of TPC-H benchmark on Athlon based systems”, Fourth Workshop on Computer Architecture Evaluation using Commercial Workloads, Monterrey, Mexico, Jan 21st, 2001.
54. Yue Luo and Lizy K. John, “Performance Impact of Multithreaded Java Server Applications”, Fourth Workshop on Computer Architecture Evaluation using Commercial Workloads, Monterrey, Mexico, Jan 21st, 2001.
55. M. Valluri and L. John, “Is Compiling for Performance == Compiling for Power?” The 5th Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT-5), Monterrey, Mexico, Jan 20, 2001.
56. L. K. John, J. Rubio, “Effectiveness of Out of Order Scheduling in the IBM PowerPC Processors”, IBM Center for Advanced Studies Inaugural Conference, July 2000.
57. P. Sheshadri and L. K. John, “Characterization of Web Server Workloads on Three Generations of IBM PowerPC Microarchitectures”, IBM Center for Advanced Studies Inaugural Conference, July 2000.
58. R. Radhakrishnan and L. K. John, “A Decoupled Translate Execute (DTE) Architecture to Improve Performance of Java Execution", Workshop on Hardware Support for Objects and Microarchitectures for Java, Held in conjunction with the International Conference on Computer Design (ICCD) 1999, Oct 10, 1999, pp. 25-29.
59. R. Radhakrishnan and L. K. John, “Web Workload Characterization at a Microarchitectural Level”, Workshop on Commercial Workload Characterization, Held In Conjunction with the 1999 High Performance Computer Architecture Symposium, Jan 1999.
60. R. Bhargava, R. Radhakrishnan, B. L. Evans, and L. K. John, “Characterization of MMX-Enhanced DSP and Multimedia Applications on a General Purpose Processor”, Digest of the Workshop on Performance Analysis and its Impact on Design (held in conjunction with ISCA 98), June 1998, pp. 16-23.
61. R. Radhakrishnan, D. Tang and L. John, “Understanding the Branch Performance of Object Oriented Workloads”, Digest of the Workshop on Performance Analysis and its Impact on Design (held in conjunction with ISCA 98), June 1998.

62. L. K. John, "The Undergraduate Curriculum in the Electrical and Computer Engineering Department at the University of Texas at Austin", Digest of the Workshop on Computer Architecture Education (held in conjunction with ISCA 98), June 1998.
63. L. Nguyen, T. Nguyen, L. K. John and S. Srivatsan, "FPGA Model of MIPS R2000 CPU", Proceedings of ASEE-GSW conference, March 1998, pp. 55-60. This paper won the best paper award at the conference.
64. A. Dewhirst, D. Nguyen, H. Tran, L. John and S. Srivatsan, "VHDL Model of MIPS R2000 CPU", Proceedings of ASEE-GSW conference, March 1998, pp. 51-55.
65. L. John, "Experience Teaching a Senior Level Course on Digital Design Using FPGAs", Proceedings of IEEE International Conference on Microelectronic Systems Education (MSE 97), Crystal City, Virginia, July 1997, pp. 97-98.
66. L. John and R. Radhakrishnan, "c_ICE: A Compiler-based Instruction Cache Exclusion Scheme", Proceedings of the Workshop on Interaction between Compilers and Computer Architecture, held in connection with HPCA Symposium, Feb 1997.
67. L. Kurian, Paul T. Hulina, and Lee D. Coraor, "Expected and Obtained Performance from Decoupled Architectures", Supercomputing Conference, Nov 1992.
68. L. Kurian, Paul T. Hulina and Lee D. Coraor, "Role of an Access Processor in a RISC Environment", Poster Session of the ACM International Supercomputing conference, Minneapolis, MN, Nov 1992.

D. Books, Chapters of Books; Editor of Books (identify whether author or editor????)

Book Authored:

1. Digital Systems Design Using VHDL, Charles Roth and Lizy K. John, 3rd edition (Cengage Publishers, 2017, 628 pages)
2. Digital Systems Design Using Verilog, Charles Roth, Lizy K. John, and Byeong Kil Lee, Cengage Publishers, 2014, 581 pages)
3. Digital Systems Design Using VHDL, Charles Roth and Lizy K. John, 2nd edition (Thompson Engineering, 2006-2007, 580 pages)

Books Edited:

1. Computer Performance Evaluation and Benchmarking, L. John and L. Eeckhout, CRC Press, 2005 (289 pages)
2. Workload Characterization of Emerging Computer Applications, Kluwer Academic Publishers, 2001, ISBN 0-7923-7315-4
3. Workload Characterization for Computer System design, edited by L. K. John and A. M. Maynard, Kluwer Academic Publishers, 2000, 209 pages, ISBN 0-7923-7777-x.
4. Workload Characterization: Methodology and Case Studies, edited by L. John and A. M. Maynard, IEEE Computer Society, 153 pages, ISBN 0-7695-0452-3

Book Chapters:

1. Lloyd Bircher and Lizy K. John, Measurement Based Power Phase Analysis, Chapter 7, Unique Chips and Systems, Taylor and Francis, 2007
2. Brian Gaide and Lizy K. John, A High-Throughput Self-Timed FPGA Core Architecture, Chapter 5, Unique Chips and Systems, Taylor and Francis, 2007
3. Chapter 1, Performance Evaluation Methodology, Computer Performance Evaluation and Benchmarking, CRC Press, 2005 (coauthor with Lieven Eeckhout)
4. Chapter 2, Performance Evaluation Methodology, Computer Performance Evaluation and Benchmarking, CRC Press, 2005 (sole author)

5. Chapter 3, Benchmarks, Computer Performance Evaluation and Benchmarking, CRC Press, 2005 (sole author)
6. Chapter 4, Aggregating Performance over a Benchmark Suite, Computer Performance Evaluation and Benchmarking, CRC Press, 2005 (sole author)
7. Ramesh Radhakrishnan, Lizy John, Ravi Bhargava, and Deepu Talla, Improving Java performance in embedded and general-purpose processors, Java Microarchitectures (Chapter 5), edited by N. Vijaykrishnan and M. Wolczko, pp. 79-104, Kluwer Academic Publishers, 2002
8. Lizy K. John, Article on Performance Evaluation, in Computer Engineering Handbook (Invited) (Sole Author)
9. M. Valluri and L. John, "Is Compiling for Performance == Compiling for Power?", Chapter 6, in Interaction between Compilers and Computer Architectures, edited by Gyunggho Lee and Pen-Chung Yew, Kluwer Academic Publishers, 2001, ISBN 0-7923-7370-7
10. Tao Li, Lizy K. John, N. Vijaykrishnan, and A. Sivasubramaniam, Characterizing Operating System Activity in SPECjvm98 Benchmarks, Book Chapter in Characterization of Contemporary Workloads, pages 53-82, Kluwer Academic Publishers, 2001, ISBN 0-7923-7315-4
11. R. Bhargava, J. Rubio, S. Kannan, L. K. John, D. Christie, and L. Klaes, "Understanding the Impact of x86/NT Computing on Microarchitecture", Book Chapter in Characterization of Contemporary Workloads, pages 203- 228, Kluwer Academic Publishers, 2001, ISBN 0-7923-7315-4
12. Article on Harvard Architecture, in the EE Encyclopedia, John Wiley and Sons, 2000 (Invited Article) (sole author)
13. Article on Bus Architectures, The Encyclopedia of Life Support Systems, UNESCO project (Invited Article) (sole author)
14. Workload Characterization: Motivation, Goals and Methodology, pages 3-14, in Workload Characterization: Methodology and Case Studies, edited by L. John and A. Maynard, IEEE Computer Society, ISBN 0-7695-0452-3
15. Article on Bit-Slice Computers, in the EE Encyclopedia, John Wiley and Sons, 1999 (Invited Article), pp. 39-44 ISBN 0471-35895-9 (sole author)
16. Classification and Performance Evaluation of Instruction Buffering Techniques, in Performance Modeling for Computer Architects, edited by C. M. Krishna, IEEE Computer Society Press. Pages 94-103. ISBN 0-8186-7094-0

*E. Reviews

*F. Technical Reports

1. Shuang Song, Q. Wu, S. Flolid, J. Dean, R. Panda, and Lizy K. John, Experiments with CPU 2017, Technical Report TR-180515-01, LCA, Department of ECE, UT Austin, Available on arxiv
2. Ajay Joshi, Aashish Phansalkar, Lieven Eeckhout, and Lizy John, “Measuring Benchmark Similarity Using Inherent Program Characteristics, Technical Report TR-060201-0, Feb 2006.
3. Yue Luo and Lizy John, “Simulating Java Commercial Throughput Workload: A Case Study”, Technical Report TR-050710-01. July 2005.
4. Yue Luo, Ajay Joshi, Aashish Phansalkar, Lizy John, and Joydeep Ghosh, “Analyzing and Improving Clustering Based Sampling for Microprocessor Simulation”, Technical Report TR-050301-01. March 2005.
5. Aashish Phansalkar, Ajay Joshi, Lieven Eeckhout, and Lizy K. John, “Measuring Program Similarity”, Technical Report TR-050127-01, Laboratory for Computer Architecture, The University of Texas at Austin, Jan 2005.
6. W. L. Bircher, J. Law, M. Valluri and Lizy K. John, “Effective Use of Performance Monitoring Counters for Run-Time Prediction of Power”, Technical Report TR-041104-01, Laboratory for Computer Architecture, The University of Texas at Austin, Nov 2004.

7. Aashish Phansalkar, Ajay Joshi, Lieven Eeckhout, and Lizy K. John, “Four Generations of SPEC CPU Benchmarks: What has changed and what has not”, Technical Report TR-041026-01-1, Laboratory for Computer Architecture, The University of Texas at Austin, Oct 2004.
8. Robert H. Bell, Jr., and Lizy K. John, “Experiments in Automatic Benchmark Synthesis”, Technical Report TR-040817-01, Laboratory for Computer Architecture, The University of Texas at Austin, Aug 2004.
9. Yue Luo and Lizy K. John, “Using Statistical Theory to Study Issues in Microprocessor Simulation”, Technical Report TR-0400225-01, Laboratory for Computer Architecture, The University of Texas at Austin, Feb 2004.
10. Lizy K. John,” More on finding a Single Number to indicate Overall Performance of a Benchmark Suite”, Technical Report TR-040126-01, Laboratory for Computer Architecture, The University of Texas at Austin, Jan 2004.
11. Aashish Phansalkar and Lizy Kurian John, “Analyzing Program Behavior of SPECint2000 Benchmark Suite using Principal Components Analysis”, Technical Report TR-040122-01, Laboratory for Computer Architecture, The University of Texas at Austin, Jan 2004.
12. Ajay Joshi, Srirarm Sambamurthy, Saket Kumar, and Lizy John, “Power Modeling in SDRAMs”, Technical Report TR-040126-02, Jan 2004.
13. Robert H. Bell, Jr. and Lizy Kurian John, “Basic Block Simulation Granularity, Basic Block Maps, and Benchmark Synthesis Using Statistical Simulation”, Technical Report TR-031119-01, Laboratory for Computer Architecture, The University of Texas at Austin, Nov 2003.
14. Byeong Kil Lee and Lizy John, “Development and Characterization of Control-Plane Network Workloads”, Aug 2003
15. Juan Rubio and Lizy K. John, “Using Simulated Annealing to Guide Server Data Placement”, Technical Report TR-030731-01, Laboratory for Computer Architecture, The University of Texas at Austin, July 2003.
16. Shiwen Hu and Lizy K. John, “Avoiding Store Misses to Fully Modified Cache Blocks”, Technical Report TR-030701-01, Laboratory for Computer Architecture, The University of Texas at Austin, July 2003.
17. Ravi Bhargava and Lizy K. John, “Cluster Assignment Strategies for a Clustered Trace Cache Processor”, Technical Report TR-030331-01, Laboratory for Computer Architecture, The University of Texas at Austin, March 2003.
18. Tao Li and Lizy John, “Run-time Modeling and Estimation of Operating System Power Consumption”, Technical Report TR-1101-02, Laboratory for Computer Architecture, The University of Texas at Austin, Nov 2002.
19. Shiwen Hu, Ravi Bhargava and Lizy Kurian John, “The Role of Return Value Prediction in Exploiting Speculative Method-Level Parallelism”, Technical Report TR-020822-02, Laboratory for Computer Architecture, The University of Texas at Austin, Aug 2002.
20. Anand S. Rajan, Juan Rubio and Lizy K. John, “Cache Performance in Java Virtual Machines: A Study of Constituent Phases”, Technical Report TR-020822-01, Laboratory for Computer Architecture, The University of Texas at Austin, Aug 2002.
21. Jason Law and Byeong Kil Lee, “Access Time and Power Characteristics of Various Future File Configurations”, Technical Report TR-020821-01, Laboratory for Computer Architecture, The University of Texas at Austin, Aug 2002.
22. Yue Luo, Pattabi Seshadri, Juan Rubio, Lizy John and Alex Mericas, “A Case Study of 3 Internet Benchmarks on 3 Superscalar Machines”, Technical Report TR-020817-01, Laboratory for Computer Architecture, The University of Texas at Austin, Aug 2002.
23. Juan Rubio, Madhavi Valluri and Lizy John, “Improving Transaction Processing using a Hierarchical Computing Server”, Technical Report TR-020719-01, Laboratory for Computer Architecture, The University of Texas at Austin, July 2002.
24. Madhavi Gopal Valluri and Lizy John, “A Hybrid-Scheduling Approach for Low-Energy Superscalar Processors”, Technical Report TR-020617-01, Laboratory for Computer Architecture, The University of Texas at Austin, June 2002.
25. Eugene B. John, Stefan Petko, Lizy John and Jason Law, “Access Time and Energy Tradeoffs for Caches in High Frequency Microprocessors”, Technical Report TR-020607-01, Laboratory for Computer Architecture, The University of Texas at Austin, June 2002.

26. Tao Li, Lizy John, Anand Sivasubramaniam and Vijaykrishnan Narayanan, "Understanding and Improving Operating System Effects in Control Flow Prediction", Technical Report TR-000630-02, Laboratory for Computer Architecture, The University of Texas at Austin, June 2002.
27. Ravi Bhargava, Juan Rubio and Lizy John, "Traveling Speculations: An Integrated Prediction Strategy for Wide-Issue Microprocessors", Technical Report TR-020524-01, Laboratory for Computer Architecture, The University of Texas at Austin, May 2002.
28. Ravi Bhargava and Lizy John, "Value Prediction Design for High-Frequency Microprocessors", Technical Report TR-020508-01, Laboratory for Computer Architecture, The University of Texas at Austin, May 2002.
29. Byeong Kil Lee and Lizy John, "Implications of Programmable General Purpose Processors for Compression/Encryption Applications", Technical Report LCA-TR-020315, Laboratory for Computer Architecture, The University of Texas at Austin, 2002.
30. Deepu Talla, Lizy John, and Doug Burger, "Hardware support to reduce overhead in fine-grain media codes", Technical Report LCA-TR-011101, Laboratory for Computer Architecture, The University of Texas, Austin, Nov 2001.
31. Yue Luo and Lizy John, "Workload Characterization of Multithreaded Java Servers", Technical Report TR-010815-01, Laboratory for Computer Architecture, The University of Texas at Austin, Aug 2001.
32. Juan Rubio and Lizy John, "Hierarchical Computing: An Architecture for Efficient Transaction Processing", Technical Report UT-CERC-TR-01-1, Computer Engineering Research Center, The University of Texas at Austin, Jan 29, 2001.
33. Ramesh Radhakrishnan, Juan Rubio, N. Vijaykrishnan and Lizy John, "Execution Characteristics of JIT Compilers", Technical Report TR-990717-01, Laboratory for Computer Architecture, The University of Texas at Austin.
34. Ravi Bhargava, Lizy John, and Francisco Matus, "Exploiting Instruction Reuse to Enhance Microprocessor Simulation", Technical Report TR-981223-01, Laboratory for Computer Architecture, The University of Texas at Austin, Dec 1998.
35. Sanjeev Ghai, Jody Joyner, and Lizy K. John, "Investigating the Effectiveness of a Third Level Cache", Technical Report TR-980501-01, May 1998.

***ORAL PRESENTATIONS:** (List co-authors, title of presentation, where given, and dates)

1. **Keynote Speech**, IEEE Women In Engineering International Leadership Summit (WIE ILS), Kochi, India, Sept 8, 2018
2. Invited talk, Approximate Techniques for Performance and Power Modeling/Prediction MODSIM 2018, Washington, Seattle, Aug 16, 2018
3. Panelist, "Modeling and Simulation for Extreme Heterogeneity", MODSIM 2018, Seattle, Aug 17, 2018.
4. Seminar, Approximate Techniques for Performance and Power Modeling/Prediction, MIT, May 29, 2018
5. Computer Science Colloquium, Approximate Techniques for Performance and Power Modeling/Prediction, William and Mary University, Virginia, Apr 20, 2018
6. **Invited Speech, Industry-Academia Partnership**, UT Cloud Workshop, Computing In Situ and In Transit, Nov 10, 2017
7. Invited Speech, IEEE SPICES 2017, Machine Learning for Performance and Power Modeling/Prediction, Aug 10, 2017
8. **Keynote Speech**, IEEE Min-Move Workshop held with IEEE Parallel Architectures and Compilation Conference (PACT), Computing In-Situ and In-Transit, Sept 2017
9. **Keynote Speech**, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS Conference, Machine Learning for Performance and Power Modeling/Prediction, April 2017, San Francisco, California

10. Adaptive Energy-Efficient Designs for Next Generation Smart Phone CPUs, Samsung Austin Research Center, Feb 3, 2017
11. Computer Architecture, Memory Systems, Performance and Power Optimizations, Speech to USPTO Visitors, April 2017
12. Seminar, "Machine Learning for Power Modeling and Prediction", Polytecnico Milan, July 8, 2016
13. 2015 Samsung SARC Technical Forum Invited Speech, "Machine Learning for Power Modeling and Prediction", Austin, Texas, October 8, 2015
14. Colloquia, "Machine Learning for Performance and Power Modeling", Indian Institute of Science, January 9, 2016
15. Invited Talk, "Workload Characterization for Big Data Computing", Intel, Bangalore, January 9, 2016
16. Invited Talk, ARM, "Machine Learning for Performance and Power Modeling", Bangalore, January 7, 2016
17. Invited Talk, IBM Watson Research Center, Yorktown Heights, New York, "Big Data Workloads, An Architect's perspective ", Invited by: Michael Healy, Sep 14, 2015
18. Invited Talk, "Big Data Workloads, A Computer Architect's perspective", AMD, Austin, Texas, April 6, 2015
19. Invited Talk, Computer Science Department Colloquium, "Big Data Workloads, A Computer Architect's perspective" Baylor University, May 1, 2015
20. Invited Speech, "Workload Characterization for Big Data Computing", Shannon Lab, Huawei, May 21, 2015.
21. **Keynote Speech,** Many Big, Many Little: Who will crunch all the Big Data?, Huawei Strategic Workshop, May 19, 2015, Shenzhen, China.
22. Huawei, China, Cloud and Big Data Workload Characterization: Challenges and Opportunities, June 23, 2014.
23. Shenzhen Institute of Advanced technology, Chinese Academy of Sciences, Shenzhen, Cloud and Big Data Workload Characterization: Challenges and Opportunities, June 24, 2014
24. Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences, Shenzhen, Multicore System Design and Optimization, June 25, 2014.
25. Chinese Academy of Sciences, Beijing, June 27, 2014, Multicore System Design and Optimization
26. **Keynote Speech**, Big Data and Cloud Workloads: An Architect's Perspective, BPOE Workshop in conjunction with ACM ASPLOS, Salt Lake City, Utah, 2014
27. **Invited Speech**, Performance Evaluation for Large Scale Systems: Closed Loop Control with Appropriate Metrics, ACM Supercomputing Conference (SC 2013), Nov 2013 (Host: Bill Kramer, UIUC)
28. SRC India Design Review, Bangalore India, Jan 10, 2014
29. "Multicore System Design and Optimization", Talk given to UT graduate Students, Sept 27, 2013
30. SRC Annual review Presentation, Portland Oregon, May 3, 2013
31. Georgia Tech, Performance Verification for Complex Chips: Role of Workload Proxies, April 2012
32. Presentation to Lockheed Martin, Hardware Software Co-design for Proprietary Systems, March 27, 2012
33. Texas A&M Seminar, Multicore System Design and Optimization: November 2011
34. **Keynote Speech**, ACM International Conference on Performance Engineering (ICPE), March 14, 2011, Karlsruhe, Germany

35. Workload Synthesis for a Communications SoC, Invited talk at the Workshop on SoC Architectures, Accelerators and Workloads (SAW) organized by Ravi Iyer (Intel) in conjunction with HPCA, February 12, 2011, San Antonio
36. SRC Annual Review Presentation, March 2011
37. Lawrence Livermore National Lab, Jan 11, 2011
38. Talk at Freescale Meeting, December 2010
39. "Multicore System Design and Optimization", UT Day at AMD, Aug 20, 2010
40. "Synthetic Benchmark Generation Framework for System Level Max Power Virus Generation and Performance Cloning", SRC Annual Review Presentation, CMU, April 27, 2010 "
41. "Why consider graduate School", Presentation to Honors Students and their parents, April 22, 2010
42. "LCA Research in Computer Architecture, Performance Evaluation and Workload Characterization", April 7, 2010, Presented at AMD Day at UT,
43. "Automatic Benchmark Synthesis: The Return of Synthetic Benchmarks", Colloquium, Computer Science Department, University of Pittsburg, April 26, 2010
44. Automatic Benchmark Synthesis for Validation of Performance and Power Modeling of High Performance Processors, Computer Science and Engineering Department Colloquium Penn State, March 2010.
45. SRC Annual Review, Stanford, CA, March 2009
46. "Effective Computer System Design using Workload Characterization", Texas A & M University Computer Science Seminar, November 3, 2008
47. Tech Area Night Presentation, Embedded Systems Area, April 2008, ECE Department
48. "Chip Design", Camp Texas, Aug 21, 2008
49. "Workload Characterization for Effective Computer System Design", Computer Science Colloquium, The University of Texas at El Paso, Apr 18, 2008
50. "Graduate School: How to Enter and Succeed", Talk given to IEEE Meeting, The University of Texas at El Paso, Apr 18, 2008.
51. **Keynote Speech**, "Performance Evaluation and Benchmarking: The Return of Synthetic Benchmarks", IBM Center for Advanced Studies (CAS) Conference, Feb 22, 2008
52. LCA Research in Computer Architecture, Performance Evaluation and Workload Characterization, Talk given to Sun Microsystems Open Sparc Initiative, January 29, 2008
53. Performance Evaluation and Benchmarking, Talk given at UT@IBM: Building Collaboration, Creating Impact, Nov 5, 2007
54. LCA Research in Computer Architecture, Performance Evaluation and Workload Characterization, Aug 28, 2007, Computer Architecture Industry Affiliates
55. Computer System Design and Technology, Camp Texas, Aug 20, 2007
56. CRA-W/CDC Programming Languages Summer School, CS Department, UT Austin, "What Programming Language Researchers should know about Computer Architecture", May 11, 2007
57. CRA-W/CDC Computer Architecture Summer Workshop, How to get started in Computer Architecture Research, Princeton, July 19 2006
58. SPEC Annual Meeting, "Use of Clustering in Benchmark Selection", Sunnyvale, CA, Jan 2005.
59. Hewlett Packard, "Workload Characterization for Computer System Design and Evaluation", June 15, 2004
60. University of Texas MITE Program "Electrical and Computer Engineering", June 7 2004
61. Lizy John, "Panelist at ISPASS Panel", Austin, TX, April 2004.

62. **Keynote speech,** "Workload Characterization: Can it save Computer Architecture and Performance Evaluation", Workshop on Commercial Workload Characterization, Madrid, Spain, Feb 15, 2004.
63. The University of Texas at Austin, ECE Department Graduate Student Orientation, "Life in Graduate School", Aug 2003
64. The University of Texas at Austin, College of Engineering Honors Program, "Workload Characterization for Computer System Design", Sept 14, 2002
65. The University of Texas at Austin, ECE Department Graduate Student Orientation, "Areas in Computer Engineering", Aug 2001
66. The University of Texas at Austin, Women in Engineering Program, "Designing with Field Programmable Gate Arrays", July 26, 2001
67. The University of Texas at Austin Honors Colloquium, "Design of Microprocessors", July 27, 2001.
68. The International Conference on Supercomputing (ICS) 2001, "Improving Java Performance using Hardware Translation", Italy, June 2001.
69. Fourth Workshop on Computer Architecture Evaluation using Commercial Workloads, "Evaluation of TPC-H benchmark on Athlon based systems", Monterrey, Mexico, Jan 21st, 2001.
70. Fourth Workshop on Computer Architecture Evaluation using Commercial Workloads, "Performance Impact of Multithreaded Java Server Applications", Monterrey, Mexico, Jan 21st, 2001.
71. The 5th Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT-5), "Is Compiling for Performance == Compiling for Power?" Monterrey, Mexico, Jan 20, 2001.
72. IEEE Workshop on Hardware Support for Objects and Microarchitectures for Java, Invited Talk, "Understanding, Exploiting and Improving Java Run Time Systems", Sept 17, 2000.
73. Tivoli Corporation, Austin, "Characterizing, Understanding and Exploiting E-business workloads", Aug 21, 2000.
74. The University of Texas at Austin Honors Colloquium, "Design of Microprocessors", July 22, 2000.
75. IBM Center for Advanced Studies (CAS) Conference, IBM Austin, "Effectiveness of Out of Order Scheduling on Three Generations of IBM PowerPC Processors", July 19, 2000.
76. Singapore National University, "Architectural Support for Java Run Time Systems", Seminar in the Computer Science Department and Parallel Processing Laboratory, June 14, 2000
77. Nanyang Technological University, Singapore, "Architectural Support for Java Run Time Systems", Seminar in the Electrical Engineering Department, June 13, 2000.
78. Intel, Austin, "Architectural Support for Java Run Time Systems", Seminar at the Intel Texas Design Center, May 10, 2000.
79. University of Illinois, Urbana Champaign, "Understanding, Exploiting and Improving Java Run Time Systems", Electrical and Computer Engineering Seminar, May 1, 2000.
80. The Pennsylvania State University, Computer Science and Engineering Department Colloquium, "Understanding, Exploiting and Improving Java Run Time Systems", March 16, 2000.
81. Carnegie Mellon University, ECE Seminar, "Architectural Support for Java Run Time Systems", March 15, 2000.
82. University of Paris Sud, France, Computer Science Seminar, "Architectural Support for Java Run Time Systems", Jan 13, 2000.
83. High Performance Computer Architecture (HPCA) 2000, "Architectural Support for Java Run Time Systems", Toulouse France, Jan 12, 2000.
84. Presentation before Technical Committee on Computer Architecture "HPCA 2002- Why Austin", Toulouse, France, Jan 10, 2000.
85. The University of Texas Honors Colloquium, July 1999, "Design of Microprocessors"

86. IEEE International Conference on Computer Design, “Code Coalescing Unit: A Mechanism to facilitate Load Store Data Communication”, Oct 1998.
87. College of Engineering UT Austin, EFAC Council Spouse meeting, Presentation title “Research in High Performance Computer Architecture at the Laboratory for Computer Architecture”, Fall 1998 EFAC.
88. Workshop on Performance Analysis and its Impact on Design (held in conjunction with ISCA 98), “Characterization of MMX-Enhanced DSP and Multimedia Applications on a General Purpose Processor”, June 1998.
89. Workshop on Computer Architecture Education (held in conjunction with ISCA 98), “The Undergraduate Curriculum in the Electrical and Computer Engineering Department at the University of Texas at Austin”, June 1998.
90. Hawaii International Conference on System Sciences, “A Scalable Optoelectronic Interconnection Network for Parallel Computing”, Jan 1998.
91. IEEE International Conference on Computer Design, “Design and Performance Evaluation of a Cache Assist to implement Selective Caching”, Oct 1997.
92. IBM Austin Innovation Series presentation, Half-day seminar “Improving Memory Access Performance of Programs”, Aug 1997.
93. Presentation at the Workshop on Integrating Design and Design Automation into the Undergraduate Computer Science Curriculum, Tampa, FL, Aug 1997.
94. Half-day Tutorial on Rapid Prototyping using FPGAs, presented at Microelectronics Systems Education (MSE) 1997, Crystal City, VA, July 1997.
95. Research in Computer Architecture in the ECE Department, Presentation before the ECE Visiting Committee, May 1997.
96. 1996 IEEE VLSI Workshop, “A Decoupled Architecture with a CISC-style Access Processor and a RISC-style Execute Processor”, Clearwater, FL, Nov 1996.
97. IEEE Symposium on Parallel and Distributed Processing, “Improving the Parallelism and Concurrency in Decoupled Access/Execute Architectures”, New Orleans, LA, Oct 1996.
98. Presentation at the Workshop on Integrating Design and Design Automation into the Undergraduate Computer Science Curriculum, Tampa, FL, Aug 1996.
99. North Carolina State University, Electrical Engineering Department, “Improving Memory Access Performance of Programs”, June 1996.
100. University of Texas at Austin, Electrical and Computer Engineering Department, “Improving Memory Access Performance of Programs”, May 1996.
101. Ohio State University, Electrical Engineering Department, “Improving Memory Access Performance of Programs”, May 1996.
102. Characterization of Media Workloads: The University of Texas at Austin Digital Signal Processing Seminar, April 12, 1996.
103. University of Maryland, College Park, Electrical Engineering Department, “Improving Memory Access Performance of Programs”, April 1996.
104. University of North Carolina Chapel Hill, Computer Science Department, “Improving Memory Access Performance of Programs”, Apr 1996.
105. The Pennsylvania State University, Computer Science and Engineering Department Colloquium, “Improving Memory Access Performance of Programs”, March 1996.
106. University of Connecticut, Electrical Engineering Department, “Improving Memory Access Performance of Programs”, March 1996.
107. Tufts University, Electrical Engineering Department, “Improving Memory Access Performance of Programs”, March 1996.

108. Ohio University, Electrical Engineering Department, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, Jan 1996.
109. Catholic University, Washington D. C., Electrical Engineering Department, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, Jan 1996.
110. University of North Texas, June 1996, “Improving Memory Access Performance of Programs”
111. Johns Hopkins University, Electrical Engineering Department, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, Jan 1996.
112. Arizona State University, Electrical Engineering and Technology, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, 1995.
113. Kansas State University, Electrical Engineering Department, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, 1995.
114. University of Delaware, Electrical Engineering Department, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, Jan 1995.
115. International Conference on VLSI Design (IEEE) “Design of a Highly Reconfigurable Interconnect for Array Processors”, Jan 1995.
116. The International Symposium on High Performance Computer Architecture (HPCA-1), “Program Balance and its Impact on High Performance Architectures”, Jan 1995.
117. IEEE International Conference on Parallel Processing, “Module Partitioning and Interlaced Data Placement Schemes to Reduce Conflicts in Interleaved Memories", Aug 1994.
118. University of Kentucky, Electrical Engineering Department, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, Summer 1994.
119. IEEE Tampa Chapter, “Rapid Prototyping Using Field Programmable Gate Arrays”, Jan 1994.
120. University of South Florida, ACM Chapter, December 1993, “Research in Computer Architecture”
121. University of South Florida, Computer Science and Engineering Department, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, Jan 1993.
122. IBM Vermont, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, Dec 1992.
123. ACM/IEEE International Symposium on Computer Architecture (ISCA 92), “Memory Latency Effects in Decoupled Architectures”, Goldcoast Australia, May 1992.

PATENTS: 10 US patents granted; 4 pending

1. U. S. Patent 9,235,397, Method and Apparatus for increasing task execution speed, January 12, 2016
2. U. S. Patent 9,038,039, Apparatus and Method for Accelerating Java Translation, May 19, 2015
3. U. S. Patent 8,359,597, “Workload-guided application scheduling in multi-core system based atleast on application branch transition rates, Jan 22, 2013
4. US Patent 8,250,350, “Computer System with non-volatile write-protected memory based operating system and secure system architecture, Aug 21, 2012
5. US Patent 8,230,407, “Apparatus and method for accelerating Java translation”, July 24, 2012
6. US Patent 8,214,629, Computer system with secure instantly available applications using non-volatile write-protected memory”, July 3, 2012
7. US patent 8,041,931, “Branch prediction apparatus, systems, and methods”, Granted Oct 18, 2011 (Patent has been licensed by UT)
8. U S Patent 7,370,183,”Branch Predictor comprising a split branch history shift register”. Patent has been licensed by UT.

9. U S Patent 7,107, 434, " System, Method and Apparatus for Allocating Hardware Resources using Pseudo Random Sequences". Patent has been licensed by UT
10. U S Patent 5,867,422 " Computer Memory Chip with field Programmable Memory Cell Arrays", Granted Feb 1999.
11. Patent Application filed in Korea, Japan and China - FE-200703-016-1-US0 - Method and Apparatus to save Java bytecode translations as blocks rather than per bytecode in an external (off processor) Java accelerator hardware
12. Patent Application filed in Korea and being filed in US, Japan and China - FE-200703-017-1-US0 - Method and Apparatus to Perform Embedding of Constants into Native Instructions
13. Provisional U. S Patent Application, Automatically Generating Microprocessor Benchmarks to Generate Maximum Power Consumption and Operating Temperature, August 2008, Application No. 61088252
14. Method and Apparatus to Automatically Generate Representative Training-sets for Supervised Machine Learning Models, UT Tech ID 6928 JOH (Cover provisional filed with patent office by UT). (with Reena Panda)
15. Improved Methodology for Load Balancing of Graph Workloads UT Tech ID 6902 JOH (Cover provisional filed with patent office by UT). (with Shuang Song)
16. PROCESSOR USING A LEVEL 3 TRANSLATION LOOKASIDE BUFFER IMPLEMENTED IN OFF-CHIP OR DIE-STACKED DYNAMIC RANDOM-ACCESS MEMORY (7010 JOH)
17. Intelligently Partitioning Data Cache to Allocate Space for Translation Entries, Patent filed by UT (with Yashwant Marathe, Jee Ho Ryoo, Nagendra Gulur) (7166 JOH)
18. Bloom Filters for Testing, Disclosure 2009 August

GRANTS AND CONTRACTS: (Co-principal investigators (if any), title of grant, sponsoring agency, total dollar value, beginning and ending dates)

Co-Investigators	Title	Agency	Grant Total	Grant Period

w/Gerstlauer and Brisk	Predictive Modeling for Next Generation Heterogeneous System Design	NSF	$1 Mil ($337K)	10/18-09/21
w/Gerstlauer	Learning Based Thermal Modeling	Samsung GRO	$99K	10/18-09/19
Sole	Improving Research Reproducibility using Proxy benchmarks	NSF	$200K	09/17-08/19
w/Gertlauer and Biros	Computing In Situ and In Transit for Hierarchical Numerical Algorithms	NSF	$800K	09/17-08/20
w/Gerstlauer	Miniaturized Proxies of Industry Standard Benchmarks for Pre-silicon Evaluation	Intel Corp	$160,000	01/17-01/19
Sole	Trace Snippets for RTL Power Modeling	Samsung	$99,990	12/16-
w/Gerstlauer	Power-Aware System Compilation	Intel	$100,000	12/17
Sole	A Methodology to Identify Application Memory Access Patterns for Efficient Hierarchical Memory Subsystem	Oracle Corporation	$97,283	6/15-5/16
w/Gerstlauer	Big Data Workloads, A Computer Architect's perspective	Samsung GRO	$99,985	01/16-06/18
w/Gerstlauer	Scalable Network/System Co-Simulation For Power and Performance Aware Network of Systems Design	Samsung GRO	$99,985	09/15-08/16
Sole	Big Data Workload Energy Characterization	Huawei	$110,000	6/14-5/15
Sole	A Methodology to Generate Miniature Proxies for Database workloads	Oracle	$60,000	6/14-5/15 1/14-12/16
Sole	Workload characterization for Big Data	SRC	$240,000	9/13-8/16
w/Biros, Gerstlauer, vandeGeijn	XPS: Algorithms and Architectures for Multiresolution Applications	NSF	$749,801 ($224K-my share)	9/13-8/15
w/Gerstlauer	Power-Aware System Compilation	Intel	200,000	10/13-9/15
Sole	Decomposition of Large Data Analytics into Hierarchical Models	AMD	50,000	6/13-5/15
Sole	A Methodology to Identify Application Memory Access Patterns for Efficient Hierarchical Caching	Oracle	60,000	6/13-5/14
w/Janapa Reddi	SHF: Sustainable and Reliable Multicore and Many-Core Computing via Cross-Layer Solutions	NSF	300,000	09/12-08/15
w/Gerstlauer	Multi-dimensional Modeling, Design and Exploration of Multi-core SoCs,	SRC	345,000	05/12-04/15
None	Automatic Generation of Multicore Proxy Workloads and Stressmarks	AMD	50,000	04/12-03/13
None	Multicore Stressmarks	AMD	50,000	05/11-04/12
None	SHF: Small: Workload Characterization and Benchmark Synthesis for Emerging Computing Systems	NSF	425,000	09/11-08/14
None	Stress-testing Multicore Processors for Worst-Case Power Consumption and Voltage Emergencies	AMD	50,000	08/10-08/11
Dan Tamir, Apan Qasem	Power Consumption Based Multicore Task Scheduling and Load Balancing	SRC	360,000 (my share: 175,500)	04/11-03/14

None	Intel Corporation Product Donation for EE316 Logic Design Lab, June, 2009,	Intel	34,361	2009 June
None	Performance Cloning for Dissemination of Proprietary Applications to Hardware Vendors	Lockheed Martin	100,000	2008-2009
None	Benchmark Synthesis for Performance and Power Modeling	Sun Microsystems	45,000	2008-2009
None	IBM Faculty Award	IBM	15,000	2008-2009
R. Figueiredo, etc	Collaborative Research Archer: Seeding a Community Based computing Infrastructure for Computer Architecture Research and Education	NSF	(my share 67,631)	2008-
None	Computer Architecture Research	AMD	8,000	Dec 07-Dec 08
None	Intel Equipment Grant for research	Intel	35,056	Sep 2008
Tao Li	Automatic Benchmark Synthesis for Validation of Performance and Power Models of High Performance Processors	SRC	330,000 (my share: 165,000)	04/08-03/11
None	Simplifying Performance Evaluation using Workload Characterization	NSF	300,000	09/07-08/11
None	Faculty Partnership Award	IBM	$25,000	06/07
None	Computer Architecture Research	AMD	$5000	11/06
None	CAS Award – Faculty Partnership Award	IBM	$7,500	06/06
None	Computer Architecture Research	AMD	$5000	11/05
None	Java Accelerators	Samsung	$128,000	2/05-8/06
None	CAS Award	IBM	$25,000	6/05
None	Statistical Techniques for Computer Performance Evaluation	NSF	$200,000	2004-2008
None	Computer Architecture Research	AMD	$5000	2/05
None	Performance Evaluation Research	IBM	$500	12/04
None	CAS project- Statistical Techniques in Performance Evaluation and Benchmarking	IBM	$25,000	7/04
None	Computer Architecture Research	Hewlett Packard	$800	6/04
None	Equipment Grant	Intel	$42,000 (approx.)	Spring 2004
None	Performance Impact of Emerging Workloads on Intel Processors	Intel	$35,000	March 2004
None	Research in Computer Architecture and Workload Characterization	AMD	$3,000	Dec 2003
None	IBM Faculty Partnership Award Project: Developing a Methodology for Predicting Characteristics of Future/Emerging Workloads	IBM	$25,000	June 2003
None	Performance Impact of Emerging Workloads on Intel Processors	Intel	$35,000	May 2003
	IBM SUR grant	IBM	$60,000 (approx.)	Fall 2002
None	IBM Faculty Partnership Award- Developing a Methodology for Predicting Characteristics of Future/Emerging Workloads	IBM	$25,000	June 2002
None	Equipment Support- Performance Impact of Emerging Workloads on Intel Processors	Intel	$10,000	Summer 2002
None	Research in Computer Architecture and Workload Characterization	AMD	$5,000	May 2002
None	Performance Impact of Emerging Workloads on Intel Processors	Intel	$35,000	March 2002

None	Intel Equipment (8-way server + 5 workstations)	Intel	$65,000 (approx.)	Spring 2002
None	Development and Characterization of Control-Plane Network Workloads	Motorola	$50,000	Jan 2002
None	Computer Architecture Research	AMD	$5,000	Dec 2001
	IBM SUR Grant	IBM	$100,00 (approx.)	Fall 2001
None	Designing Microprocessors and Computer Systems for Emerging Workloads	NSF	$265,000	2001-2004
	Intel Equipment (10 workstations)	Intel	$40,000 (approx.)	2000-2001
None	IBM Faculty Partnership Award- Effectiveness of Out of Order Microarchitectural techniques for web server workloads	IBM	$30,000	May 2001
None	UT Research Internship Program	Univ. of TX, at Austin	$15,500	2001-2002
	Computer Architecture Seminar Series	AMD	$15,000	
None	Understanding and Optimizing e-Business workloads and the underlying infrastructure	Tivoli	$30,000	Aug 2000
None	IBM Center for Advanced Studies Partnership Award- Effectiveness of Out of Order Microarchitectural Techniques for web server workloads	IBM	$25,000	March 2000
	Workshop on Workload Characterization 2000	AMD	$2,500	2000
None	Career Award- Improving the Access-Execute Balance and Concurrency in High Performance Processors	NSF	$315,000	1996-2000
None	UT Co-op Book Subvention Grant	Univ. of TX, at Austin	$2,500	Aug 1999
None	DELL-LARIAT grant- Characterization of Multimedia Application and Analysis of their Performance Impact	Dell	$32,127	July 1999
None	Workshop on Workload Characterization	Intel	$4,000	July 1999
None	Computer hardware grant- Characterization of Multimedia Workloads and Analysis of their Performance Impact	Intel	$4,181	July 1999
None	Software donation- Web Server Characterization Studies on the Pentium Platforms	Microsoft	$3,814	Jan 1999
None	Web Server Characterization Studies on the Pentium Platforms	Intel	$15,320	Dec 1998
None	UT research Internship Program	Univ. of TX, at Austin	$15,000	1998-1999
None	UT Endowed Lecturer Program	Univ. of TX, at Austin	$1,100	Spring 1998
None	Summer Research Assignment Award	Univ. of TX, at Austin	$11,000	Summer 1997
None	Junior faculty Enhancement Award	Oak Ridge Associated Universities	$5,000	1996-1997
None	Matching Award to Oak Ridge Junior Faculty Enhancement Award	UT Austin	$5,000	Fall 1996
None	Matching Award to NSF CAREER Equipment	UT Austin	$10,000	Fall 1996
None	Startup Grant	Univ. of TX, at Austin	$55,000	Fall 1996

None	Microprocessor Performance Evaluation System - Advanced Micro Devices (proprietary equipment given for UT research. Dollar equivalent not specified by AMD)	AMD	Not Specified	Dec 1997
S. Keckler, D. Burger, L. Alvisi, M.D. Dahlin, C. Lin, C.R. Moore, K. McKinley, and H. Vin	"TRIPS: The Tera-op Reliable Intelligently adaptive Processing System Implementation for Polymorphous Computing Architectures (PCA),"	Defense Advanced Research Projects Agency	$7,617,912 $100,000 (approx./ my share)	2003-2005
Steve Keckler, D. Burger, L. Alvisi, M.D. Dahlin, C. Lin, K. McKinley, and H. Vin	TRIPS: The Tera-op Reliable Intelligently adaptive Processing System	Defense Advanced Research Projects Agency	$3,027,48 $400,000 (approx./ my share)	6/01-5/03
Prof. E. Swartzlander and Prof. E. John	ATP Grant- High Performance MultiMedia Processors Principal Investigator	State of Texas Advanced Technology Program	$157,800 $72,806 (my share.)	1/00-12/01
Prof. C. Chase	Impact of Contemporary Programming Paradigms and Workloads Principal Investigator	NSF	$356,314 $256,314 (my share)	1998-2001
Prof. E. Swartzlander	ATP Grant- High Performance Digital Signal Processors Principal Investigator	State of Texas Advanced Technology Program	$134,640 80,784 (my share)	1/98-12/99
Prof. Yale Patt	Equipment Donation	Intel	$136,640	Nov 1999
Prof. Yale Patt	Software Donation	Microsoft	$61,039	Sept 1999
Prof. Evans	TMS320C62x Development Tools	Texas Instruments	Not Specified	1998
Prof. J. C. Browne of Computer Science, co-PIs: L. John, Prof. C. Chase and Prof. P. Teller at the University of Texas at El Paso	IBM- SUR Grant- End-to-End Measurement, Modeling and Simulation of Parallel/Distributed Computer Systems	IBM	$100,000	Oct 1997
Dr. Pete Maurer and Dr. N. Ranganathan of the University of South Florida, Tampa, Florida	NSF CISE Infrastructure Grant * This was an award to Univ. of S. Florida while Lizy John was faculty there. This grant was not transferred to UT, however, I continued to participate in the project until 1998	NSF	$373,524 $100,00 (approx./ my share)	1995-1998
None	FPGA lab hardware and software donation (while faculty at University of Southern Florida)	Xilinx	$40,000 (approx.)	1994-1995
None	International Faculty Travel grant	University of South Florida	$1,500	1995
None	Office of Sponsored research	University of South Florida	$5,500 (approx.)	1994
None	Startup grant	University of South Florida	$10,000	1993

PH.D. SUPERVISIONS COMPLETED: *(Name, *title, year, major dept, name of institution)*
(May want to add another column for titles.)

Michael LeBeane	Aug 2018	Optimizing Communication for Clusters of GPUs	ECE	UT
Reena Panda	Dec 2017	Proxy Benchmarks for Emerging Workloads (Apple)	ECE	UT
Xinnian Zheng (0.5)	May 2017	Learning Based Performance Modeling (NVIDIA)	ECE	UT
Jee Ho Ryoo	May 2017	Heterogeneous Memory Systems (Oracle)	ECE	UT
M. Faisal Iqbal	Aug 2013	Multicore Communication Processors	ECE	UT
Youngtaek Kim	May 2013	Stressmarks for Voltage Emergencies (Intel)	ECE	UT
M. Umar Farooq	Dec 2013	Value Based Branch Prediction (ARM)	ECE	UT
Arun Arvind Nair	May 2012	Modeling of Soft Errors (AMD)	ECE	UT
Karthik Ganesan	Dec 2011	Automatic Generation of Synthetic Workloads for Multicore Systems (Oracle)	ECE	UT
Jian Chen	May 2011	Resource Management for Efficient Single-ISA Heterogeneous Computing (Intel)	ECE	UT
Ciji Isen	May 2011	The Use of Memory State Knowledge to Improve Computer Memory System Organization (AMD)	ECE	UT
Jeff Stuecheli	May 2011	Ccordinated Memory Scheduling (IBM)	ECE	UT
Dimitris Kaseridis	May 2011	Memory-subsystem Resource Management for the Many-core Era (ARM Corporation)	ECE	UT
Lloyd Bircher	Dec 2010	Predictive Power Management for Multi-Core Processors (AMD)		
Ajay Joshi	Dec 2007	Constructing Adaptable and Scalable Synthetic Benchmarks for Microprocessor Performance Evaluation (ARM Corporation)	ECE	UT
Aashish Phansalkar	May 2006	Similarity Analysis and Benchmark Subsetting (Employed at Intel)	ECE	UT
Rob Bell Jr.	Dec 2005	Automatic Workload Synthesis for Early Design Studies and Performance Model Validation (Employed at IBM)	ECE	UT
Byeong Kil Lee	Aug 2005	Network Processor Design: Benchmarks and Architectural Alternatives (Employed at Texas Instruments)	ECE	UT
Shiwen Hu	Dec 2005	Effective Adaptive Computing Environment Management via Dynamic Optimization, (Employed at Freescale)	ECE	UT
Yue Luo	Aug 2005	Improving Sampled Microprocessor Simulation (Microsoft)	ECE	UT
Madhavi Valluri	May 2005	A Hybrid-Scheduling Approach for Energy-Efficient Superscalar Processors (Employed at IBM)	ECE	UT
Juan Rubio	Aug 2004	Exploring the Potential of a Hierarchical Computing Model for a Commercial Server (Employed at IBM Austin Research Lab)	ECE	UT
Tao Li	Aug 2004	OS-aware Architecture for Improving Microprocessor Performance and Energy Efficiency, (Assistant Professor University of Florida)	ECE	UT
Ravi Bhargava	Aug 2003	Instruction History Management for High-Performance Microprocessors (Employed at AMD)	ECE	UT
Deepu Talla	Aug 2001	Architectural Techniques to Accelerate Multimedia Applications on General-Purpose Processors, August 2001 (Employed at Texas Instruments)	ECE	UT
Ramesh Radhakrishnan	Aug 2000	Microarchitectural Techniques to Enable Efficient Java Execution (Employed at Dell)	ECE	UT

M.S. SUPERVISIONS COMPLETED: *(Name, year, major department, name of institution*

(May want to add another column for titles.)

Sarbartha Banerjee	May 2018	Electrical and Computer Engineering	Univ of Texas at Austin
Yashwant Marathe	May 2018	Electrical and Computer Engineering	Univ of Texas at Austin
Joseph Whitehouse	May 2016	Electrical and Computer Engineering	Univ of Texas at Austin
Jee Ho Ryoo	May 2014	Electrical and Computer Engineering	Univ of Texas at Austin
Darshan Gandhi	May 2014	Electrical and Computer Engineering	Univ of Texas at Austin
Abhishek Tondon	Dec 2013	Electrical and Computer Engineering	Univ of Texas at Austin
Don Owen	May 2013	Electrical and Computer Engineering	Univ of Texas at Austin
Ankita Garg	May 2013	Computer Sciences	Univ. of Texas at Austin
Bhargavi Narayanasetty	May 2011	Electrical and Computer Engineering	Univ. of Texas at Austin
Chaitanya Nayak	May 2011	Electrical and Computer Engineering	Univ. of Texas at Austin
Rengarajan	2010	Electrical and Computer Engineering	Univ. of Texas at Austin
Karthik Ganesan	Dec 2008	Electrical and Computer Engineering	Univ. of Texas at Austin
Rajiv Bhatia	Aug 2008	Electrical and Computer Engineering	Univ. of Texas at Austin
Justin Friesenhahn	Dec 2007	Electrical and Computer Engineering	Univ. of Texas at Austin
Jason Matalka	Aug 2006	Electrical and Computer Engineering	Univ. of Texas at Austin
Kathryn Stacer	May 2006	Electrical and Computer Engineering	Univ. of Texas at Austin
Lloyd Bircher	May 2006	Electrical and Computer Engineering	Univ. of Texas at Austin
Diego Vila	May 2006	Electrical and Computer Engineering	Univ. of Texas at Austin
Brijesh Patel	2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Jenson Lam	2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Brian Gaide	2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Jignesh Gondalia	2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Saket Kumar	May 2004	Electrical and Computer Engineering	Univ. of Texas at Austin
Michael Arunkumar	Dec 2003	Electrical and Computer Engineering	Univ. of Texas at Austin
Michael Lance Karm	Dec 2003	Electrical and Computer Engineering	Univ. of Texas at Austin
Patrick James Peters	Dec 2003	Electrical and Computer Engineering	Univ. of Texas at Austin
Mike Clark	May 2003	Electrical and Computer Engineering	Univ. of Texas at Austin
Anand Sunder Rajan	2003	Electrical and Computer Engineering	Univ. of Texas at Austin
James Yang	2002	Electrical and Computer Engineering	Univ. of Texas at Austin
Ravi Bhargava	Aug 2000	Electrical and Computer Engineering	Univ. of Texas at Austin
Vikram Godbole	May 2000	Electrical and Computer Engineering	Univ. of Texas at Austin
Sanjeev Ghai	May 2000	Electrical and Computer Engineering	Univ. of Texas at Austin
Srikanth Kannan	May 2000	Electrical and Computer Engineering	Univ. of Texas at Austin
Jyotsna Sabarinathan	Dec 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Jody Joyner	Dec 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Juan Rubio	May 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Poorva Murarka	May 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Purnima Vasudevan	May 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Roy Shalem	Aug 1998	Electrical and Computer Engineering	Univ. of Texas at Austin
Dachih-Tang	Aug 1998	Electrical and Computer Engineering	Univ. of Texas at Austin
Yin Teh	Dec 1997	Electrical and Computer Engineering	Univ. of Texas at Austin
Ramesh Radhakrishnan	Aug 1997	Computer Science and Engineering	Univ. of South Florida
Vijay Kammila	1996	Computer Science and Engineering	Univ. of South Florida
Vinod Reddy	Dec 1996	Computer Science and Engineering	Univ. of South Florida
Amudha Muthiah	1996	Computer Science and Engineering	Univ. of South Florida
Raghuveer Reddy	1995	Computer Science and Engineering	Univ. of South Florida

PH.D. IN PROGRESS: *(List students names by category)*

A. Students admitted to candidacy

1. Don Owen
2. Abhishek Tondon

B. Post M.S. students preparing to take Ph.D. qualifying exam

1. Justin Friesenhahn

M.S. IN PROGRESS: (*List students names)*

1. Jiajun Wang
2. Shuang Song
3. Qinzhe Wu
4. Bagus Hanindhito
5. Steven Flolid
6. Jim Xavier

UNDERGRAD RESEARCH ASSISTANTS: (*List students names)*

1. Zachary Susskind
2. Joseph Dean
3. Benjamin Thorell

VITA: *(One-half page paragraph that can be used for general purposes)*

Dr. Lizy Kurian John holds the Cullen Trust for Higher Education Professorship No. 3 in Electrical Engineering in the Department of Electrical & Computer Engineering at The University of Texas at Austin. She received her Ph.D. in computer engineering from The Pennsylvania State University in 1993. She joined The University of Texas Austin faculty in 1996. Her research is in the areas of computer architecture, multicore processors, memory systems, performance evaluation and benchmarking, workload characterization, and reconfigurable computing.

Prof. John's research has been supported by the National Science Foundation, Semiconductor Research Consortium (SRC), DARPA, Lockheed Martin, AMD, Oracle, Huawei, IBM, Intel, Motorola, Freescale, Dell, Samsung, Texas Instruments, etc.. She is recipient of NSF CAREER award (1996), UT Austin Engineering Foundation Faculty Award (2001), Halliburton, Brown and Root Engineering Foundation Young Faculty Award (1999), University of Texas Alumni Association Teaching Award (2004), The Pennsylvania State University Outstanding Engineering Alumnus (2011) etc.

Lizy John holds 10 U. S. patents and has published 16 book chapters, 200+ refereed journal and conference publications, and more than 50 workshop papers. She has coauthored books on Digital Systems Design using VHDL (Cengage Publishers 2017, 2007), Digital Systems Design using Verilog (Cengage Publishers 2014) and has edited a book on Computer Performance Evaluation and Benchmarking (CRC Press 2005). She has also edited three books on workload characterization.

Prof. John is the Editor-in-Chief elect of IEEE Micro (term begins 2019), and is in the editorial boards of IEEE Transactions on Sustainable Computing, IEEE Computer Architecture Letters, ACM Transactions on Architectures and Code Optimization, and has served in the past as an associate editor of IEEE Transactions on Computers and IEEE Transactions on VLSI. She is a member of IEEE, IEEE Computer Society, ACM, and ACM SIGARCH. She is an IEEE Fellow (Class of 2009).