EE 382N SUPERSCALAR MICROPROCESSOR ARCHITECTURE

Fall 2013 Unique No. 17270 T Th 11-12:30 pm ENS 126

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Course Description:
Computer architects have been striving to improve processor performance ever since the first stored program computer was designed half a century ago. Superscalar execution is one of the techniques in this avenue and most modern microprocessors employ superscalar issue and other instruction-level parallelism techniques to enhance their performance. The individual cores in most modern multicore processors utilize superscalar techniques. In the simplest words, superscalar processors are processors that can issue more than one instruction per cycle. This course deals with the tradeoffs and design considerations in the design of superscalar microprocessors and a comparison to other high performance architectural paradigms.

Course contents:

Definition of superscalar, superpipelined, SIMD and VLIW processors - Available parallelism in programs – Instruction Level Parallelism - Out of order instruction execution – Reservation Stations - Reorder Buffers - Exception handling in out of order processors - Branch Prediction techniques - Memory Systems for Superscalar Processors -Trace Caches - Memory Disambiguation and load/store reordering - Performance Evaluation of Superscalar Processors. Power and Energy consumption of processors. Comparison to Multicore processors.

Prerequisites:
EE 460N/382N.1 computer architecture course. Talk to the professor if you have questions on the prerequisite.

Good programming skills (C, Unix and at least one assembly language).

Interest in state-of-the-art microprocessors

Materials: Required:

Course notes/slides on blackboard; A Collection of papers from conferences and journals. Will be made available on Blackboard (courses.utexas.edu)

References (Not required to buy) :

1. Superscalar Processor Design, John P. Shen and Mikko Lipasti, McGraw Hill Publishers. (Many students in the past found it useful to buy this book)

2. Superscalar Microprocessor Design, by Mike Johnson, Prentice Hall Publishers

3. Computer Architecture: A Quantitative Approach, by Hennessy and Patterson, Morgan Kaufman

4. Computer Architecture: The Hardware/Software Approach, by Hennessy and Patterson, Morgan Kaufman Publishers

Grading Policy: The grading policy will be

2 Exams	45%
Course Project	25%
Project Presentation	5%
Homework Assignments, Paper Critiques, Class Participation, Literature Survey Report	25%

A 91%, A- 89%, B+ 86%, B 81% B- 79%, C+ 76%, C 71% C- 69% D - 60%, F- 50%

Last day to drop the class without academic penalty is the 12th class day. After that the course may be dropped only for non-academic reasons. A student seeking to drop the class after the fourth class should go to Engineering Student Affairs Office (ECJ 2.200). The course grade that is assigned in these cases will be the professor's estimate of your current grade. Your grade must be a "C" or better in order to receive a "Q" on the drop card.

COURSE EVALUATION: You will be given an opportunity to formally evaluate the class during the last week of classes. In addition, other informal evaluations may be conducted by the professor in the class. If you have a burning question/comment/suggestion, you may convey it to the professor during or after any lecture, verbally or in a written fashion. Or, send email.

The professor reserves the right to correct any typo on this announcement.

The University of Texas at Austin provides upon request special assistance for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4241 TDD.

Academic Dishonesty

Faculty in the ECE Department are committed to detecting and responding to all instances of scholastic dishonesty and will pursue cases of scholastic dishonesty in accordance with university policy. All parties in our community -- faculty, staff, and students -- are responsible for creating an environment that educates outstanding engineers, and this goal entails excellence in technical skills, self-giving citizenry, and ethical integrity. The world wants engineers who are competent and fully trustworthy, and both qualities must be developed day by day throughout an entire lifetime. Scholastic dishonesty includes, but is not limited to, cheating, plagiarism, collusion, falsifying academic records, or any act designed to give an unfair academic advantage to the student. The fact that you are in this class as an engineering student is testament to your abilities. Penalties for scholastic dishonesty are severe and can include, but are not limited to a record in your academic folder, a zero on the assignment/exam, re-taking the exam in question, an F in the course, or expulsion from the University. Don't jeopardize your career by an act of scholastic dishonesty

Details about academic integrity and what constitutes scholastic dishonesty can be found at the website for the UT Dean of Students Office and the General Information Catalog, Section 11-802.

EE 382N Fall 2013 More Info on Grading

Paper and Pencil HW Assignments + Programming assignments + Literature Survey

News presentation – Each student should present an interesting news item on a modern microprocessor with 1-2 slides to class (no more than 2 mnts + 3 mnt discussion) (25)

Paper – leading discussion – Several papers will be discussed in class. Some of these papers will be lead by students. Each student (student team) will lead the presentation (once). (50)

Paper Critiques, Questions based on papers – read paper and write critique before the class the paper is being discussed (approx 100)

Scribing – One student takes notes during lecture, refines it and uploads it for everybody within 24 hours after class. (25 each time)

Class Participation – (5 points each time) To get good participation grades

Be on-time
Participate in discussions
No Disruptive behavior

Literature Survey Proposal – Sept 14

Literature Survey Due – Sept 30

All of the above added up will constitute 25% of the course grade.

Project proposal due – Oct 7

Project Interim Report due – Nov 3

Project Presentations – Nov 26, Dec 3, Dec 5 (Some changes may occur depending on number of students in class. Days may have to be added.)

Test 1 – October 15
Test 2 – Nov 21

Project Final Report Due – Friday Dec 11, noon

Tentative Splits – (Changes might occur depending on the actual assignment)
Proj Prop – 3%; Interim Report – 2% - HW- 15% - HW1 – 1.5%; HW2 – 2.25%; HW3 – 2.25%; HW4 – 4.5%; HW5 – 4.5%; Literature Survey – 7%;