Errata Verilog Book

1. Page 20 – bottom – example on the right – bits that are being added, 0010 should be 0011
2. Page 33 – Figure 1-36 Caption for (a) Typo. Circiut should be changed to Circuit
3. Page 37 – Line 2 – Equation 1-38 – Highlighted character must be =; in the book it appears as +;

*fmax* = 1/( *tp*max + *tc*max + *tsu*)**(1-38)**

1. Page 39 – Example. Question (a)- Change to “What is the maximum clock frequency …..”; i.e. change “minimum clock period” to “maximum clock frequency”
2. Page 46 – Line 3 from bottom – “The last waveform in Figure 1-45 illustrates…” must be changed to “The last waveform in Figure 1-52 illustrates…”
3. Page 70 – middle of page – second logic equation should be

**Cout = XY + YCin + XCin**

The highlighted operator is wrong in the current edition.

1. Page 80 – line 16 – missing {

Must be { else if (condition)

1. Page 82 – line 8 from bottom – remove @ and add wait; must read as

wait(posedge CLK)

1. Page 86 – Line 7 – Add // before the text to indicate it is a comment
2. Page 97 – last line – add 0 at the end of last line. It should read ….hence sign bit is 0.
3. Page 103 – section 2.13.2 – line 4 – case Sel must be changed to case (Sel)
4. Page 103 – last line - remove semicolon from the endcase statement;

endcase; must be endcase

1. Page 126 – Line 9 – Delete reg [7:0]
2. Page 138 – Question 2.14 – last line of code must be

B <= B + 7;

The + sign is not appearing correctly in the current edition. Replace | with +

1. Page 154 – Question 2.56 – change = to <= (7 places to correct)

sel <= 0;

sel <= sel + 1;

sel <= sel + 2;

F <= I0;

F <= I1;

F <= I2;

F <= I3;

1. Page 167 – Equation 3-1 – Change A’B’+AC to A’B’ + AC’
2. Page 203 – Line 2 – Change TomaHawk reference to [34]
3. Page 225 – section 4.5 – Line 9 – Replace long dash with 2 short dashes.

i.e. 1—0/0110 must be replaced with 1- - 0/0110

1. Page 288 – Line 6 – change “use d” to “used”
2. Page 319 – Caption of TABLE 5-3, last line should be Figure 5-29 (not 5-29b).i.e. 5-29b should be changed to 5-29
3. Page 319 – Last para – line 3 – typo – muliplexer -> multiplexer
4. Page 335 – Top right – the table next to the figure – Change the second X1 to X2; Change the 3rd X1 to X3. So the table must read

T1T2

1. 1
2. X1

10 X2

11 X3

1. Page 355- Second paragraph must be modified as follows: “The Xilinx Kintex FPGA uses four copies of the basic block shown in Figure 6-13 to form a slice. Two such slices are combined to form a Configurable Logic Block (CLB). Each slice thus contains four six-input Look Up Tables (LUT6), 8 flip-flops, the carry chain, and several multiplexers.”
2. Page 355- The paragraph after Figure 6-13 should be replaced by the following: “Each LUT6 can be used to generate one 6-variable function or two 5-variable functions. The 6-variable function is generated by combining two 5-variable functions using a 2-to-1 multiplexer. There are 2 outputs from the LUT6, namely O6 and O5. One of the outputs (O6) can use up to 6 input variables. The second output (O5) can use only up to 5 input variables. It should be noted that these are not independent variables or independent functions. Five of the variables are common between O6 and O5 and the function O5 has to be a sub-function of the function O6. There are 3 external outputs from the slice, AMUX, A and AQ, but only two of them can be used simultaneously.  One of the outputs, A is a combinational output, while the AQ output is always a registered output. The AMUX output can be either combinational or registered. The O6 function can be brought out through any of the 3 output lines, however, the O5 output can be brought out only via AMUX and AQ. There are several multiplexers and other gates to allow this routing. The slices also support carry chaining. The Kintex chips use two slight variations of this slice structure, which they call SLICEL and SLICEM.”
3. Page 377 – Line 3 after subtitle Synthesis of a Case Statement – Change “inputs a and b are each implemented with 2-bit binary numbers.” to “input a and output b are 2-bit binary numbers.”
4. Page 384 – Figure – Top left block of figure 6-31(b) – the block must say 4-bit adder; Currently it says 4-bit Counter. Replace Counter with “Adder”. Only in the top left block. There is another 4-bit counter below that. That stays as counter.
5. Page 419 – Figure 7-12- Step7 of the flowchart – The path for No (N) should go back to Step 4, not step 2.
6. Page 433 – left-align the end after Cin= Cout; with begin – 3 lines above.
7. Page 462 – middle of Page – Change “Figure 8-22 shows a Verilog code that read a file …”.with *“*Figure 8-22 shows Verilog code that reads a file …” (i.e. remove “a” and change read to reads.)
8. Page 483 –first row in the table – last column - $s3 should be changed to $3.
9. Page 483 –first row in the table – first column – Change Add to add.

i.e. Add -> add

1. Page 483 –second row in the table – first column – Change Sub to sub.

i.e. Sub -> sub

1. Page 483 – row 23 in Table 9-7 rightmost column – beq $1,$2,100 should be changed to beq $1,$2,25
2. Page 483 – row 24 in Table 9-7 rightmost column – bne $1,$2,100 should be changed to bne $1,$2,25
3. Page 483 – row 29 in Table 9-7 rightmost column – j 10000 should be changed to j 2500
4. Page 483 – row 31 (last row) in Table 9-7 rightmost column – jal 10000 should be changed to jal 2500
5. Page 490 – last paragraph – Line 3 from bottom – change R-format to I-format
6. Page 490 – last paragraph – Line 2 from bottom – change I-format to R-format
7. Page 495 – Delete Line 8 of code in Figure 9-7 –

i.e. reg[6:0] counter; should be deleted.

1. Page 495 – Line 14 of code in Figure 9-7 – Add // to show that the code is commented out. So it should read

//$readmemh(“MIPS\_Instructions.txt”, RAM):

1. Page 503 – line 14 from bottom – PC=$16 is wrong; Change $16 to 16, i.e. PC = 16.
2. Page 508 – Question 9.1 Delete “Pentium 4 ->”
3. Page 508 – Question 9.1 Delete “Pentium 3 ->”
4. Page 521 – Line 5 – Change S5 to S2.
5. Page 539 – Line 2 – The, the -> Then, the
6. Page 553 – middle of page – Change LSFR to LFSR.
7. Page 555 – towards bottom of page – (e) case expression - remove semicolon from the endcase statement;

endcase; must be endcase