

**THE UNIVERSITY OF TEXAS AT AUSTIN**  
**College of Engineering**  
**Standard Resume**

**FULL NAME:** Lizy Kurian John                      **TITLE:** Professor

**DEPARTMENT:** Electrical and Computer Engineering

**CITIZENSHIP:**                      U.S.

**EDUCATION:** *(Institution, major, degree, dates)*

The Pennsylvania State University	Computer Engineering	PhD	August 1993
The University of Texas at El Paso	Computer Engineering	MS	December 1989
The University of Kerala, India	Electronics and Communication	BS	August 1984

**PROFESSIONAL REGISTRATION:** Texas Professional Engineer License, Since 2001

**CURRENT AND PREVIOUS ACADEMIC POSITIONS:** *(Institution, rank(s), beginning and ending dates for each rank)*

The University of Texas at Austin	Professor and Centennial Teaching Fellow	Fall 2007-
The University of Texas at Austin	Associate Professor	Fall 2001-Summer 2007
The University of Texas at Austin	Assistant Professor	Fall 1996-Summer 2001
The University of South Florida, Tampa	Assistant Professor	Fall 1993-Summer 1996

*(The order of the categories below this point is optional)*

**OTHER PROFESSIONAL EXPERIENCE:** *(Name of company, position, beginning and ending dates)*

Penn State, Electrical Engineering Dept	Research Assistant	8/90 - 8/93
Penn State, Electrical Engineering Dept	Teaching Assistant	1/90 - 5/90
University of Texas at El Paso, Electrical Engineering Dept	Teaching Assistant	8/88 -12/89
Indian Space Research Organization, Trivandrum, India	Scientist/Engineer	8/84 - 8/88

**\*CONSULTING:** *(Names of companies, beginning and ending dates)*

Texas Digital and MultiMedia Systems	May 2008-date
EcoViv Inc.	June 2008-date
SmoothStone	June 2008-date

**HONORS AND AWARDS:** *(Include dates)*

- IEEE Fellow, 2009-
- SPEC Benchmark workshop 2006, The K. Dixit award for best paper won by student Ajay Joshi
- TEXAS EXES Teaching Award, Feb 2004
- Engineering Foundation Faculty Award, College of Engineering, UT Austin, Fall 2001

- UT Austin Engineering Foundation Centennial Teaching Fellowship in Electrical Engineering No. 2, Sept 2000- present
- Halliburton, Brown and Root Engineering Foundation Young Faculty Award, College of Engineering, UT Austin, Fall 1999
- IBM Austin Center for Advanced Studies (CAS) and University Partnership Award- every year since 2001
- Best Paper Award, Computer Track, IEEE International Performance Conference on Computing and Communication, Feb 1999
- Elevated to Senior Membership of IEEE (Electrical and Electronics Engineers), 1997
- National Science Foundation CAREER Award, 1996-2001
- \$1000 award for being Advisor of the student who won the University Level George H. Mitchell Undergraduate Student Achievement Award, April 2002 (Student Pattabi Seshadri won the \$2000 award)
- Oak Ridge Junior Faculty Enhancement Award, 1996-1997
- Outstanding Young Investigator, College of Engineering, University of South Florida, 1995-1996
- Outstanding Undergraduate Teaching Award, University of South Florida, Tampa, 1994-1995.
- Best Paper Award, ASEE Gulf Southwest Conference, March 1998
- Graduate School Fellowship, awarded by the Graduate School, The Pennsylvania State University, 1991-1992
- George Krutilek Fellowship awarded by the Graduate School, The University of Texas at El Paso, 1988-1989
- Graduate School Marshal for the December 1989 commencement at The University of Texas at El Paso
- Schellenger Research Scholarship awarded by the Electrical Engineering Department, Univ. of Texas El Paso, Summer 1989
- Selected by NCERT (National Council of Educational Research and Training), New Delhi, Govt. of India, on the basis of a National Examination, for the National Talent Search Scholarship for 1977-1984
- 3rd Rank in the Kerala University B.Sc. Engineering Degree Exam, 1984
- 1st rank (1st out of 70,462 students) in the Kerala University Pre Degree Exam, India, 1979
- 2nd rank in the whole state of Kerala (2nd out of 275,554 students) in the Kerala State Higher Secondary School Exam, India, 1977

**\*MEMBERSHIPS IN PROFESSIONAL AND HONORARY SOCIETIES:**

- Senior Member, IEEE, 1997-present
- Member, IEEE Computer Society, 1989-present
- Member, ACM (Association of Computing Machinery), ACM - SIGARCH, since 1990
- Member ACM SIGMICRO since 2001
- Member Eta Kappa Nu, Tau Beta Pi, Phi Kappa Phi

**UNIVERSITY COMMITTEE ASSIGNMENTS:** *(Include major departmental, college, and university assignments, including administrative assignments, with beginning and ending dates)*

Departmental-	Computer Engineering Ph. D Coordinator	2007-
	Curriculum Reform Subcommittee	2008
	ECE ABET Committee	2003-2007
	ECE Appeals Committee	1999-2003
	ECE Awards Committee	2001-04
	ECE Hiring Subcommittee, Computer Architecture Position	2001-06
	Department of ECE, Appeals Committee	April 2000-Mar 2001, April 2001- March 2002
	Department of ECE, Computer Engineering Faculty Committee	September 1996- present
	Department of ECE Subcommittee on Computer Engineering Graduate Admissions	1997-2006
	Department of ECE, Graduate Studies Committee,	September 1996- present

	Department of ECE, Undergraduate Software Curriculum Committee	Sept 1996-2001
	Department of ECE, Undergraduate Digital Systems Curriculum Committee	Sept 1996-2001
College-	College of Engineering Honors Committee	2005-2008
	College of Engineering Hocott Awards Committee	2006, 2007, 2008
	College of Engineering Equal Opportunity in Engineering Committee	2005-08
	College of Engineering Honors Committee	2004-05
	College of Engineering Equal Opportunity in Engineering Committee	2004-05
	College of Engineering Honors Committee	2003-04
	College of Engineering Equal Opportunity in Engineering Committee	2003-04
	College of Engineering Honors Students Committee	2002-03
	College of Engineering Honors Students Committee, chaired by Prof. Bill Rossen	1997-98, 1998-99, 1999-2000, 2000-01, 2001-02
University-	Circuit Design Masters Program Minority Liaison	2007
	Circuit Design Masters Program Minority Liaison	2006
	Circuit Design Master Program Minority Liaison	2005

**PROFESSIONAL SOCIETY AND MAJOR GOVERNMENTAL COMMITTEES:** *(Include dates)*

- **Search Committee Member**, ACM Transactions on Architecture and Code Optimization (TACO) Editor In Chief Search , 2008-2009
- **Associate Editor**, IEEE Transactions on VLSI, 2003 December-August 2007
- **Editorial Board**, IEEE MICRO, 2005 -
- **Editorial Board**, International Journal on Embedded Systems, 2005-present
- **Member**, National Science Foundation Workshop on Computer Performance Evaluation Techniques, December 2001, Austin TX
- **Member**, National Science Foundation Proposal Review Panel, 2000, 1998, 1997

**\*COMMUNITY ACTIVITIES:**

**General Chair**

- IEEE International Symposium on Workload Characterization (IISWC) 2005
- IEEE International Symposium on Performance Analysis of Systems and Software, ISPASS 05
- IEEE Intl Workshop on Workload Characterization (WWC), 1998-2005

**Program Chair**

- SPEC Workshop 2006, Program co-chair
- ISPASS 2004 (IEEE International Symposium on Performance Analysis of Systems and Software)
- ICCD 1999 Architecture Track Program co-chair ( IEEE International Conference on Computer Design)
- ISPASS 2000 Workload Characterization Track (IEEE International Symposium on Performance of Software and Systems)
- WWC (Workshop on Workload Characterization), 1998-2004

- ODES 2003-2005 (Optimizations for DSP and Embedded Systems Workshop), (held in conjunction with the CGO symposium) (co-chair)

#### **Program Committee Member**

- Virtual Execution Environments (VEE) 2008
- PACT (Parallel Architectures and Compilation techniques) 2009
- IPDPS 2009
- IEEE International Conference on Computer Design (ICCD) 2008
- 2007 Supercomputing Conference, Performance Track
- IEEE Symp on High Performance Computer Architecture (HPCA 2005)
- IEEE-Symp on High Performance Computer Architecture (HPCA 2002)
- Parallel Architectures and Compilation techniques (PACT 2003)
- IEEE-International Symposium on Microarchitecture (MICRO-33), 2000
- IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2001)
- IEEE International Performance Conference on Computing and Communication (IPCCC 2000)
- IEEE International Conference on Computer Design, Architecture Track (ICCD 1999)
- IEEE International Performance Conference on Computing and Communication (IPCCC 1999)
- 1998 IEEE International Conference on Computer Design (ICCD), Architecture Track
- International Performance and Dependability Symposium (IPDS), held along with DSN 2002
- North Atlantic Test Symposium, 1997
- Workshop on Workload Characterization (1998-2004)
- MoBS workshop 2005 (held with ISCA)
- Value Prediction Workshop, 2004
- MRE 2004 (Managed RunTime Environment), 2003 (held with CGO)
- INTERACT-6, Workshop on Interaction between Architectures and Compilers, in conjunction with IEEE-International Symposium on High Performance Computer Architecture (HPCA-8), 2002
- Workshop on Hardware Support for Objects and Microarchitectures for Java (in conjunction with IEEE International Conference on Computer Design 2001)
- Workshop on Decoupled Access Execute Architectures (MEDEA) in conjunction with PACT2001
- Workshop on Hardware Support for Objects and Microarchitectures for Java (in conjunction with IEEE International Conference on Computer Design ICCD 2000)
- Workshop on Decoupled Access Execute Architectures (in conjunction with PACT 2000)
- Workshop on Media Processors and Digital Signal Processors, Nov 1999 (in conjunction with 32<sup>nd</sup> IEEE International Symposium on Microarchitecture Micro-32)
- Workshop on Hardware Support for Objects and Microarchitectures for Java (in conjunction with IEEE International Conference on Computer Design 1999)

#### **Other Committees/Positions:**

- Member, Industrial and Professional Advisory Council (IPAC), Penn State College of Engineering, 2008
- Member, IEEE Senior Member Selection Panel, October 2007
- Member, External Advisory Board, ECE Department, UT El Paso, 2008
- Member, External Advisory Board, University of North Texas, 2008
- ACM SIGMICRO Vice Chair, 2006-2008
- ACM SIGMICRO Member at large, 2005-2008
- Steering Committee, SPEC workshops, 2005-date
- Steering Committee, IISWC, 2005-present
- Steering Committee, ISPASS, 2000-present
- ACM SIGMICRO Public Relations Director 2002-03, 2001-02
- Travel Awards Chair, IEEE International Symposium on Parallel Architectures and Compilation techniques (PACT 2003)
- Tutorials/Workshop Chair, IEEE International Symposium on Performance Analysis of Systems and Software, ISPASS, March 2003
- 2000 IEEE International Conference on Computer Design, Special Sessions Chair

- Finance Chair, IEEE Workshop on Workload Characterization, 1998-2004
- Finance Chair, IEEE International Performance Conference on Computing and Communication, (IPCCC 2000)
- Panel Chair, IEEE International Performance Conference on Computing and Communication, Feb 1999
- Registration Chair - IEEE International Symposium on Microarchitecture, MICRO-31, Dallas, TX, Dec 1998

#### Other Workshops Organized:

1. 1<sup>st</sup> Workshop on Integrating Design and Design Automation into Undergraduate Computer Science and Engineering Curriculum.  
For: University Faculty from around the country.  
Partially funded by: The National Science Foundation  
August 5-8, 1996 Tampa, Florida, 33620.
2. 2<sup>nd</sup> Workshop on Integrating Design and Design Automation into Undergraduate Computer Science and Engineering Curriculum.  
Partially funded by: National Science Foundation  
August 4-7, 1997 Tampa, Florida, 33620.

#### Workshop Sessions/Seminars/Tutorials Organized:

1. Workshop Session on High Performance Processors organized at:  
Workshop title: IEEE Computer Society 1996 Annual Workshop on VLSI  
Held: Nov. 3-6, 1996  
Location: Clearwater, Florida
2. Half-day Tutorial Presentation:  
At the Workshop of Microelectronic Systems Education, July 1997, Arlington, Virginia. Tutorial Topic:  
Rapid Prototyping using FPGAs, July 23, 1997
3. Half-day Seminar presented:  
In the AUSTIN INNOVATION SERIES, Aug 27, 1997 at IBM, Austin  
Topic: Improving the Memory Access Performance of Programs

#### Technical Reviewer:

Technical reviewer for several journals, conferences, and workshops, various years, including but not limited to

- HPCA 2008
- ACM TACO
- ACM TOMACS
- IEEE Transactions on Computers
- IEEE Transactions on Parallel and Distributed Systems
- The Computer Journal
- The Journal of VLSI
- Microprocessors and Microsystems
- IEE Journal of Computers and Digital Techniques
- IEEE Computer
- IEEE Micro Magazine
- IEEE Concurrency
- IEEE/ACM International Symposium on Computer Architecture (ISCA)
- IEEE Intl High Performance Computer Architecture Symposium (HPCA)
- IEEE International Symposium on Microarchitecture (MICRO)
- PACT (Parallel Architectures and Compilation Techniques) Conf., 2001
- IEEE Workshop on Hardware Support for Objects and Microarchitectures for Java (in conjunction with IEEE International Conference on Computer Design)
- IEEE International Performance Conference on Computing and Communication 1999, 2000
- IEEE Workshop on Workload Characterization
- Workshop on Media Processors and Digital Signal Processors, Nov 1999 (in conjunction with IEEE Micro-32)
- IEEE International Conference on Computer Design (ICCD) 1998, 1999
- North Atlantic Test Symposium 1997
- Reviewer for McGraw Hill 2001-2002
- Reviewer for McGraw Hill, 2000
- Reviewer for Prentice Hall USA (1995), Prentice Hall UK (1999)
- Reviewer for Addison Wesley (1997)
- Kluwer Academic Publishers Book Proposal Reviewer, 2001
- Reviewer for IEEE Computer's Special Issue on Billion Transistor Processors, 1997
- Member, Focus Group on IEEE Spectrum and its Web Site, Tammadge Market Research Group, May 1998

Other Activities:

1. **Judge:** Texas High School State Science and Engineering Fair, April 2001
2. **Judge:** Florida High School Science Fair, 1994

**PUBLICATIONS:** *\*In listing publications, please use the following format: author's name(s), title of paper, journal name, volume number, page numbers, month and year. )*

A. Refereed Archival Journal Publications

1. Byeong Kil Lee and Lizy K. John, "Hardware acceleration for media / transaction applications in Network Processors", Accepted for publication in **IEEE Transactions on VLSI**, 2008
2. Ajay Joshi, Lieven Eeckhout, Robert H. Bell Jr. and L. K. John, Distilling the Essence of Proprietary Workloads into Miniature Benchmarks. accepted at **ACM Transactions on Architecture and Code Optimization (TACO)**, 2008
3. Yue Luo, Ajay Joshi, Aashish Phansalkar, Lizy K. John, and Joydeep Ghosh, "Analyzing and Improving Clustering Based Sampling for Microprocessor Simulation". Accepted at International **Journal of High Performance Computing and Networking**, To appear 2008

4. Ajay Joshi, Yue Luo and Lizy John, Applying Statistical Sampling for Fast and Efficient Simulation of Commercial Workloads, **IEEE Transactions on Computers**, Vol. 56, No. 11, November 2007
5. C. Isen, H. Angepat, L. John, J. P. Choi, H. J. Song, "Embedded Java Benchmark Analysis on the ARM Processor". Accepted for **International Journal on Embedded Systems**, 2007.
6. Tao Li , Lizy Kurian John , Anand Sivasubramaniam , N. Vijaykrishnan , Juan Rubio, OS-Aware Branch Prediction: Improving Microprocessor Control Flow Prediction for Operating Systems, **IEEE Transactions on Computers**, Vol. 56, No. 1, January 2007, pp. 2-17
7. Joshua J. Yi , Lieven Eeckhout , David J. Lilja , Brad Calder , Lizy K. John , James E. Smith The Future of Simulation: A Field of Dreams, **IEEE Computer**, November 2006, pp. 22-29
8. Ajay Joshi, Aashish Phansalkar, Lieven Eeckhout, and Lizy K. John, "Measuring Benchmark Similarity Using Inherent Program Characteristics", **IEEE Transactions on Computers**, Vol. 55, No. 6, June 2006, pp. 769-782.
9. Madhavi Valluri, Lizy John and Heather Hanson, "Hybrid-Scheduling: A Technique to Exploit Static Schedules for Reduced Energy Consumption in High-Performance Processors. **IEEE Transactions on VLSI**. Vol. 14, No. 9, September 2006, pp. 1039-1043
10. Byeong Kil Lee, L. K. John and E. B. John, "Architectural Enhancements for Network Congestion Control Applications". **IEEE Transactions on VLSI**, VOL.14, NO. 6, pp. 609-615, JUNE 2006
11. Shiwen Hu, Madhavi Valluri, and Lizy K. John, "Effective Adaptive Computing Environment Management via Dynamic Optimization", **ACM Transactions on Architecture and Code Optimization (TACO)**, Vol. 3, No. 4, Dec 2006, pp. 477-501
12. Tao Li and Lizy Kurian John, "Operating System Power Minimization through Run-time Processor Resource Adaptation". Accepted at **Journal of Microprocessor and Microsystems**, Volume 30, Issue 4, page 173-224, June 2006
13. Juan Rubio and Lizy K. John, "Reducing Server Data Traffic using a Hierarchical Computation Model", **IEEE Transactions on Parallel and Distributed Systems**, Oct 2005, 933-943.
14. Byeong Kil Lee and Lizy K. John, "Implications of Executing Compression and Encryption Applications on General Purpose Processors", **IEEE Transactions on Computers**, July 2005, Vol. 54, No. 7, pp. 917-922.
15. Tao Li, Ravi Bhargava, L. K. John, "Adapting Branch-Target Buffer to Improve the Target Predictability of Java Code", **ACM Transactions on Architecture and Code Optimization (TACO)**, Vol. 2, No. 2, June 2005, pp. 109-130.
16. L. Eeckhout, Y. Luo, K. Bosschere, and Lizy K. John, "BLRL: Accurate and Efficient Warmup for Sampled Processor Simulation," **The Computer Journal**. Vol. 48. No. 4, May 2005, pp. 451-459.
17. Yue Luo and Lizy K. John, "Efficiently Evaluating Speedup Using Sampled Processor Simulation, **Computer Architecture Letters**, vol 3, Sept 2004, pp. 22-25.
18. D. Burger, S. Keckler, K. S. McKinley, M. Dahlin, L.K. John, C. Lin, C. R. Moore, J. Burrill, R. G. McDonald, W. Yoder and the TRIPS team, "Scaling to the End of Silicon with EDGE architectures", **IEEE Computer**, July 2004, pp. 44-55.
19. Yue Luo and Lizy John, "Locality Based On-Line Trace Compression", **IEEE Transactions on Computers**, Volume 53, Number 6, June 2004, pp. 723-731.
20. Shiwen Hu, Ravi Bhargava, and Lizy K. John, "The Role of Return Values in Exploiting Speculative Method-Level Parallelism", **The Journal of Instruction-Level Parallelism (JILP)**, Vol. 5. November 2003.
21. Deepu Talla, Lizy John, and Doug Burger, "Bottlenecks in multimedia processing with SIMD style extensions and architectural enhancements", **IEEE Transactions on Computers**, Volume 52, Number 8, ISSN 0018-9, Aug 2003, pp. 1015-1031.

22. Yue Luo, Pattabi Seshadri, Juan Rubio, Lizy John and Alex Mericas, "Benchmarking Internet Servers on Superscalar Machines", **IEEE Computer**, Feb 2003, pp. 34-40.
23. Tao Li and L. John, "ADirpNB: A cost-effective way to Reduce Directory Memory Overhead for Full Map Directory Based Cache Coherence Protocols", **IEEE Transactions on Computers**, Sept 2001, Vol. 50, No. 9, pp. 921-934.
24. R. Radhakrishnan, N. Vijaykrishnan, L. K. John, A. Sivasubramaniam, J. Rubio, and J. Sabarinathan, "Java Runtime Systems: Characterization and Architectural Implications", **IEEE Transaction on Computers**, Feb 2001, Vol.50, No. 2, pp. 131-146.
25. Lizy Kurian John, "Data Placement Schemes to Reduce Conflicts in Interleaved Memories", **The Computer Journal**, Vol. 43, No. 2, 2000.
26. Lizy Kurian John, "Memory Chips with Adjustable Configurations", **The VLSI Design Journal**, Gordon Breach Publishers, Vol. 10(2), 1999, pp. 203-215.
27. L. K. John, Tao Li and A. Subramanian, "Annex Cache: A Cache Assist to implement Selective Caching", **Microprocessors and Microsystems Journal**, December 1999, Volume 23 Nos 8-9, Elsevier Publications, pp. 537-551.
28. Lizy Kurian John and Eugene B. John, "A Dynamically Reconfigurable Interconnect for Array Processors", **IEEE Transactions on VLSI**, March 1998, Vol. 6, No. 1, pp. 150-157.
29. Lizy Kurian John, Yu-cheng Liu, "Performance Model for a Prioritized Multiple-Bus Multiprocessor System", **IEEE Transactions on Computers**, Vol. 45, No. 5, May 1996, pp. 580-588.
30. Paul T. Hulina, Lee Coraor, Lizy Kurian and Eugene John, "Design and VLSI Implementation of an Address Generation Coprocessor", **IEE Proceedings on Computers and Digital Techniques**, Vol. 142, No. 2, March 1995, pp. 145-151.
31. Lizy Kurian, Paul T. Hulina and Lee D. Coraor, "Memory Latency Effects in Decoupled Architectures", **IEEE Transactions on Computers**, Vol. 43, No. 10, Oct 1994, pp. 1129 - 1139.
32. Paul T. Hulina, Lizy Kurian, Eugene John and Lee D. Coraor, "Design and VLSI Implementation of an Access Processor for a Decoupled Architecture", **Journal of Microprocessors and Microsystems**, vol 16, No 5, May 1992, pp. 237 - 247.

#### Other journal/magazine Articles:

1. A. Phansalkar, A. Joshi and Lizy K. John, "Subsetting the SPEC CPU 2006", **Computer Architecture News**, Vol. 35, No. 1-March 2007, pp. 69-76
2. L. K. John, "More on Finding a Single Number to Indicate Overall Performance of a Benchmark Suite", **ACM Computer Architecture News**, Vol. 32, No. 1- March 2004, pp. 3- 8.
3. Deepu Talla and Lizy John, "MediaBreeze: A decoupled architecture for accelerating multimedia applications", **ACM Computer Architecture News**, ACM Press, ISSN 0163-5964, vol. 29, no. 5, Dec. 2001, pp. 62-67.
4. Lizy John and Ramesh Radhakrishnan, "c\_ICE: A Compiler-Based Instruction Cache Exclusion Scheme", **Newsletter of the Technical Committee on Computer Architecture (TCCA)**, June 1997, pp 60-61.

#### Papers Under Review:

1. Rob Bell Jr. and L. K. John, "Improved Automatic Test Case Synthesis for Performance Model Validation and the Role of Statistical Simulation". Submitted to **IEEE Transactions on Computers**.
2. Tao Li, Lizy Kurian John, "OS-aware Tuning: Improving I-Cache Energy Efficiency on the System Workloads". Submitted to **IEEE Transactions on Computers**.

#### **B. Refereed Conference Proceedings**

1. W. Lloyd Bircher and Lizy K. John, " Analysis of Dynamic Power management on Multi-Core Processors", **Proceedings of the International Conference on Supercomputing (ICS)**, 2008, pp/ 327-338, (37 accepts/ 140 submissions)

2. A. Joshi, L. Eeckhout, L. K. John, and C. Isen, "Automated Microprocessor Stressmark Generation", Proceedings of the IEEE International High Performance Computer Architecture (HPCA) Symposium, 2008
3. Jian Chen and Lizy K. John, "Energy-Aware Application Scheduling on a Heterogeneous Multi-core System", 2008 IEEE International Symposium on Workload Characterization, Sept 14-16
4. Ciji Isen and Lizy John, On the Representativeness of Embedded Java Benchmarks. IEEE International Symposium on Workload Characterization (IISWC) 2008.
5. Karthik Ganesan, Lizy K. John, Valentina Salapura, and James Sexton, "A Performance Counter Based Workload Characterization on Blue Gene/P", Proceedings of the International Conference on Parallel Processing (ICPP), 2008
6. Arun Nair and Lizy K. John, "Simulation Points for SPEC CPU 2006", Proceedings of the 2008 International Conference on Computer Design (ICCD), 2008.
7. Justin J. Friesenhahn, Lizy Kurian John, and Mark McDermott, "Power Analysis of a Path-Based Perceptron Branch Predictor," Austin conference on Integrated Systems and circuits (ACISC), May 2008.
8. A. Phansalkar, A. Joshi and L. K. John, "Analysis of Redundancy and Program Balance in SPEC CPU 2006", ISCA 2007, San Diego, June 2007, pp. 412-423 (46 accepts/204 submissions)
9. William Lloyd Bircher and Lizy K. John, Complete System Power Estimation: A Trickle-Down Approach Based on Performance Events, ISPASS (IEEE International Symposium on Performance Analysis of Systems and Software) April 2007
10. Ajay Joshi, Lieven Eeckhout, and Lizy John. Exploring the Application Behavior Space Using Parameterized Synthetic Benchmarks. Extended abstract, Parallel Architectures and Compilation Techniques, September 2007
11. Joshua J. Yi, Resit Sendag, Lieven Eeckhout, Ajay Joshi, David J. Lilja, and Lizy K. John, Evaluating Benchmark Subsetting Approaches, International Symposium on Workload Characterization, October 2006, pp. 93-104 (18/57 submissions)
12. Ajay Joshi, Lieven Eeckhout, Robert H. Bell Jr., and Lizy K. John, Performance Cloning: A Technique for Disseminating Proprietary Applications as Benchmarks International Symposium on Workload Characterization. October 2006, pp. 105-115 (18 accepted/57 submissions)
13. Jiajin Tu, Jian Chen, and Lizy K. John, Hardware Efficient Piecewise Linear Branch Predictor. 20th International Conference on VLSI Design. January 2007.
14. Kenneth Hoste, Aashish Phansalkar, Lieven Eeckhout, Andy Georges, Lizy K. John and Koen De Bosschere, "Performance Prediction based on Inherent Program Similarity", Proceedings of Parallel Architectures and Compilation Techniques (PACT), Sept. 2006.
15. Lloyd Bircher and Lizy John, Power Phases in a Commercial Server Workload, Poster Paper for International Symposium for Lower Power Electronics and Design (ISLPED), Germany, Oct. 2006.
16. Shiwen Hu and Lizy K. John, "Avoiding Store Misses to Fully Modified Cache Blocks", IEEE International Performance Computing and Communications Conference (IPCCC), April 2006, pp. 289-296. (Acceptance rate: 60 accepted/142 submissions = 42%)
17. Tao Li and Lizy Kurian John, "OS-aware Tuning: Improving Instruction Cache Energy Efficiency on System Workloads", IEEE International Performance Computing and Communications Conference, April 2006, pp. 321-330. (Acceptance rate: 60 accepted/142 submissions = 42%)
18. Robert H. Bell, Rajiv R. Bhatia, Lizy John, Jeff Stuecheli, Ravel Thai, John Griswell, Paul Tu, Louis Capps, Anton Blanchard, "Automatic Testcase Synthesis and Performance Model Validation for High-Performance PowerPC Processors", Proceedings of the International Symposium on Performance Analysis of Systems and Software (ISPASS), March 2006, pp. 154-165. (Acceptance rate: 24 accepted/81 submissions = 30%)
19. Ajay Joshi, Lizy John, Joshua J. Yi, Robert H. Bell Jr., Lieven Eeckhout and David Lilja, "Evaluating the Efficacy of Statistical Simulation for Design Space Exploration", Proceedings of the International

- Symposium on Performance Analysis of Systems and Software (ISPASS), March 2006, pp. 70-79. (Acceptance rate: 24 accepted/81 submissions = 30%)
20. Shiwen Hu and Lizy K. John, "Impact of Virtual Execution Environments on Processor Energy Consumption and Hardware Adaptation", Accepted for ACM International Conference on Virtual Execution Environments (VEE 2006), 2006, pp. 100-110. (Acceptance rate: 17 accepted/44 submissions = 39%)
  21. Robert H. Bell and Lizy K. John, "Efficient Power Analysis using Synthetic Testcases", IEEE International Symposium for Workload Characterization (IISWC), Oct 2005, pp. 110-118. (Acceptance rate: 17 accepted/52 submissions = 33%)
  22. Yue Luo and Lizy John, "Simulating Commercial Java Throughput Workloads: A Case Study", International Conference on Computer Design (ICCD 05), Oct 2005, pp. 393-398. (Acceptance rate: 101 accepted/313 submissions = 32%)
  23. Yue Luo, Ajay Joshi, Aashish Phansalkar, Lizy John, and Joydeep Ghosh, "Analyzing and Improving Clustering Based Sampling for Microprocessor Simulation", 17th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), Oct 2005, pp. 193-200. (Acceptance rate: 29 accepted/93 submissions = 35%)
  24. W. Lloyd Bircher, M. Valluri, J. Law and L. John, "Runtime Identification of Microprocessor Energy Saving Opportunities", International Symposium on Low Power Electronics and Design (ISLPED), Aug 2005, pp. 275-280. (Acceptance rate: 53 accepted/233 submissions = 23%)
  25. B. K. Lee, L. John and E. B. John, "Architectural Support for Accelerating Congestion Control Applications in network Processors", IEEE 16th International Conference on Application-specific Systems, Architectures and Processors (ASAP 2005), July 2005, pp. 169-175. (Acceptance rate: 43 accepted/90 submissions = 48%)
  26. Robert H. Bell, Jr. and Lizy K. John "Improved Automatic Test case Synthesis for Performance Model Validation", 19th ACM International Conference on Supercomputing (ICS), June 2005, pp. 111-120. (Acceptance rate: 42 accepted/152 submissions = 28%)
  27. Madhavi Valluri, Lizy K. John, and Kathryn McKinley "Low Power, Low Complexity Instruction Issue Using Compiler Assistance", 19th ACM International Conference on Supercomputing (ICS), June 2005, pp. 209-218. (Acceptance rate: 42 accepted/152 submissions = 28%)
  28. Aashish Phansalkar, Ajay Joshi, Lieven Eeckhout, and Lizy K. John, "Measuring Program Similarity", Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 05), April 2005, pp. 10-20. (Acceptance rate: 27 accepted/92 submissions = 29%)
  29. Yue Luo and L. K. John, "On Sampling Unit Size in Sampled Microprocessor Simulation", Proceedings of the IEEE IPCCC Conference, April 2005, pp. 81-90. (Acceptance rate: 36 accepted/103 submissions = 35%)
  30. Shiwen Hu, Madhavi Valluri, and Lizy K. John, "Effective Adaptive Computing Environment Management via Dynamic Optimization", International Symposium on Code Generation and Optimization (CGO), March 2005, pp. 63-73. (Acceptance rate: 26 accepted/75 submissions = 35%)
  31. Yue Luo, Lizy K. John, and Lieven Eeckhout, "Self-Monitored Adaptive Cache Warm-Up for Microprocessor Simulation", Proceedings of 16th Symposium on Computer Architecture and High Performance Computing (SBAC-PAD) 2004, pp. 10-17. (Acceptance rate: 32 accepted/93 submissions = 34%)
  32. Juan Rubio, Charles Lefurgy, and Lizy K. John, "Improving Server Performance on Transaction Processing Workloads by Enhanced Data Placement", Proceedings of 16th Symposium on Computer Architecture and High Performance Computing (SBAC-PAD) 2004, pp. 84-91. (Acceptance rate: 32 accepted/93 submissions = 34%)
  33. Juan Rubio and Lizy John, "Analysis of the Execution of a Next Generation Application on Superscalar and Grid Processors", Proceedings of IEEE International Conference on Parallel and Distributed Systems (ICPADS 2004), Newport Beach, California, July 7-9, 2004, pp. 307-314. (Acceptance rate: 66 accepted/213 submissions = 31%)

34. Lieven Eeckhout, Robert Bell Jr., Bastiaan Stougie, Koen De Bosschere, Lizy K. John, "Control Flow Modeling in Statistical Simulation for Accurate and Efficient Processor Design Studies", Proceedings of the International Symposium on Computer Architecture (ISCA), Munich, Germany, June 2004, pp. 350-361. (Acceptance rate: 31 accepted/217 submissions = 14%)
35. Byeong Kil Lee and Lizy K. John, "NpBench: A Benchmark Suite for Control Plane and Data Plane Applications for Network Processors", ICCD 2003, pp. 226-233. (Acceptance rate: 61 accepted/233 submissions = 26%)
36. Madhavi Valluri, Lizy Kurian John and Heather Hanson, "Exploiting compiler-generated schedules for energy savings in high-performance processors", In Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED), Seoul, Korea, Aug 2003, pp. 414-419. (Acceptance rate: 90 accepted/221 submissions = 41%)
37. Tao Li and Lizy Kurian John, "Routine based OS-aware Microprocessor Resource Adaptation for Run-time Operating System Power Saving", In Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED), Seoul, Korea, Aug 2003, pp. 241-246. (Acceptance rate: 90 accepted/221 submissions = 41%)
38. S. Kim, N. Vijaykrishnan, M. J. Irwin, and L. K. John, "On Load Latency in Low-Power Caches", In Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED), Seoul, Korea, Aug 2003, pp. 258-261. (Acceptance rate: 90 accepted/221 submissions = 41%)
39. Tao Li and Lizy Kurian John, "Run-time Modeling and Estimation of Operating System Power Consumption", In Proceedings of the International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), 2003, pp. 160-171. (Acceptance rate: 26 accepted/222 submissions = 12%)
40. Ravi Bhargava and Lizy K. John, "Improving Dynamic Cluster Assignment for Clustered Trace Cache Processors", In Proceedings of the 30th International Symposium on Computer Architecture (ISCA 2003), June 2003, pp. 264-274. (Acceptance rate: 36 accepted/184 submissions = 20%)
41. Robert H. Bell, Jr. and Lizy Kurian John, "Interface Design Techniques for Single Chip Systems", In Proceedings of the Sixteenth IEEE Conference on VLSI Design, January 2003, pp. 388-394. (Acceptance rate: 84 accepted/210 submissions = 40%)
42. Tao Li, Lizy John, Anand Sivasubramaniam, Narayanan Vijaykrishnan and Juan Rubio, "Understanding and Improving Operating System Effects in Control Flow Prediction", In Proceedings of the Tenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-X), 2002, pp. 68-80. (Acceptance rate: 24 accepted/130 submissions = 18%)
43. Tao Li, Lizy John and Robert H. Bell, Jr., "Modeling and Evaluation of Control Flow Prediction Schemes Using Complete System Simulation and Java Workloads", In Proceedings of the tenth IEEE/ACM International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS), 2002, pp. 391-400. (Acceptance rate: 51 accepted/180 submissions = 28%)
44. Tao Li, Ravi Bhargava and Lizy John, "Rehashable BTB: An Adaptive Branch Target Buffer to Improve the Target Predictability of Java Code", In Proceedings of the International Conference on High Performance Computing (HiPC), 2002, pp. 597-608. (Acceptance rate: 57 accepted/145 submissions = 39%)
45. Eugene B. John, Stefan Petko, Lizy John and Jason Law, "Access Time and Energy Tradeoffs for Caches in High Frequency Microprocessors", In Proceedings of 45th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Tulsa, Oklahoma, Aug 2002, pp. 421- 424 (vol.3).
46. Byeong Kil Lee, Lizy John, "Implications of Programmable General Purpose Processors for Compression/Encryption Applications", IEEE 13th International Conference on Application-specific Systems, Architectures and Processors (ASAP 2002), San Jose, California, July 2002, pp. 233-242.
47. Ravi Bhargava and Lizy John, "Latency and Energy Aware Value Prediction for High-Frequency Processors", In Proceedings of 16th ACM International Conference on Supercomputing (ICS), June 2002, pp. 45-56. (Acceptance rate: 31 accepted/144 submissions = 22%)
48. Sudhanva Gurumurthi, Anand Sivasubramaniam, Mary Jane Irwin, Narayanan Vijaykrishnan, Mahmut Kandemir, Tao Li, and Lizy Kurian John, "Using Complete Machine Simulation for Software Power

- Estimation: The SoftWatt Approach”, In Proceedings of the 2002 International Symposium on High Performance Computer Architecture (HPCA), Feb 2002, pp. 141-150. (Acceptance rate: 26 accepted/130 submissions = 20%)
49. Robert H. Bell, Jr., Chang Yong Kang, Lizy John, Earl E. Swartzlander, Jr., “CDMA as a Multiprocessor Interconnect Strategy”, Proceedings of the Thirty-Fifth Asilomar Conference on Signals, Systems, and Computers, Nov 2001, pp. 1246-1250 (vol. 2).
  50. Y. Luo and L. John, “Workload Characterization of multithreaded Java Servers”, International Symposium on Performance Analysis of Software and Systems (ISPASS), 2001, pp. 128-136. (Acceptance rate: 20 accepted/68 submissions = 29%)
  51. Tao Li and L. John, “Understanding the Control Flow Transfer and its Predictability in Java Processing”, International Symposium on Performance Analysis of Software and Systems (ISPASS), 2001, pp. 65-76. (Acceptance rate: 20 accepted/68 submissions = 29%)
  52. D. Talla and L. John, “Cost-effective Hardware Acceleration of Multimedia Applications”, International Conference on Computer Design (ICCD 2001), Sept 2001, pp. 415-424. (Acceptance rate: 61 accepted/181 submissions = 34%)
  53. R. Radhakrishnan, R. Bhargava, and L. K. John, “Improving Java Performance using Hardware Translation”, Proceedings of the International Conference on Supercomputing (ICS 2001), Italy, June 2001, pp. 427-439. (Acceptance rate: 45 accepted/133 submissions = 34%)
  54. Serene Banerjee, Lizy K. John, and Brian L. Evans, “The EASE Branch Predictor”, Proceedings of the International Conference on Communications, Computers & Devices, Dec 2000. (Acceptance rate: 69 accepted/181 submissions = 38%)
  55. S. Banerjee, H. R. Sheikh, L. K. John, B. L. Evans, and A. C. Bovik, “VLIW DSP vs. Superscalar Implementation of a Baseline H.263 Video Encoder”, Proc. IEEE Asilomar Conf. on Signals, Systems, and Computers, vol. 2, Pacific Grove, CA, Oct 29-Nov 1, 2000, pp. 1665-1669.
  56. D. Talla, L. John, V. Lapinskii and B. Evans, “Evaluating Signal Processing and Multimedia Applications on SIMD, VLIW and Superscalar Architectures”, In Proceedings of the IEEE International Conference on Computer Design (ICCD 2000), Sept 2000, pp. 163-172. (Acceptance rate: 69 accepted/181 submissions = 38%)
  57. R. Radhakrishnan, D. Talla, L. John, “Allowing for ILP in an Embedded Java Processor”, Proceedings of the ACM/IEEE International Symposium on Computer Architecture (ISCA2000), Vancouver, Canada, June 2000, pp. 294-305. (Acceptance rate: 29 accepted/166 submitted = 17%)
  58. L. Tao, L. K. John, N. Vijaykrishnan, A. Sivasubramaniam, A. Murthy, and J. Sabarinathan, “Using Complete System Simulation to Characterize SPECjvm98 Benchmarks”, Proceedings of the ACM International Conference on Supercomputing (ICS 2000), Santa Fe, New Mexico, May 2000, pp. 22-33. (Acceptance rate: 33 accepted/122 submissions = 28%)
  59. R. Bhargava and L. K. John, “Issues in the Design of Store Buffers in Dynamically Scheduled Processors”, In Proceedings of IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2000), Austin, TX, April 24-25 2000, pp. 76-87.
  60. D. Talla and L. K. John, “Execution Characteristics of Multimedia Applications on a Pentium II Processor”, Proceedings of the IEEE International Performance, Computing and Communications Conference (IPCCC), Phoenix, AZ, Feb 2000, pp. 516-523.
  61. R. Radhakrishnan, N. Vijaykrishnan, L. K. John and A. Sivasubramaniam, “Architectural Issues in Java Runtime Systems”, Proceedings of the IEEE International Symposium on High Performance Computer Architecture (HPCA-2000), Toulouse, France, Jan 2000, pp. 387-398. (Acceptance rate: 35 accepted/163 submissions = 21%)
  62. D. Talla, S. Rao and L. John, “An Evolutionary Computation Embedded IIR LMS Algorithm”, International Conf on Signal Processing Applications and Technology (ICSPAT), Orlando, FL, Nov 1999.
  63. M. Clark and L. K. John, “Performance Evaluation of Configurable Hardware Features on the AMD-K5”, In Proceedings of the IEEE International Conference on Computer Design (ICCD 99), Oct 1999, pp. 102-107. (Acceptance rate: 71 accepted/220 submissions = 32%)

64. S. Srivatsan, and L. John, "On the Use of Pseudorandom Sequences for High Speed Resource Allocators in Superscalar Processors", Proceedings of the IEEE International Conference on Computer Design (ICCD 99), Oct 1999, pp. 124-130. (Acceptance rate: 71 accepted/220 submissions = 32%)
65. R. Radhakrishnan, J. Rubio and L. John, "Characterization of Java Applications at ByteCode and UltraSPARC Machine Code Levels", ICCD 1999, Oct 1999, pp. 281-284. (Acceptance rate: 71 accepted/220 submissions = 32%)
66. G. E. Allen, B. L. Evans, and L. K. John, "Real-Time High-Throughput Sonar Beamforming Kernels Using Native Signal Processing and Memory Latency Hiding Techniques", Proc. IEEE Asilomar Conf on Signals, Systems and Computers, Pacific Grove, CA, Oct 24-27, 1999, pp. 137-141.
67. D. Talla and L. John, "Quantifying Effectiveness of MMX in Native Signal Processing", IEEE Midwest Symposium on Circuits and Systems, Aug 1999.
68. H. Nguyen and L. John, "Exploiting SIMD Parallelism in DSP and Multimedia Algorithms Using the AltiVec Technology", Proceedings of the ACM International Conference on Supercomputing (ICS 99), Greece, June 1999, pp. 11-20. (Acceptance rate: 57 accepted/180 submissions = 32%)
69. R. Radhakrishnan and L. John, "A Performance Study of Modern Web Server Applications", Euro-Par 1999, Lecture Notes in Computer Science, Springer, pp. 239-247. (Acceptance rate: 188 accepted/343 submissions = 55%)
70. D. Talla and L. K. John, "Performance Evaluation and Benchmarking of Native Signal Processing", Euro-Par 1999, Lecture Notes in Computer Science, Springer, pp. 266-270. (Acceptance rate: 188 accepted/343 submissions = 55%)
71. R. Shalem, E. John and L. K. John, "A Novel Low Power Static Energy recovery Full Adder Cell", Proceedings of the 1999 IEEE Great Lakes Symposium on VLSI, Michigan, March 1999, pp. 380-383.
72. B. Grayson, L. John and C. Chase, "The Effects of Memory-Access Ordering on Multiple-Issue Uniprocessor Performance", Proceedings of the IEEE Performance, Computers and Communications Conference (IPCCC), Feb 1999, pp. 293-302.
73. R. Bhargava, L. K. John and F. Matus, "Accurately Modeling Speculative Instruction Fetching in Trace-Driven Simulation", Proceedings of the IEEE Performance, Computers and Communications Conference (IPCCC), Feb 1999, pp. 65-71.
74. D. Tang, A. M. G. Maynard and L. K. John, "Contrasting Branch Characteristics and Branch Predictor Performance of C++ and C Programs", Proceedings of the IEEE Performance, Computers and Communications Conference (IPCCC), Feb 1999, pp. 275-283.
75. S. Srinivasan, P. Chabra, P. Jaini, A. Aziz and L. John, "Formal Verification of Snoop-based Cache Coherence Protocol using Symbolic Model Checking", in the Proceedings of the 12th International Conference on VLSI Design (Published by IEEE Computer Society), India, Jan 1999, pp. 288-293. (Acceptance rate: 75 accepted/194 submissions = 39%)
76. R. Bhargava, L. K. John, B. L. Evans, and R. Radhakrishnan, "Evaluating MMX Technology using DSP and Multimedia Applications", Proceedings of the IEEE Symposium on Microarchitecture (MICRO-31), Dallas, Texas, Dec 1998, pp. 37-46. (Acceptance rate: 28 accepted/108 submissions = 26%)
77. R. Radhakrishnan and L. John, "Execution Characteristics of Object Oriented Programs on the UltraSPARC-II", Proceedings of the 5th International Conference on High Performance Computing (Published by IEEE Computer Society), Dec 1998, pp. 202-211. (Acceptance rate: 62 accepted/104 submissions = 60%)
78. L. John, Y. Teh, F. Matus and C. Chase, "Code Coalescing Unit: A Mechanism to Facilitate Load Store Data Communication", Proceedings of IEEE International Conference on Computer Design, Oct 1998, pp. 550-557. (Acceptance rate: 69 accepted/189 submissions = 36%)
79. G. Beers and L. John, "A Novel Memory Bus Driver/Receiver Architecture for Higher Throughput", Proceedings of the International Conference on VLSI Design (Published by IEEE Computer Society), Jan 1998, pp. 259-264. (Acceptance rate: 57 accepted/123 submissions = 46%)
80. A. Kulkarni, N. Chander, S. Pillai, L. John, "Modeling and Analysis of the Difference-Bit Cache", Proceedings of the Great Lakes Symposium on VLSI, 1998, pp. 140-145.

81. E. John, F. Hudson and L. K. John, "Hybrid Tree: A Salable Optoelectronic Interconnection Network for Parallel Computing", Proceedings of the Hawaii International Conference on System Sciences, Jan 1998, Vol. VII, pp. 466-474. (Acceptance rate: 75 accepted/181 submissions = 41%)
82. L. John and A. Subramanian, "Design and Performance Evaluation of a Cache Assist to implement Selective Caching", Proceedings of the IEEE International Conference on Computer Design, Oct 1997, pp. 510-518. (Acceptance rate: 91 accepted/175 submissions = 52%)
83. Lizy Kurian-John and R. Radhakrishnan, "Improving the Parallelism and Concurrency in Decoupled Architectures", Proceedings of the IEEE Symposium on Parallel and Distributed Processing, New Orleans, Oct 1996, pp. 130-137. (Acceptance rate: 84 accepted/217 submissions = 39%)
84. L. K. John, "VaWiRAM: A Variable Width Random Access Memory Module", Proceedings of the 9th International Conference on VLSI Design, Jan 1996, pp. 219-224. (Acceptance rate: 75 accepted/137 submissions = 55%)
85. L. K. John, R. Reddy, V. Kammila, and P. Maurer, "Investigating the Use of Cache as a Local Memory", Proceedings of the International High Performance Computing Conference (HiPC), Dec 1995, pp. 117-122. (Acceptance rate: 126 accepted/213 submissions = 59%)
86. L. K. John, V. Reddy, P. Hulina and L. Coraor, "Program Balance and its Impact on High Performance RISC Architectures", Proceedings of the International Symposium on High Performance Computer Architecture (HPCA), Jan 1995, pp. 370-379. (Acceptance rate: 36 accepted/190 submissions = 19%)
87. L. Kurian, D. Brewer, and E. John, "Design of a Highly Reconfigurable Interconnect for Array Processors", Proceedings of the 8th International Conference on VLSI Design, Jan 1995, pp. 321-325. (Acceptance rate: 77accepted/139 submissions = 55%)
88. L. K. John, V. Reddy, P. T. Hulina and L. D. Coraor, "A Comparative Evaluation of Software Techniques to Hide Memory Latency", Proceedings of the 28th Hawaii International Conference on System Sciences (HICSS), Jan 1995, Vol. I, 229-238.
89. L. Kurian and Y. Liu, "Performance Model for a Prioritized Multiple-Bus Multiprocessor System", Proceedings of the IEEE Symposium on Parallel and Distributed Processing (IPDPS), Oct 1994, pp. 577-584.
90. L. Kurian, B. Choi, P. T. Hulina, and L. D. Coraor, "Module Partitioning and Interlaced Data Placement Schemes to Reduce Conflicts in Interleaved Memories", Proceedings of the 23rd International Conference on Parallel Processing, Aug 1994, Vol. I, pp. 212 - 219.
91. L. Kurian, P. T. Hulina and L. D. Coraor, "Memory Latency Effects in Decoupled Architectures with a Single Data Memory Module", Proc. of the 19th Intl. Symposium on Computer Architecture (ISCA), Australia, May 1992, pp. 236-245.
92. L. Kurian and M. J. Thazhuthaveetil, "Effect of Hot Spots on Multiprocessor Systems using Circuit Switched Interconnection Networks", Proceedings of the 20th International Conference on Parallel Processing, Aug 1991, Vol. I, pp. 554 - 557.
93. L. Kurian, P. T. Hulina, L. D. Coraor and D. N. Mannai, "Classification and Performance Evaluation of Instruction Buffering Techniques", Proceedings of the 18th International Symposium on Computer Architecture (ISCA), Toronto, Canada, May 1991, pp. 150-159

### C. Other Major Publications

#### Invited Conference Papers:

1. Juan Rubio and Lizy K. John, "Understanding the Execution of a Radar Motion Indication Application", Proceedings of International Conference on Parallel and Distributed Systems (ICPADS) 2004.
2. Deepu Talla and Lizy John, "Facts and myths about media processing on general-purpose processors", In Proceedings of IEEE International Conference on Information Technology: Research and Education (Special Session on Technology and Trends in Media Processing), Newark, NJ, Aug 10-13: 2003

#### Other Conference and Workshop Papers:

1. Dimitris Kaseridis and Lizy John, Performance Analysis of Multiple Threads/Cores Using the UltraSPARC T1", Workshop on Unique Chips and Systems (UCAS-4), April 20th, 2008, Austin
2. Ajay Joshi, Lieven Eeckhout, Lizy John, and Ciji Isen. Stressing Microarchitectures Through Custom Benchmark Synthesis, *IBM Center for Advanced Studies (IBM CAS)*, 2008.
3. Ajay Joshi, Lieven Eeckhout, and Lizy John. The Return of Synthetic Benchmarks. *Standard Performance Evaluation Corporation Benchmark Workshop*, January 2008.
4. Ciji Isen, Lizy K. John, On the Object Orientedness of C++ Programs in SPEC CPU 2006, *Standard Performance Evaluation Corporation Benchmark Workshop*, January 2008.
5. Sarah Bird, Aashish Phansalkar, Lizy K. John, Alex Mericas, Rajeev Indukuru , Characterization of Performance of SPEC CPU Benchmarks on Intel's Core Microarchitecture based Processor, SPEC Workshop January 2007
6. Ajay Joshi, Lieven Eeckhout, Robert H. Bell Jr., and Lizy John, Performance Cloning: A Technique for Disseminating Proprietary Applications as Benchmarks, 8<sup>th</sup> annual IBM CAS Conferences, March 2007
7. Sarah Bird, Aashish Phansalkar, Lizy K. John, Performance Characterization of SPEC CPU Benchmarks on Intel's Core Microarchitecture based processor, 8<sup>th</sup> Annual IBM CAS Conference March 2, 2007
8. Jian Chen, Nidhi Nayyar, and Lizy K. John, Mapping of Applications to Heterogeneous Multi-cores Based on Micro-architecture Independent Characteristics, Third Workshop on Unique Chips and Systems (UCAS), Held in conjunction with IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), April 2007.
9. Dimitris Kaseridis and Lizy K. John. CMP/CMT Scaling of SPECjbb2005 on UltraSPARC T1 Tenth Workshop on Computer Architecture Evaluation using Commercial Workloads, February 2007
10. Brian Gaide and Lizy John, A High Throughput Self-Timed FPGA Core Architecture, Digest of UCAS-2 (Workshop on Unique Chips and Systems), held in conjunction with ISPASS 2006, March 2006
11. Ajay Joshi, Rob Bell Jr., and Lizy K. John, "Capturing Locality of Reference and Branch Predictability of Programs in Synthetic Workloads", IBM Center for Advanced Studies (CAS) Conference, Feb 2006.
12. Rob Bell, Jr., Rajiv R. Bhatia, Lizy K. John, Jeff Stuecheli, John Griswell, Paul Tu, Louis Capps, Anton Blanchard, Ravel Thai, "Automatic Testcase Synthesis and Performance Model Validation for High-Performance PowerPC Processors", IBM Center for Advanced Studies (CAS) Conference, Feb 2006.
13. Aashish Phansalkar and Lizy K. John, "Performance Prediction using Program Similarity", SPEC workshop, Jan 2006.
14. Joshua J. Yi, Ajay Joshi, Resit Sendag, Lieven Eeckhout, and David J. Lilja, "Analyzing the Processor Bottlenecks in SPEC CPU 2000" 2006 SPEC Benchmark Workshop, Jan 2006.
15. W. L. Bircher, J. Law, M. Valluri and Lizy K. John, "Effective Use of Performance Monitoring Counters for Run-Time Prediction of Power", Poster in IBM Austin Conference on Energy-Efficient Design (ACEED) 2005 IBM, Austin, March 2005.
16. A. Phansalkar, A. Joshi, L. Eeckhout and L. John, "Measuring Program Similarity: Experiments with SPEC CPU benchmark suites", Proceedings of the IBM Center for Advanced Studies (CAS) Conference, Austin, TX, Feb 2005.
17. R. Bell Jr and L. K. John, "Capturing the Essence of Benchmarks: A New Approach to benchmark Synthesis", Proceedings of the IBM Center for Advanced Studies (CAS) Conference, Austin, TX, Feb 2005.
18. Robert H. Bell Jr., Lieven Eeckhout, Lizy K. John, and Koen De Bosschere, "Deconstructing and Improving Statistical Simulation in HLS", Third Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD), along with ISCA June 2004.

19. Madhavi Valluri and Lizy John, "Hybrid-Scheduling: A Compile-Time Approach for Energy-Efficient Superscalar Processors", Poster in IBM Austin Conference on Energy-Efficient Design (ACEED) 2004 IBM, Austin, TX, March 2-4, 2004.
20. Yue Luo and Lizy John, "Using Statistical Theory to Study Issues in Microprocessor Simulation", Proceedings of the Fifth Annual Austin Center for Advanced Studies Conference (CAS), Feb 2004.
21. Ravi Bhargava and Lizy K. John, "Performance and Energy Impact of Instruction-Level Value Predictor Filtering", In Proceedings of the First Value-Prediction Workshop (VPW1) [held with ISCA 03], June 2003.
22. Shiwen Hu, Ravi Bhargava, and Lizy K. John, "The Role of Return Values in Exploiting Speculative Method-Level Parallelism", In Proceedings of the First Value-Prediction Workshop (VPW1) [held with ISCA'03], June 2003.
23. Shiwen Hu, Lizy John, "Comparison of JVM Phases on Data Cache Performance", In the First Workshop on Managed Run Time Workloads, San Francisco, CA, March 2003.
24. Yue Luo and Lizy K. John, "Automatically Selecting Representative Traces for Simulation Based on Cluster Analysis of Instruction Address hashes", IBM CAS Conference, Feb 2003.
25. Pattabi Seshadri, Lizy John and Alex Mericas, "Workload Characterization of Java Server Applications on Two PowerPC Processors", In Proceedings of the Third Annual Austin Center for Advanced Studies Conference, Austin, TX, Feb 15, 2002.
26. Lizy John, "Contemporary Performance Evaluation: Overwhelming Effort? Irrelevant Results?" "Position paper, NSF workshop, Dec 2001.
27. Deepu Talla and Lizy John, "A decoupled architecture for accelerating multimedia applications, Proceedings of Workshop on Memory Access Decoupled Architectures" in conjunction with IEEE International Conference on Parallel Architectures and Compilation Techniques, Barcelona, Spain, Sept 8, 2001. (Selected as one of 2 best papers)
28. P. Sheshadri and L. K. John, "Characterization of Web Server Workloads on Three Generations of IBM PowerPC Microarchitectures", IBM Center for Advanced Studies Conference, Feb 2001.
29. Mike Clark, Ajaya Durg, Kevin Lienenbrugger, and Lizy John, "Evaluation of TPC-H benchmark on Athlon based systems", Fourth Workshop on Computer Architecture Evaluation using Commercial Workloads, Monterrey, Mexico, Jan 21st, 2001.
30. Yue Luo and Lizy K. John, "Performance Impact of Multithreaded Java Server Applications", Fourth Workshop on Computer Architecture Evaluation using Commercial Workloads, Monterrey, Mexico, Jan 21st, 2001.
31. M. Valluri and L. John, "Is Compiling for Performance == Compiling for Power?" The 5th Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT-5), Monterrey, Mexico, Jan 20, 2001.
32. L. K. John, J. Rubio, "Effectiveness of Out of Order Scheduling in the IBM PowerPC Processors", IBM Center for Advanced Studies Inaugural Conference, July 2000.
33. P. Sheshadri and L. K. John, "Characterization of Web Server Workloads on Three Generations of IBM PowerPC Microarchitectures", IBM Center for Advanced Studies Inaugural Conference, July 2000.
34. R. Radhakrishnan and L. K. John, "A Decoupled Translate Execute (DTE) Architecture to Improve Performance of Java Execution", Workshop on Hardware Support for Objects and Microarchitectures for Java, Held in conjunction with the International Conference on Computer Design (ICCD) 1999, Oct 10, 1999, pp. 25-29.
35. R. Radhakrishnan and L. K. John, "Web Workload Characterization at a Microarchitectural Level", Workshop on Commercial Workload Characterization, Held In Conjunction with the 1999 High Performance Computer Architecture Symposium, Jan 1999.
36. R. Bhargava, R. Radhakrishnan, B. L. Evans, and L. K. John, "Characterization of MMX-Enhanced DSP and Multimedia Applications on a General Purpose Processor", Digest of the Workshop on Performance Analysis and its Impact on Design (held in conjunction with ISCA 98), June 1998, pp. 16-23.

37. R. Radhakrishnan, D. Tang and L. John, "Understanding the Branch Performance of Object Oriented Workloads", Digest of the Workshop on Performance Analysis and its Impact on Design (held in conjunction with ISCA 98), June 1998.
38. L. K. John, "The Undergraduate Curriculum in the Electrical and Computer Engineering Department at the University of Texas at Austin", Digest of the Workshop on Computer Architecture Education (held in conjunction with ISCA 98), June 1998.
39. L. Nguyen, T. Nguyen, L. K. John and S. Srivatsan, "FPGA Model of MIPS R2000 CPU", Proceedings of ASEE-GSW conference, March 1998, pp. 55-60. This paper won the best paper award at the conference.
40. A. Dewhirst, D. Nguyen, H. Tran, L. John and S. Srivatsan, "VHDL Model of MIPS R2000 CPU", Proceedings of ASEE-GSW conference, March 1998, pp. 51-55.
41. L. John, "Experience Teaching a Senior Level Course on Digital Design Using FPGAs", Proceedings of IEEE International Conference on Microelectronic Systems Education (MSE 97), Crystal City, Virginia, July 1997, pp. 97-98.
42. L. John and R. Radhakrishnan, "c\_ICE: A Compiler-based Instruction Cache Exclusion Scheme", Proceedings of the Workshop on Interaction between Compilers and Computer Architecture, held in connection with HPCA Symposium, Feb 1997.
43. L. Kurian, Paul T. Hulina, and Lee D. Coraor, "Expected and Obtained Performance from Decoupled Architectures", Supercomputing Conference, Nov 1992.
44. L. Kurian, Paul T. Hulina and Lee D. Coraor, "Role of an Access Processor in a RISC Environment", Poster Session of the ACM International Supercomputing conference, Minneapolis, MN, Nov 1992.

#### D. Books, Chapters of Books; Editor of Books (identify whether author or editor????)

##### Book Authored:

1. Digital Systems Design Using VHDL, Charles Roth and Lizy K. John, 2<sup>nd</sup> edition (Thompson Engineering, 2006-2007, 580 pages)

##### Books Edited:

1. Computer Performance Evaluation and Benchmarking, CRC Press, 2005 (289 pages)
2. Workload Characterization of Emerging Computer Applications, Kluwer Academic Publishers, 2001, ISBN 0-7923-7315-4
3. Workload Characterization for Computer System design, edited by L. K. John and A. M. Maynard, Kluwer Academic Publishers, 2000, 209 pages, ISBN 0-7923-7777-x.
4. Workload Characterization: Methodology and Case Studies, edited by L. John and A. M. Maynard, IEEE Computer Society, 153 pages, ISBN 0-7695-0452-3

##### Book Chapters:

1. Lloyd Bircher and Lizy K. John, Measurement Based Power Phase Analysis, Chapter 7, Unique Chips and Systems, Taylor and Francis, 2007
2. Brian Gaide and Lizy K. John, A High-Throughput Self-Timed FPGA Core Architecture, Chapter 5, Unique Chips and Systems, Taylor and Francis, 2007
3. Chapter 1, Performance Evaluation Methodology, Computer Performance Evaluation and Benchmarking, CRC Press, 2005 (coauthor with Lieven Eeckhout)
4. Chapter 2, Performance Evaluation Methodology, Computer Performance Evaluation and Benchmarking, CRC Press, 2005 (sole author)
5. Chapter 3, Benchmarks, Computer Performance Evaluation and Benchmarking, CRC Press, 2005 (sole author)

6. Chapter 4, Aggregating Performance over a Benchmark Suite, Computer Performance Evaluation and Benchmarking, CRC Press, 2005 (sole author)
7. Ramesh Radhakrishnan, Lizy John, Ravi Bhargava, and Deepu Talla, Improving Java performance in embedded and general-purpose processors, Java Microarchitectures (Chapter 5), edited by N. Vijaykrishnan and M. Wolczko, pp. 79-104, Kluwer Academic Publishers, 2002
8. Lizy K. John, Article on Performance Evaluation, in Computer Engineering Handbook (Invited) (Sole Author)
9. M. Valluri and L. John, "Is Compiling for Performance == Compiling for Power?", Chapter 6, in Interaction between Compilers and Computer Architectures, edited by Gyunggho Lee and Pen-Chung Yew, Kluwer Academic Publishers, 2001, ISBN 0-7923-7370-7
10. Tao Li, Lizy K. John, N. Vijaykrishnan, and A. Sivasubramaniam, Characterizing Operating System Activity in SPECjvm98 Benchmarks, Book Chapter in Characterization of Contemporary Workloads, pages 53-82, Kluwer Academic Publishers, 2001, ISBN 0-7923-7315-4
11. R. Bhargava, J. Rubio, S. Kannan, L. K. John, D. Christie, and L. Klaes, "Understanding the Impact of x86/NT Computing on Microarchitecture", Book Chapter in Characterization of Contemporary Workloads, pages 203- 228, Kluwer Academic Publishers, 2001, ISBN 0-7923-7315-4
12. Article on Harvard Architecture, in the EE Encyclopedia, John Wiley and Sons, 2000 (Invited Article) (sole author)
13. Article on Bus Architectures, The Encyclopedia of Life Support Systems, UNESCO project (Invited Article) (sole author)
14. Workload Characterization: Motivation, Goals and Methodology, pages 3-14, in Workload Characterization: Methodology and Case Studies, edited by L. John and A. Maynard, IEEE Computer Society, ISBN 0-7695-0452-3
15. Article on Bit-Slice Computers, in the EE Encyclopedia, John Wiley and Sons, 1999 (Invited Article), pp. 39-44 ISBN 0471-35895-9 (sole author)
16. Classification and Performance Evaluation of Instruction Buffering Techniques, in Performance Modeling for Computer Architects, edited by C. M. Krishna, IEEE Computer Society Press. Pages 94-103. ISBN 0-8186-7094-0

#### \*E. Reviews

#### \*F. Technical Reports

1. Ajay Joshi, Aashish Phansalkar, Lieven Eeckhout, and Lizy John, "Measuring Benchmark Similarity Using Inherent Program Characteristics, Technical Report TR-060201-0, Feb 2006.
2. Yue Luo and Lizy John, "Simulating Java Commercial Throughput Workload: A Case Study", Technical Report TR-050710-01. July 2005.
3. Yue Luo, Ajay Joshi, Aashish Phansalkar, Lizy John, and Joydeep Ghosh, "Analyzing and Improving Clustering Based Sampling for Microprocessor Simulation", Technical Report TR-050301-01. March 2005.
4. Aashish Phansalkar, Ajay Joshi, Lieven Eeckhout, and Lizy K. John, "Measuring Program Similarity", Technical Report TR-050127-01, Laboratory for Computer Architecture, The University of Texas at Austin, Jan 2005.
5. W. L. Bircher, J. Law, M. Valluri and Lizy K. John, "Effective Use of Performance Monitoring Counters for Run-Time Prediction of Power", Technical Report TR-041104-01, Laboratory for Computer Architecture, The University of Texas at Austin, Nov 2004.
6. Aashish Phansalkar, Ajay Joshi, Lieven Eeckhout, and Lizy K. John, "Four Generations of SPEC CPU Benchmarks: What has changed and what has not", Technical Report TR-041026-01-1, Laboratory for Computer Architecture, The University of Texas at Austin, Oct 2004.

7. Robert H. Bell, Jr., and Lizy K. John, "Experiments in Automatic Benchmark Synthesis", Technical Report TR-040817-01, Laboratory for Computer Architecture, The University of Texas at Austin, Aug 2004.
8. Yue Luo and Lizy K. John, "Using Statistical Theory to Study Issues in Microprocessor Simulation", Technical Report TR-0400225-01, Laboratory for Computer Architecture, The University of Texas at Austin, Feb 2004.
9. Lizy K. John, "More on finding a Single Number to indicate Overall Performance of a Benchmark Suite", Technical Report TR-040126-01, Laboratory for Computer Architecture, The University of Texas at Austin, Jan 2004.
10. Aashish Phansalkar and Lizy Kurian John, "Analyzing Program Behavior of SPECint2000 Benchmark Suite using Principal Components Analysis", Technical Report TR-040122-01, Laboratory for Computer Architecture, The University of Texas at Austin, Jan 2004.
11. Ajay Joshi, Srirarm Sambamurthy, Saket Kumar, and Lizy John, "Power Modeling in SDRAMs", Technical Report TR-040126-02, Jan 2004.
12. Robert H. Bell, Jr. and Lizy Kurian John, "Basic Block Simulation Granularity, Basic Block Maps, and Benchmark Synthesis Using Statistical Simulation", Technical Report TR-031119-01, Laboratory for Computer Architecture, The University of Texas at Austin, Nov 2003.
13. Byeong Kil Lee and Lizy John, "Development and Characterization of Control-Plane Network Workloads", Aug 2003
14. Juan Rubio and Lizy K. John, "Using Simulated Annealing to Guide Server Data Placement", Technical Report TR-030731-01, Laboratory for Computer Architecture, The University of Texas at Austin, July 2003.
15. Shiwen Hu and Lizy K. John, "Avoiding Store Misses to Fully Modified Cache Blocks", Technical Report TR-030701-01, Laboratory for Computer Architecture, The University of Texas at Austin, July 2003.
16. Ravi Bhargava and Lizy K. John, "Cluster Assignment Strategies for a Clustered Trace Cache Processor", Technical Report TR-030331-01, Laboratory for Computer Architecture, The University of Texas at Austin, March 2003.
17. Tao Li and Lizy John, "Run-time Modeling and Estimation of Operating System Power Consumption", Technical Report TR-1101-02, Laboratory for Computer Architecture, The University of Texas at Austin, Nov 2002.
18. Shiwen Hu, Ravi Bhargava and Lizy Kurian John, "The Role of Return Value Prediction in Exploiting Speculative Method-Level Parallelism", Technical Report TR-020822-02, Laboratory for Computer Architecture, The University of Texas at Austin, Aug 2002.
19. Anand S. Rajan, Juan Rubio and Lizy K. John, "Cache Performance in Java Virtual Machines: A Study of Constituent Phases", Technical Report TR-020822-01, Laboratory for Computer Architecture, The University of Texas at Austin, Aug 2002.
20. Jason Law and Byeong Kil Lee, "Access Time and Power Characteristics of Various Future File Configurations", Technical Report TR-020821-01, Laboratory for Computer Architecture, The University of Texas at Austin, Aug 2002.
21. Yue Luo, Pattabi Seshadri, Juan Rubio, Lizy John and Alex Mericas, "A Case Study of 3 Internet Benchmarks on 3 Superscalar Machines", Technical Report TR-020817-01, Laboratory for Computer Architecture, The University of Texas at Austin, Aug 2002.
22. Juan Rubio, Madhavi Valluri and Lizy John, "Improving Transaction Processing using a Hierarchical Computing Server", Technical Report TR-020719-01, Laboratory for Computer Architecture, The University of Texas at Austin, July 2002.
23. Madhavi Gopal Valluri and Lizy John, "A Hybrid-Scheduling Approach for Low-Energy Superscalar Processors", Technical Report TR-020617-01, Laboratory for Computer Architecture, The University of Texas at Austin, June 2002.

24. Eugene B. John, Stefan Petko, Lizy John and Jason Law, "Access Time and Energy Tradeoffs for Caches in High Frequency Microprocessors", Technical Report TR-020607-01, Laboratory for Computer Architecture, The University of Texas at Austin, June 2002.
25. Tao Li, Lizy John, Anand Sivasubramaniam and Vijaykrishnan Narayanan, "Understanding and Improving Operating System Effects in Control Flow Prediction", Technical Report TR-000630-02, Laboratory for Computer Architecture, The University of Texas at Austin, June 2002.
26. Ravi Bhargava, Juan Rubio and Lizy John, "Traveling Speculations: An Integrated Prediction Strategy for Wide-Issue Microprocessors", Technical Report TR-020524-01, Laboratory for Computer Architecture, The University of Texas at Austin, May 2002.
27. Ravi Bhargava and Lizy John, "Value Prediction Design for High-Frequency Microprocessors", Technical Report TR-020508-01, Laboratory for Computer Architecture, The University of Texas at Austin, May 2002.
28. Byeong Kil Lee and Lizy John, "Implications of Programmable General Purpose Processors for Compression/Encryption Applications", Technical Report LCA-TR-020315, Laboratory for Computer Architecture, The University of Texas at Austin, 2002.
29. Deepu Talla, Lizy John, and Doug Burger, "Hardware support to reduce overhead in fine-grain media codes", Technical Report LCA-TR-011101, Laboratory for Computer Architecture, The University of Texas, Austin, Nov 2001.
30. Yue Luo and Lizy John, "Workload Characterization of Multithreaded Java Servers", Technical Report TR-010815-01, Laboratory for Computer Architecture, The University of Texas at Austin, Aug 2001.
31. Juan Rubio and Lizy John, "Hierarchical Computing: An Architecture for Efficient Transaction Processing", Technical Report UT-CERC-TR-01-1, Computer Engineering Research Center, The University of Texas at Austin, Jan 29, 2001.
32. Ramesh Radhakrishnan, Juan Rubio, N. Vijaykrishnan and Lizy John, "Execution Characteristics of JIT Compilers", Technical Report TR-990717-01, Laboratory for Computer Architecture, The University of Texas at Austin.
33. Ravi Bhargava, Lizy John, and Francisco Matus, "Exploiting Instruction Reuse to Enhance Microprocessor Simulation", Technical Report TR-981223-01, Laboratory for Computer Architecture, The University of Texas at Austin, Dec 1998.
34. Sanjeev Ghai, Jody Joyner, and Lizy K. John, "Investigating the Effectiveness of a Third Level Cache", Technical Report TR-980501-01, May 1998.

**\*ORAL PRESENTATIONS:** (List co-authors, title of presentation, where given, and dates)

1. Tech Area Night Presentation, Embedded Systems Area, April 2008, ECE Department
2. "Chip Design", Camp Texas, Aug 21, 2008
3. "Workload Characterization for Effective Computer System Design", Computer Science Colloquium, The University of Texas at El Paso, Apr 18, 2008
4. "Graduate School: How to Enter and Succeed", Talk given to IEEE Meeting, The University of Texas at El Paso, Apr 18, 2008.
5. "Performance Evaluation and Benchmarking: The Return of Synthetic Benchmarks", Keynote speech, IBM Center for Advanced Studies (CAS) Conference, Feb 22, 2008
6. Performance Evaluation and Benchmarking, Talk given at [UT@IBM: Building Collaboration, Creating Impact](#), Nov 5, 2007
7. LCA Research in Computer Architecture, Performance Evaluation and Workload Characterization, Aug 28, 2007, Computer Architecture Industry Affiliates
8. Computer System Design and Technology, Camp Texas, Aug 20, 2007

9. CRA-W/CDC Programming Languages Summer School, CS Department, UT Austin, "What Programming Language Researchers should know about Computer Architecture", May 11, 2007
10. CRA-W/CDC Computer Architecture Summer Workshop, How to get started in Computer Architecture Research, Princeton, July 19 2006
11. SPEC Annual Meeting, "Use of Clustering in Benchmark Selection", Sunnyvale, CA, Jan 2005.
12. Hewlett Packard, "Workload Characterization for Computer System Design and Evaluation", June 15, 2004
13. University of Texas MITE Program "Electrical and Computer Engineering", June 7 2004
14. Lizy John, "Panelist at ISPASS Panel", Austin, TX, April 2004.
15. Lizy John, "Workload Characterization: Can it save Computer Architecture and Performance Evaluation", Keynote speech, Workshop on Commercial Workload Characterization, Madrid, Spain, Feb 15, 2004.
16. The University of Texas at Austin, ECE Department Graduate Student Orientation, "Life in Graduate School", Aug 2003
17. The University of Texas at Austin, College of Engineering Honors Program, "Workload Characterization for Computer System Design", Sept 14, 2002
18. The University of Texas at Austin, ECE Department Graduate Student Orientation, "Areas in Computer Engineering", Aug 2001
19. The University of Texas at Austin, Women in Engineering Program, "Designing with Field Programmable Gate Arrays", July 26, 2001
20. The University of Texas at Austin Honors Colloquium, "Design of Microprocessors", July 27, 2001.
21. The International Conference on Supercomputing (ICS) 2001, "Improving Java Performance using Hardware Translation", Italy, June 2001.
22. Fourth Workshop on Computer Architecture Evaluation using Commercial Workloads, "Evaluation of TPC-H benchmark on Athlon based systems", Monterrey, Mexico, Jan 21st, 2001.
23. Fourth Workshop on Computer Architecture Evaluation using Commercial Workloads, "Performance Impact of Multithreaded Java Server Applications", Monterrey, Mexico, Jan 21st, 2001.
24. The 5th Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT-5), "Is Compiling for Performance == Compiling for Power?" Monterrey, Mexico, Jan 20, 2001.
25. IEEE Workshop on Hardware Support for Objects and Microarchitectures for Java, Invited Talk, "Understanding, Exploiting and Improving Java Run Time Systems", Sept 17, 2000.
26. Tivoli Corporation, Austin, "Characterizing, Understanding and Exploiting E-business workloads", Aug 21, 2000.
27. The University of Texas at Austin Honors Colloquium, "Design of Microprocessors", July 22, 2000.
28. IBM Center for Advanced Studies (CAS) Conference, IBM Austin, "Effectiveness of Out of Order Scheduling on Three Generations of IBM PowerPC Processors", July 19, 2000.
29. Singapore National University, "Architectural Support for Java Run Time Systems", Seminar in the Computer Science Department and Parallel Processing Laboratory, June 14, 2000
30. Nanyang Technological University, Singapore, "Architectural Support for Java Run Time Systems", Seminar in the Electrical Engineering Department, June 13, 2000.
31. Intel, Austin, "Architectural Support for Java Run Time Systems", Seminar at the Intel Texas Design Center, May 10, 2000.
32. University of Illinois, Urbana Champaign, "Understanding, Exploiting and Improving Java Run Time Systems", Electrical and Computer Engineering Seminar, May 1, 2000.
33. The Pennsylvania State University, Computer Science and Engineering Department Colloquium, "Understanding, Exploiting and Improving Java Run Time Systems", March 16, 2000.

34. Carnegie Mellon University, ECE Seminar, "Architectural Support for Java Run Time Systems", March 15, 2000.
35. University of Paris Sud, France, Computer Science Seminar, "Architectural Support for Java Run Time Systems", Jan 13, 2000.
36. High Performance Computer Architecture (HPCA) 2000, "Architectural Support for Java Run Time Systems", Toulouse France, Jan 12, 2000.
37. Presentation before Technical Committee on Computer Architecture "HPCA 2002- Why Austin", Toulouse, France, Jan 10, 2000.
38. The University of Texas Honors Colloquium, July 1999, "Design of Microprocessors"
39. IEEE International Conference on Computer Design, "Code Coalescing Unit: A Mechanism to facilitate Load Store Data Communication", Oct 1998.
40. College of Engineering UT Austin, EFAC Council Spouse meeting, Presentation title "Research in High Performance Computer Architecture at the Laboratory for Computer Architecture", Fall 1998 EFAC.
41. Workshop on Performance Analysis and its Impact on Design (held in conjunction with ISCA 98), "Characterization of MMX-Enhanced DSP and Multimedia Applications on a General Purpose Processor", June 1998.
42. Workshop on Computer Architecture Education (held in conjunction with ISCA 98), "The Undergraduate Curriculum in the Electrical and Computer Engineering Department at the University of Texas at Austin", June 1998.
43. Hawaii International Conference on System Sciences, "A Scalable Optoelectronic Interconnection Network for Parallel Computing", Jan 1998.
44. IEEE International Conference on Computer Design, "Design and Performance Evaluation of a Cache Assist to implement Selective Caching", Oct 1997.
45. IBM Austin Innovation Series presentation, Half-day seminar "Improving Memory Access Performance of Programs", Aug 1997.
46. Presentation at the Workshop on Integrating Design and Design Automation into the Undergraduate Computer Science Curriculum, Tampa, FL, Aug 1997.
47. Half-day Tutorial on Rapid Prototyping using FPGAs, presented at Microelectronics Systems Education (MSE) 1997, Crystal City, VA, July 1997.
48. Research in Computer Architecture in the ECE Department, Presentation before the ECE Visiting Committee, May 1997.
49. 1996 IEEE VLSI Workshop, "A Decoupled Architecture with a CISC-style Access Processor and a RISC-style Execute Processor", Clearwater, FL, Nov 1996.
50. IEEE Symposium on Parallel and Distributed Processing, "Improving the Parallelism and Concurrency in Decoupled Access/Execute Architectures", New Orleans, LA, Oct 1996.
51. Presentation at the Workshop on Integrating Design and Design Automation into the Undergraduate Computer Science Curriculum, Tampa, FL, Aug 1996.
52. North Carolina State University, Electrical Engineering Department, "Improving Memory Access Performance of Programs", June 1996.
53. University of Texas at Austin, Electrical and Computer Engineering Department, "Improving Memory Access Performance of Programs", May 1996.
54. Ohio State University, Electrical Engineering Department, "Improving Memory Access Performance of Programs", May 1996.
55. Characterization of Media Workloads: The University of Texas at Austin Digital Signal Processing Seminar, April 12, 1996.
56. University of Maryland, College Park, Electrical Engineering Department, "Improving Memory Access Performance of Programs", April 1996.

57. University of North Carolina Chapel Hill, Computer Science Department, "Improving Memory Access Performance of Programs", Apr 1996.
58. The Pennsylvania State University, Computer Science and Engineering Department Colloquium, "Improving Memory Access Performance of Programs", March 1996.
59. University of Connecticut, Electrical Engineering Department, "Improving Memory Access Performance of Programs", March 1996.
60. Tufts University, Electrical Engineering Department, "Improving Memory Access Performance of Programs", March 1996.
61. Ohio University, Electrical Engineering Department, "Issues in the Design of a Decoupled Architecture for the RISC Environment", Jan 1996.
62. Catholic University, Washington D. C., Electrical Engineering Department, "Issues in the Design of a Decoupled Architecture for the RISC Environment", Jan 1996.
63. University of North Texas, June 1996, "Improving Memory Access Performance of Programs"
64. Johns Hopkins University, Electrical Engineering Department, "Issues in the Design of a Decoupled Architecture for the RISC Environment", Jan 1996.
65. Arizona State University, Electrical Engineering and Technology, "Issues in the Design of a Decoupled Architecture for the RISC Environment", 1995.
66. Kansas State University, Electrical Engineering Department, "Issues in the Design of a Decoupled Architecture for the RISC Environment", 1995.
67. University of Delaware, Electrical Engineering Department, "Issues in the Design of a Decoupled Architecture for the RISC Environment", Jan 1995.
68. International Conference on VLSI Design (IEEE) "Design of a Highly Reconfigurable Interconnect for Array Processors", Jan 1995.
69. The International Symposium on High Performance Computer Architecture (HPCA-1), "Program Balance and its Impact on High Performance Architectures", Jan 1995.
70. IEEE International Conference on Parallel Processing, "Module Partitioning and Interlaced Data Placement Schemes to Reduce Conflicts in Interleaved Memories", Aug 1994.
71. University of Kentucky, Electrical Engineering Department, "Issues in the Design of a Decoupled Architecture for the RISC Environment", Summer 1994.
72. IEEE Tampa Chapter, "Rapid Prototyping Using Field Programmable Gate Arrays", Jan 1994.
73. University of South Florida, ACM Chapter, December 1993, "Research in Computer Architecture"
74. University of South Florida, Computer Science and Engineering Department, "Issues in the Design of a Decoupled Architecture for the RISC Environment", Jan 1993.
75. IBM Vermont, "Issues in the Design of a Decoupled Architecture for the RISC Environment", Dec 1992.
76. ACM/IEEE International Symposium on Computer Architecture (ISCA 92), "Memory Latency Effects in Decoupled Architectures", Goldcoast Australia, May 1992.

**PATENTS:**

1. U S Patent #5,867,422 " Computer Memory Chip with field Programmable Memory Cell Arrays", Granted Feb 1999. Patent has been licensed for a multimillion dollar license with a major chip company.
2. U S Patent 7, 107, 434, " System, Method and Apparatus for Allocating Hardware Resources using Pseudo Random Sequences". Patent has been licensed by UT
3. U S Patent 7,370,183,"Branch Predictor comprising a split branch history shift register". Patent has been licensed by UT.

4. Patent Application filed in Korea and being filed in US, Japan and China - FE-200703-016-1-US0 - Method and Apparatus to save Java bytecode translations as blocks rather than per bytecode in an external (off processor) Java accelerator hardware
5. Patent Application filed in Korea and being filed in US, Japan and China - FE-200703-017-1-US0 - Method and Apparatus to Perform Embedding of Constants into Native Instructions
6. Provisional U S Patent Application, Workload-Guided Application Scheduling in Multi-core Systems, Application No. 61096075, September 2008
7. Provisional U. S Patent Application, Automatically Generating Microprocessor Benchmarks to Generate Maximum Power Consumption and Operating Temperature, August 2008, Application No. 61088252

**GRANTS AND CONTRACTS:** (Co-principal investigators (if any), title of grant, sponsoring agency, total dollar value, beginning and ending dates)

Co-Investigators	Title	Agency	Grant Total	Grant Period
None	Performance Cloning for Dissemination of Proprietary Applications to Hardware Vendors	Lockheed Martin	100,000	2008-2009
None	Benchmark Synthesis for Performance and Power Modeling	Sun Microsystems	45,000	2008-2009
None	IBM Faculty Award	IBM	15,000	2008-2009
R. Figueiredo, etc	Collaborative Research Archer: Seeding a Community Based computing Infrastructure for Computer Architecture Research and Education	NSF	(my share 67,631)	2008-
None	Computer Architecture Research	AMD	8,000	Dec 07- Dec 08
None Tao Li	Intel Equipment Grant for research Automatic Benchmark Synthesis for Validation of Performance and Power Models of High Performance Processors	Intel SRC	35,056 330,000 (my share: 165,000)	Sep 2008-04/08-03/11
None	Simplifying Performance Evaluation using Workload Characterization	NSF	300,000	09/07-08/10
None	Faculty Partnership Award	IBM	\$25,000	06/07
None	Computer Architecture Research	AMD	\$5000	11/06
None	CAS Award – Faculty Partnership Award	IBM	\$7,500	06/06
None	Computer Architecture Research	AMD	\$5000	11/05
None	Java Accelerators	Samsung	\$128,000	2/05-8/06
None	CAS Award	IBM	\$25,000	6/05
None	Statistical Techniques for Computer Performance Evaluation	NSF	\$200,000	2004-2008
None	Computer Architecture Research	AMD	\$5000	2/05
None	Performance Evaluation Research	IBM	\$500	12/04
None	CAS project- Statistical Techniques in Performance Evaluation and Benchmarking	IBM	\$25,000	7/04
None	Computer Architecture Research	Hewlett Packard	\$800	6/04
None	Equipment Grant	Intel	\$42,000 (approx.)	Spring 2004
None	Performance Impact of Emerging Workloads on Intel Processors	Intel	\$35,000	March 2004

None	Research in Computer Architecture and Workload Characterization	AMD	\$3,000	Dec 2003
None	IBM Faculty Partnership Award Project: Developing a Methodology for Predicting Characteristics of Future/Emerging Workloads	IBM	\$25,000	June 2003
None	Performance Impact of Emerging Workloads on Intel Processors	Intel	\$35,000	May 2003
	IBM SUR grant	IBM	\$60,000 (approx.)	Fall 2002
None	IBM Faculty Partnership Award- Developing a Methodology for Predicting Characteristics of Future/Emerging Workloads	IBM	\$25,000	June 2002
None	Equipment Support- Performance Impact of Emerging Workloads on Intel Processors	Intel	\$10,000	Summer 2002
None	Research in Computer Architecture and Workload Characterization	AMD	\$5,000	May 2002
None	Performance Impact of Emerging Workloads on Intel Processors	Intel	\$35,000	March 2002
None	Intel Equipment (8-way server + 5 workstations)	Intel	\$65,000 (approx.)	Spring 2002
None	Development and Characterization of Control-Plane Network Workloads	Motorola	\$50,000	Jan 2002
None	Computer Architecture Research	AMD	\$5,000	Dec 2001
	IBM SUR Grant	IBM	\$100,00 (approx.)	Fall 2001
None	Designing Microprocessors and Computer Systems for Emerging Workloads	NSF	\$265,000	2001-2004
	Intel Equipment (10 workstations)	Intel	\$40,000 (approx.)	2000-2001
None	IBM Faculty Partnership Award- Effectiveness of Out of Order Microarchitectural techniques for web server workloads	IBM	\$30,000	May 2001
None	UT Research Internship Program	Univ. of TX, at Austin	\$15,500	2001-2002
None	Computer Architecture Seminar Series	AMD	\$15,000	
None	Understanding and Optimizing e-Business workloads and the underlying infrastructure	Tivoli	\$30,000	Aug 2000
None	IBM Center for Advanced Studies Partnership Award- Effectiveness of Out of Order Microarchitectural Techniques for web server workloads	IBM	\$25,000	March 2000
None	Workshop on Workload Characterization 2000	AMD	\$2,500	2000
None	Career Award- Improving the Access-Execute Balance and Concurrency in High Performance Processors	NSF	\$315,000	1996-2000
None	UT Co-op Book Subvention Grant	Univ. of TX, at Austin	\$2,500	Aug 1999
None	DELL-LARIAT grant- Characterization of Multimedia Application and Analysis of their Performance Impact	Dell	\$32,127	July 1999
None	Workshop on Workload Characterization	Intel	\$4,000	July 1999
None	Computer hardware grant- Characterization of Multimedia Workloads and Analysis of their Performance Impact	Intel	\$4,181	July 1999
None	Software donation- Web Server Characterization Studies on the Pentium Platforms	Microsoft	\$3,814	Jan 1999

None	Web Server Characterization Studies on the Pentium Platforms	Intel	\$15,320	Dec 1998
None	UT research Internship Program	Univ. of TX, at Austin	\$15,000	1998-1999
None	UT Endowed Lecturer Program	Univ. of TX, at Austin	\$1,100	Spring 1998
None	Summer Research Assignment Award	Univ. of TX, at Austin	\$11,000	Summer 1997
None	Junior faculty Enhancement Award	Oak Ridge Associated Universities	\$5,000	1996-1997
None	Matching Award to Oak Ridge Junior Faculty Enhancement Award	UT Austin	\$5,000	Fall 1996
None	Matching Award to NSF CAREER Equipment Startup Grant	UT Austin	\$10,000	Fall 1996
None		Univ. of TX, at Austin	\$55,000	Fall 1996
None	Microprocessor Performance Evaluation System - Advanced Micro Devices (proprietary equipment given for UT research. Dollar equivalent not specified by AMD)	AMD	Not Specified	Dec 1997
S. Keckler, D. Burger, L. Alvisi, M.D. Dahlin, C. Lin, C.R. Moore, K. McKinley, and H. Vin	“TRIPS: The Tera-op Reliable Intelligently adaptive Processing System Implementation for Polymorphous Computing Architectures (PCA),”	Defense Advanced Research Projects Agency	\$7,617,912	2003-2005
Steve Keckler, D. Burger, L. Alvisi, M.D. Dahlin, C. Lin, K. McKinley, and H. Vin	TRIPS: The Tera-op Reliable Intelligently adaptive Processing System	Defense Advanced Research Projects Agency	\$100,000 (approx./my share) \$3,027,48	6/01-5/03
Prof. E. Swartzlander and Prof. E. John	ATP Grant- High Performance MultiMedia Processors Principal Investigator	State of Texas Advanced Technology Program	\$157,800 \$72,806 (my share.)	1/00-12/01
Prof. C. Chase	Impact of Contemporary Programming Paradigms and Workloads Principal Investigator	NSF	\$356,314 \$256,314 (my share)	1998-2001
Prof. E. Swartzlander	ATP Grant- High Performance Digital Signal Processors Principal Investigator	State of Texas Advanced Technology Program	\$134,640 80,784 (my share)	1/98-12/99
Prof. Yale Patt Prof. Yale Patt	Equipment Donation Software Donation	Intel Microsoft	\$136,640 \$61,039	Nov 1999 Sept 1999
Prof. Evans	TMS320C62x Development Tools	Texas Instruments	Not Specified	1998
Prof. J. C. Browne of Computer Science, co-PIs: L. John, Prof. C. Chase and Prof. P. Teller at the University of Texas at El Paso	IBM- SUR Grant- End-to-End Measurement, Modeling and Simulation of Parallel/Distributed Computer Systems	IBM	\$100,000	Oct 1997

Dr. Pete Maurer and Dr. N. Ranganathan of the University of South Florida, Tampa, Florida	NSF CISE Infrastructure Grant * This was an award to Univ. of S. Florida while Lizy John was faculty there. This grant was not transferred to UT, however, I continued to participate in the project until 1998	NSF	\$373,524	1995- 1998
None	FPGA lab hardware and software donation (while faculty at University of Southern Florida)	Xilinx	\$100,00 (approx./ my share) \$40,000 (approx.)	1994- 1995
None	International Faculty Travel grant	University of South Florida	\$1,500	1995
None	Office of Sponsored research	University of South Florida	\$5,500 (approx.)	1994
None	Startup grant	University of South Florida	\$10,000	1993

**PH.D. SUPERVISIONS COMPLETED:** *(Name, \*title, year, major dept, name of institution)*  
*(May want to add another column for titles.)*

Ajay Joshi	Dec 2007	Constructing Adaptable and Scalable Synthetic Benchmarks for Microprocessor Performance Evaluation (ARM Corporation)	ECE	UT
Aashish Phansalkar	May 2006	Similarity Analysis and Benchmark Subsetting (Employed at Marvel)	ECE	UT
Rob Bell Jr.	Dec 2005	Automatic Workload Synthesis for Early Design Studies and Performance Model Validation (Employed at IBM)	ECE	UT
Byeong Kil Lee	Aug 2005	Network Processor Design: Benchmarks and Architectural Alternatives (Employed at Texas Instruments)	ECE	UT
Shiwen Hu	Dec 2005	Effective Adaptive Computing Environment Management via Dynamic Optimization, (Employed at Freescale)	ECE	UT
Yue Luo	Aug 2005	Improving Sampled Microprocessor Simulation (Microsoft)	ECE	UT
Madhavi Valluri	May 2005	A Hybrid-Scheduling Approach for Energy-Efficient Superscalar Processors (Employed at IBM)	ECE	UT
Juan Rubio	Aug 2004	Exploring the Potential of a Hierarchical Computing Model for a Commercial Server (Employed at IBM Austin Research Lab)	ECE	UT
Tao Li	Aug 2004	OS-aware Architecture for Improving Microprocessor Performance and Energy Efficiency, (Assistant Professor University of Florida)	ECE	UT
Ravi Bhargava	Aug 2003	Instruction History Management for High-Performance Microprocessors (Employed at AMD)	ECE	UT
Deepu Talla	Aug 2001	Architectural Techniques to Accelerate Multimedia Applications on General-Purpose Processors, August 2001 (Employed at Texas Instruments)	ECE	UT
Ramesh Radhakrishnan	Aug 2000	Microarchitectural Techniques to Enable Efficient Java Execution (Employed at Dell)	ECE	UT

**M.S. SUPERVISIONS COMPLETED:** *(Name, year, major department, name of institution)*  
*(May want to add another column for titles.)*

Rajiv Bhatia	Aug 2008	Electrical and Computer Engineering	Univ. of Texas at Austin
Justin Friesenhahn	Dec 2007	Electrical and Computer Engineering	Univ. of Texas at Austin
Jason Matalka	Aug 2006	Electrical and Computer Engineering	Univ. of Texas at Austin

Kathryn Stacer	May 2006	Electrical and Computer Engineering	Univ. of Texas at Austin
Lloyd Bircher	May 2006	Electrical and Computer Engineering	Univ. of Texas at Austin
Diego Vila	May 2006	Electrical and Computer Engineering	Univ. of Texas at Austin
Brijesh Patel	2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Jenson Lam	2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Brian Gaide	2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Jignesh Gondalia	2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Saket Kumar	May 2004	Electrical and Computer Engineering	Univ. of Texas at Austin
Michael Arunkumar	Dec 2003	Electrical and Computer Engineering	Univ. of Texas at Austin
Michael Lance Karm	Dec 2003	Electrical and Computer Engineering	Univ. of Texas at Austin
Patrick James Peters	Dec 2003	Electrical and Computer Engineering	Univ. of Texas at Austin
Mike Clark	May 2003	Electrical and Computer Engineering	Univ. of Texas at Austin
Anand Sunder Rajan	2003	Electrical and Computer Engineering	Univ. of Texas at Austin
James Yang	2002	Electrical and Computer Engineering	Univ. of Texas at Austin
Ravi Bhargava	Aug 2000	Electrical and Computer Engineering	Univ. of Texas at Austin
Vikram Godbole	May 2000	Electrical and Computer Engineering	Univ. of Texas at Austin
Sanjeev Ghai	May 2000	Electrical and Computer Engineering	Univ. of Texas at Austin
Srikanth Kannan	May 2000	Electrical and Computer Engineering	Univ. of Texas at Austin
Jyotsna Sabarinathan	Dec 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Jody Joyner	Dec 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Juan Rubio	May 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Poorva Murarka	May 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Purnima Vasudevan	May 1999	Electrical and Computer Engineering	Univ. of Texas at Austin
Roy Shalem	Aug 1998	Electrical and Computer Engineering	Univ. of Texas at Austin
Dachih-Tang	Aug 1998	Electrical and Computer Engineering	Univ. of Texas at Austin
Yin Teh	Dec 1997	Electrical and Computer Engineering	Univ. of Texas at Austin
Ramesh Radhakrishnan	Aug 1997	Computer Science and Engineering	Univ. of South Florida
Vijay Kammila	1996	Computer Science and Engineering	Univ. of South Florida
Vinod Reddy	Dec 1996	Computer Science and Engineering	Univ. of South Florida
Amudha Muthiah	1996	Computer Science and Engineering	Univ. of South Florida
Raghuveer Reddy	1995	Computer Science and Engineering	Univ. of South Florida

**PH.D. IN PROGRESS:** *(List students names by category)*

A. Students admitted to candidacy

1. Lloyd Bircher

B. Post M.S. students preparing to take Ph.D. qualifying exam

1. Ciji Isen
2. Dimitris Kaseridis
3. Jeff Stuecheli
4. Jian Chen
5. Arun Nair
6. Umar Farooq
7. Justin Friesenhahn
8. JungHo Jo

**M.S. IN PROGRESS:** *(List students names)*

1. Karthik Ganesan

**VITA:** *(One-half page paragraph that can be used for general purposes)*

Lizy Kurian John is a professor and Engineering Foundation Centennial Teaching Fellow in the Department of Electrical and Computer Engineering at the University of Texas at Austin. She joined the department in September 1996. She received her Ph. D in Computer Engineering from the Pennsylvania State University in 1993. She was on the faculty of the Computer Science and Engineering department at the University of South Florida from 1993 to 1996. Her research interests include designing computer systems for merging workloads, high performance processor and memory architectures, superscalar and superpipelined processors, cache memories, program behavior studies, computer performance evaluation and benchmarking, compiler optimization for high performance processors, rapid prototyping, Field Programmable Gate Arrays etc. She has coauthored one book, edited 4 books, written 16 book chapters, and published more than 150 journal and conference papers in several prestigious journals and highly selective conferences including the IEEE Transactions on Computers, IEEE Transactions on VLSI, ACM/IEEE International Symposium on Computer Architecture (ISCA), ACM International Conference on Supercomputing (ICS), IEEE Micro Symposium (MICRO), IEEE High Performance Computer Architecture Symposium (HPCA). She holds 3 patents and several applications are in progress. Her research has been supported by the Semiconductor Research Consortium, National Science Foundation, the State of Texas Advanced Technology program, DELL Computer Corporation, IBM, Tivoli, AMD, Motorola, Intel and Microsoft Corporations. She is recipient of a National Science Foundation CAREER award and a Junior Faculty Enhancement Award from Oak Ridge Associated Universities.

She received the TEXAS EXES Teaching Award in Feb 2004, the Engineering Foundation Faculty Award, College of Engineering, in Fall 2001, and the Halliburton, Brown and the Root Engineering Foundation Young Faculty Award in Fall 1999. She is a Fellow of IEEE. She is a member of ACM and ACM SIGARCH. She is also a member of Eta Kappa Nu, Tau Beta Pi and Phi Kappa Phi.