

Project Design Review Schedule

Week # 1: Thursday April 17th

<u>Unit</u>	<u>Duration</u>	<u>Time</u>
CACHE Memories	30 min.	6:30 – 7:00
TLB	30 min	7:00 – 7:30
MMU	30 min	7:30 – 8:00
BREAK	10 min	
REGISTER FILES	30 min.	8:10 – 8:40
LIBRARY	20 min.	8:40 – 9:00

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Week # 2: Thursday April 24th

<u>Unit</u>	<u>Duration</u>	<u>Time</u>
FFU	20 min.	6:30 – 6:50
SPU	20 min	6:50 – 7:10
TLU	30 min	7:10 – 7:40
EXU	30 min	7:40 – 8:10
BREAK	10 min	
LSU	30 min.	8:10 – 8:40
IFU	30 min.	8:40 – 9:10

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Week # 3: Thursday May 1st

<u>Unit</u>	<u>Duration</u>	<u>Time</u>
Full Chip Clocks & Reset	30 min.	6:30 – 7:00
Global Power & Power Grid	30 min.	7:00 – 7:30
Global Timing	30 min.	7:30 – 8:00
BREAK	10 min	
Full Chip Integration	45 min.	8:10 – 8:55
Class evaluation		8:55 – 9:15

Project Design Review

- **The design review is your opportunity to convince the instructors that you know what you are doing on this project.**
- **The review should:**
 - NOT be done using elaborate PowerPoint foils. You need to focus on content not fancy colors.
 - NOT be verbose. Keep it short and sweet and to the point. Provide backup material if needed.
- **The grading will be a combination of peer and instructor review.**
- **The review should cover:**
 - Description, block diagram, timing diagrams at the block, cluster or chip level of your part of the design. Provide enough detail to indicate a comprehensive understanding of your portion of the chip.
 - What assumptions, assertions, optimizations did you make in order to complete the design? Be able to defend them based on supporting documentation.
 - What issues, problems, etc. exist with that part of the chip. How were the issues addressed? How did your particular portion of the design affect the other sections of the chip?
 - What are the risks associated with your portion of the design? What risk mitigation plans would you put in place?
 - **What would you do different if you took the class over again.**