Fall 2006 | **VLSI Design** **FINAL EXAM.** | **J. Abraham** **December 13, 2006**

Name: Exam, No. 3

- Open Book, Open Notes.
- Time Limit: 3 hours (pace yourself).
- Check for 8 pages in exam.
- Write all your answers in the spaces/boxes provided.
- Show any calculations in these pages using the back of the pages if needed.
- State clearly any assumptions made.

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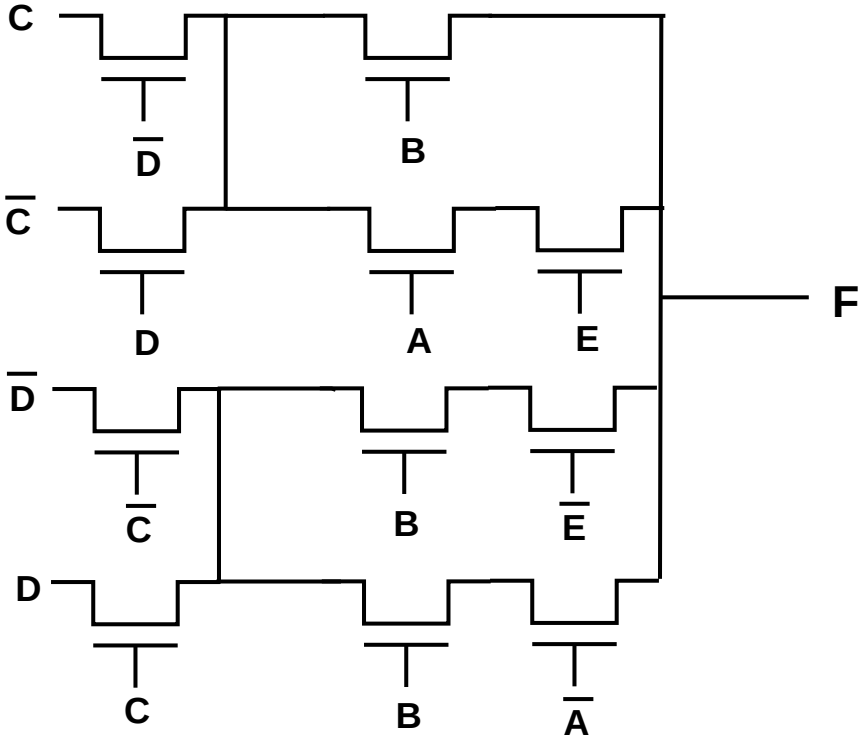
1. (10 points)

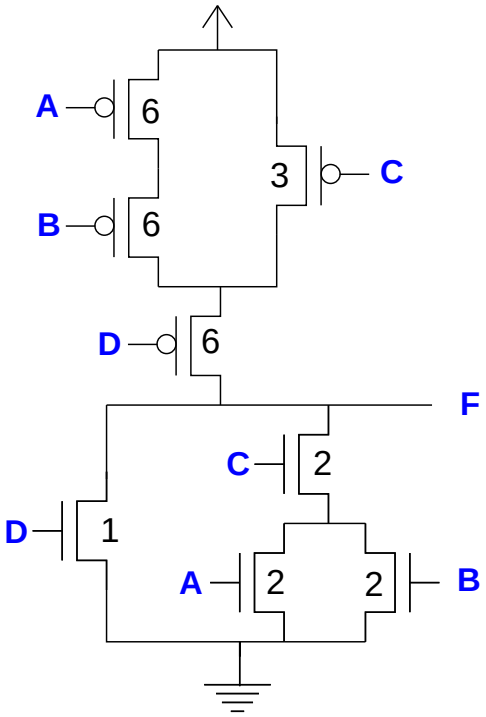
Write down the logic function implemented by the circuit below; use parantheses in the expression to reduce the number of literals.



F =

2. (10 points)

Find the largest as well as contimination delays for both 0-1 and 1-0 transitions for the circuit below. The widths of the transistors are given. Assume that a minimum width transistor will have an on-resistance of **R** and a gate capacitance of **C**; the source and drain capacitances are also C, and there is **no** sharing of diffusions. Give the input combinations which produce the respective delays (assuming that the internal nodes are charged or discharged as appropriate).



Input (ABCD) producing the largest rise delay:

Largest rise delay =

Input (ABCD) producing the largest fall delay:

Largest fall delay =

Input (ABCD) producing the smallest rise delay:

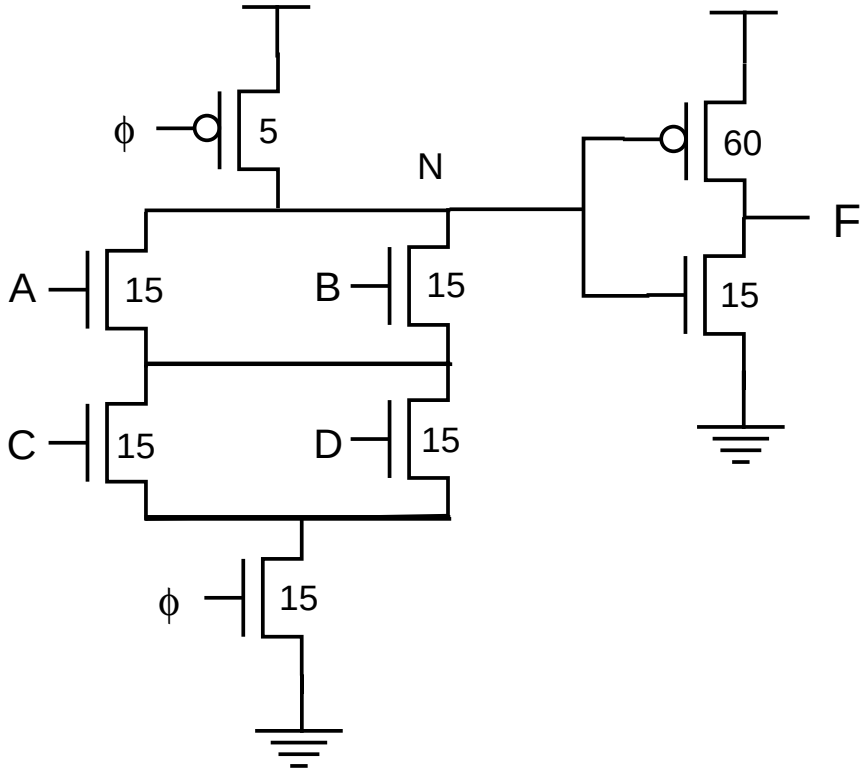
Contamination rise delay =

Input (ABCD) producing the smallest fall delay:

Contamination fall delay =

3. (10 points)

The domino circuit has the widths of the transistors shown next to them. Assume that a minimum width transistor has a gate capacitance of C, with the source and drain capacitances also each equal to C. Assume no sharing of diffusion.



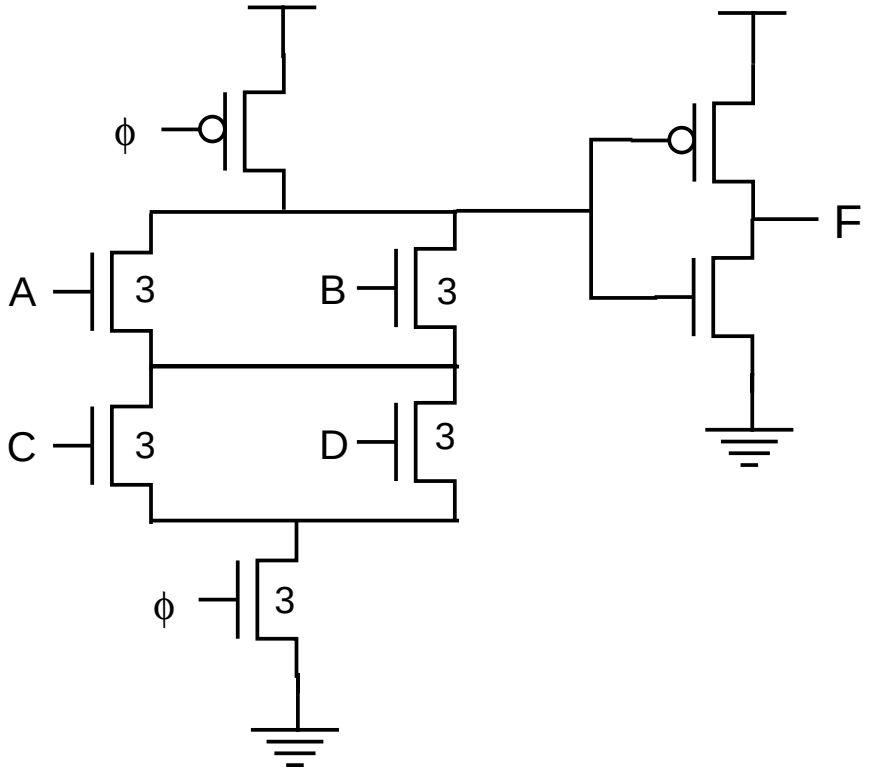
(a) Under the worst-case input sequence, what is the largest voltage drop on the dynamic node, N?

(b) Give a sequence of inputs (ABCD) which will cause the voltage drop on N.

(c) How should the static inverter be sized to cause a voltage drop (noise) of at most 20% on the node N?

4. (15 points)

The best stage effort for a domino circuit has been found to be between 2.0 and 2.76 (for unfooted and footed blocks). The circuit below has the transistor widths labeled for the dynamic portion. The static inverter is a standard Hi-Skew with a logical effort of 5/6.



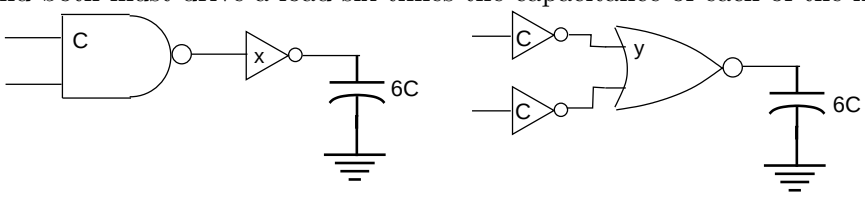
(a) If the stage effort is 2.5, what would be the corresponding path electrical effort, H (using the standard logical effort formulation)?

(b) What would be the delay of the circuit for the design in (a)?

(c) What would be the sizes of the P and N transistors in the static inverter (for the same design)?

5. (15 points)

Consider the two different implementations of an AND gate below. Both have an input capacitance of C and both must drive a load six times the capacitance of each of the inputs.



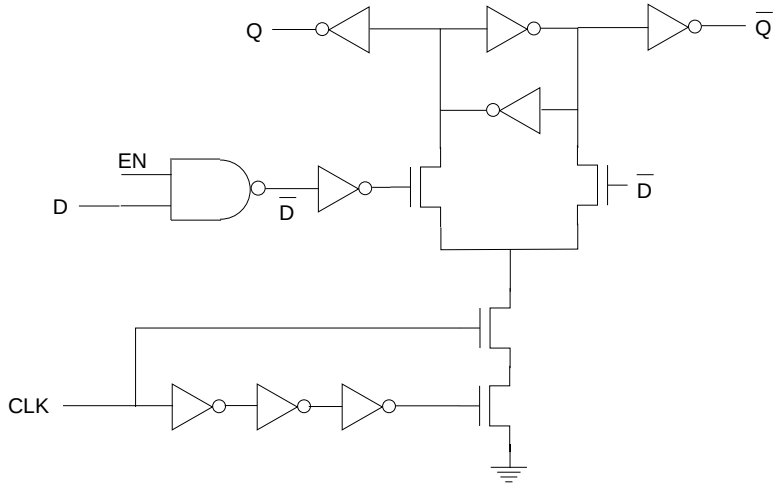
(a) What is the path effort of each design?

(b) Which design will be the fastest? Explain.

(c) Compute the sizes of the logic gates, x and y to achieve the least delay.

6. (15 points)

The inverters in the flip-flop below have rise and fall delays of 50 pS. The NAND gate has a rise delay of 100 pS and a fall delay of 150 pS.



Neglecting the delay of the nMOS transistors, what are the parameters of the flip-flop?

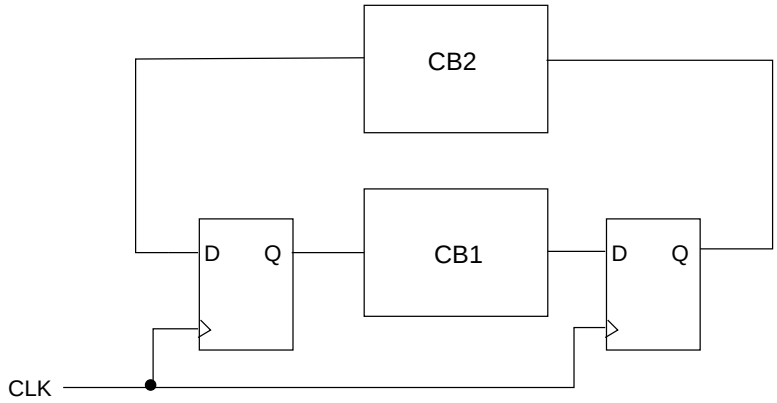
(a) Setup time

(b) Hold time

(c) CLK-Q delay

7. (15 points)

The sequential circuit below has two flops and two combinational blocks, CB1 and CB2. The design is made using a library which includes inverters with a 25 pS rise and fall delay.



The parameters of the flops are: $t_{pcq} = 100pS, \quad t_{ccq} = 20pS, \quad t_{setup} = 50pS, \quad t_{hold} = 100ps$

The parameters of the combinational block are as follows.
CB1: $t_{pd} = 250pS, t_{cd} = 100pS$
CB2: $t_{pd} = 350pS, t_{cd} = 50pS$

(a) Will the circuit work correctly? Explain and, if not, suggest a fix which will not affect the maximum frequency at which the circuit can be operated.

(b) If the circuit can be operated correctly, what is the maximum frequency at which it will work correctly?

(c) Suggest a modification to the clock circuitry to increase the frequency found in (b). Explain.

8. (10 points)

An embedded hardware accelerator in a system-on-chip is designed in a 1 V, 90 nm process, and has 1 million logic transistors with an average width of 12λ. The gate capacitance, $C_g = 2fF/\mu m$. The gates have an activity factor of 0.2.

(a) What is the maximum clock frequency if the dynamic power should not exceed 20 mW?

(b) If the subthreshold leakage is $20nA/\mu m$ and the gate leakage is $2nA/\mu m$, and if half the transistors are off (on average), what is the leakage power?

VLSI Design — **J. Abraham**

Fall 2006 — **EXAM. II** — **November 20, 2006**

Name: Exam, No. 2

- **Open Book, Open Notes.**
- **Time Limit: 75 minutes (pace yourself).**
- **Check for 6 pages in exam.**
- **Write all your answers in the spaces/boxes provided.**
- **Show any calculations in these pages using the back of the pages if needed.**
- **State clearly any assumptions made.**

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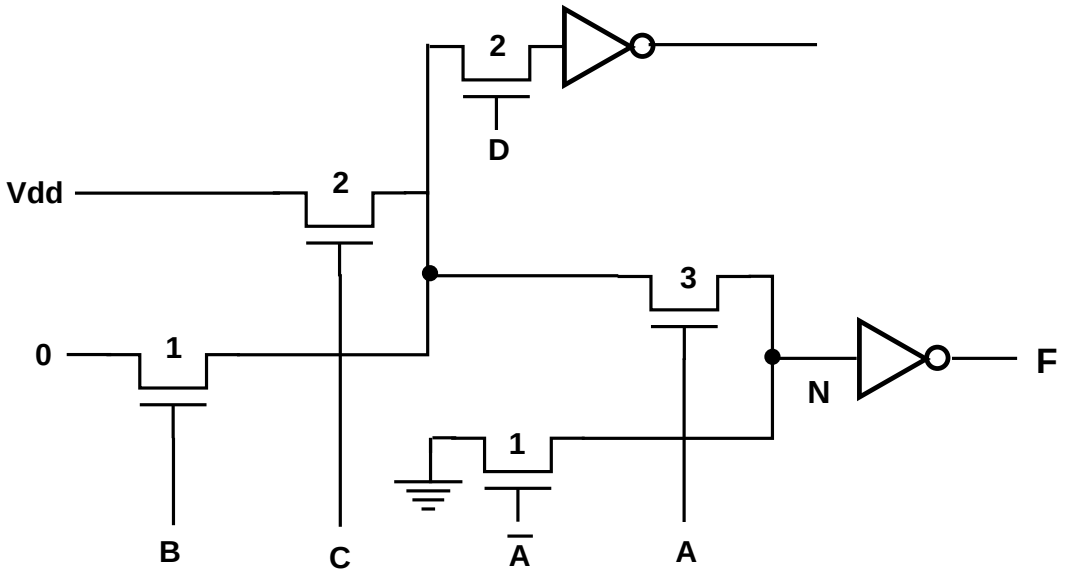
1. (20 points)

The inverters in the circuit below have minimum-sized transistors and the widths of the pass transistors are shown in the figure. Assume that the diffusion capacitance of a transistor is equal to its gate capacitance, and that a minimum sized transistor has gate and diffusion capacitance equal to C. In addition, $V_{dd} = 2V$, $V_{tn} = 0.3V$ and $|V_{tp}| = 0.4V$.

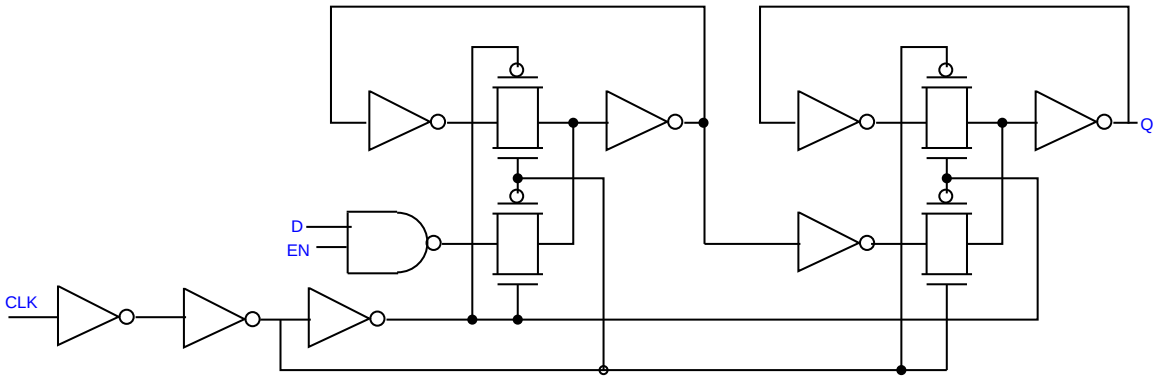


The sequence ABCD = (0011, 1001) is given as input to the circuit. Write down the voltage on node N just after the sequence is applied.

Voltage on Node N = ____

2. (20 points)

The components of the flip-flop below have the following rise/fall delays (in picoseconds).
Nand gate: 75/125
Transmission gate: 75/75
Inverter: 50/50



What are the values of the following flip-flop parameters (which a designer needs to use to calculate the performance of a system)?

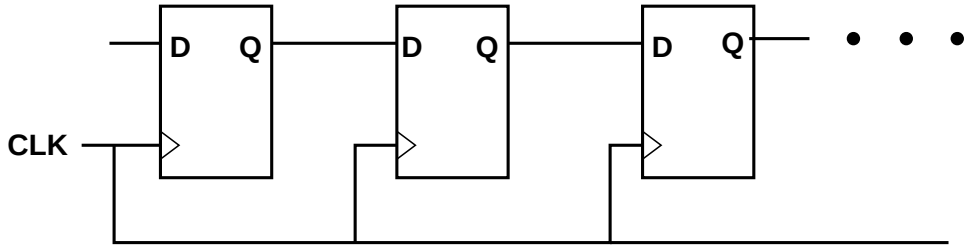
(a) Setup time = ____ **ps**

(b) Hold time = ____ **ps**

(c) Clock-to-Q delay = ____ **ps**

4. (20 points)

The flops used in the shift register below have a setup time of 100 ps, a maximum clock-Q delay of 150 ps, and a minimum clock-Q delay of 100 ps.



(a) How fast can this circuit be clocked?

Clock frequency = ☐ **MHz**

(b) What is the limit on the hold time of the flops at this frequency?

Hold time < ☐ **ps**

(c) What is the limit on the hold time of the flops at a frequency of 1 GHz?

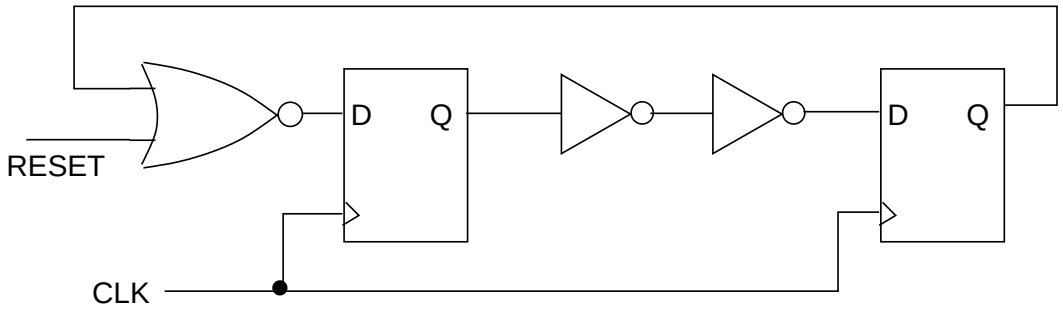
Hold time < ☐ **ps**

(d) What is the limit on the hold time of the flops if the circuit is clocked at a frequency of 100 MHz?

Hold time < ☐ **ps**

3. (20 points)

(a) What is the highest frequency at which the following circuit can be operated correctly? The parameters of the components are as follows.
Inverter: $t_{pd} = 200ps$**,** $t_{cd} = 100ps$
2-input NOR: $t_{pd} = 200ps$**,** $t_{cd} = 150ps$
D-flop: $t_{pd} = 200ps$ $t_{cd} = 0ps$**, Setup time = 300 ps, Hold time = 100 ps.**



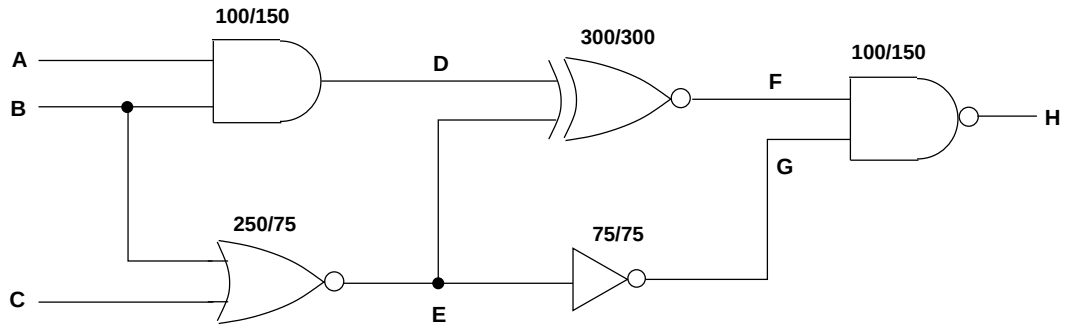
Maximum Clock frequency = ☐ **MHz**

(b) If the two inverters are removed (the Q of the first flop is connected to the D of the second), what will be the highest frequency at which the circuit can be operated. Explain your answer.

Maximum Clock frequency = ☐ **MHz**

5. (20 points)

(a) Write down all the paths from input B to the output and the worst-case and lowest delays for each path in the circuit below. The rise and fall times (in picoseconds) for each gate are shown over the gate symbol as risetime/falltime.



For example, the paths from input A to the output, and the delays are:

Path	Worst-case delay	Lowest delay
ADFH	600 ps	500 ps

(b) Give the test sequences for the following cases:

(i) Rising input on B, path BDFH

(i) Falling input on B, path BEFH

(ii) Rising input on B, path BEFH

VLSI Design — **J. Abraham**

Fall 2006 — **EXAM. II** — **November 20, 2006**

Name: Exam, No. 2

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1. (20 points)

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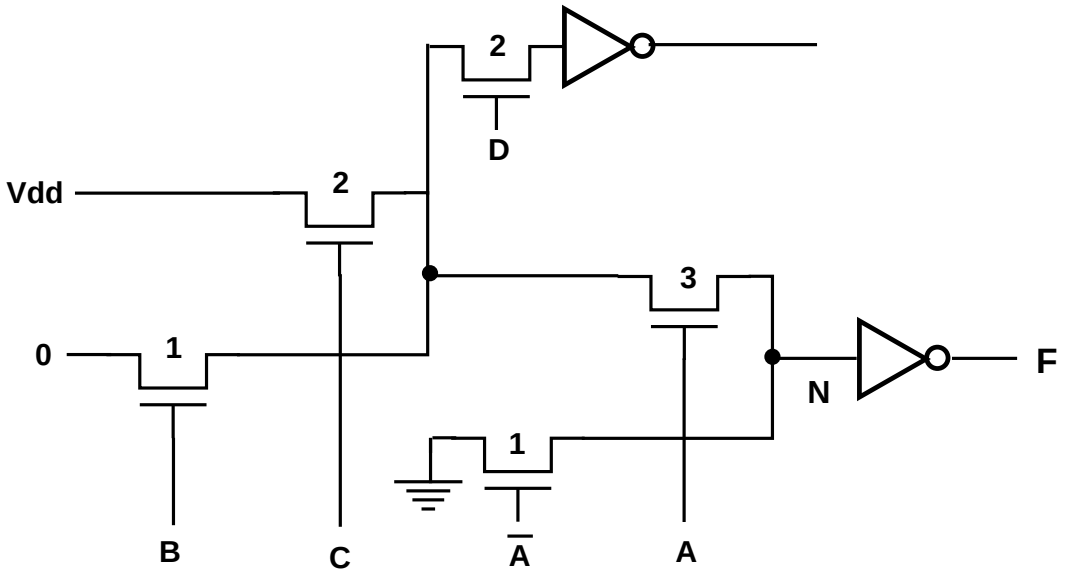

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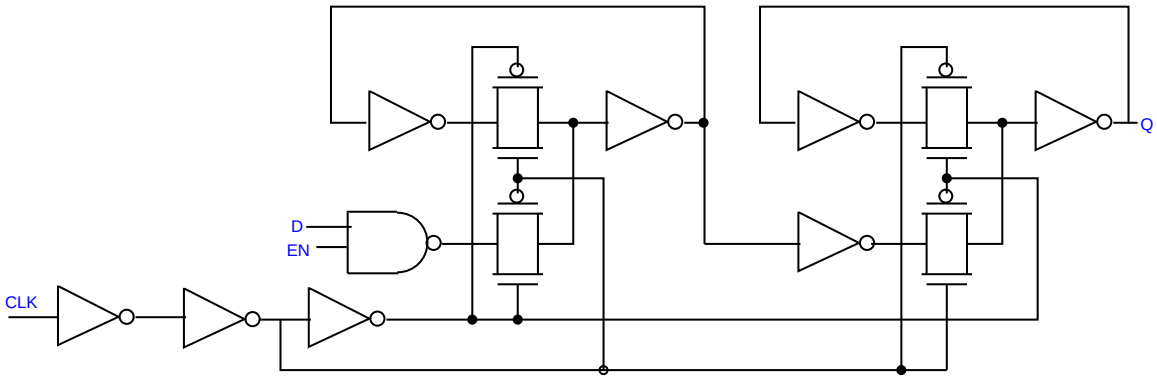

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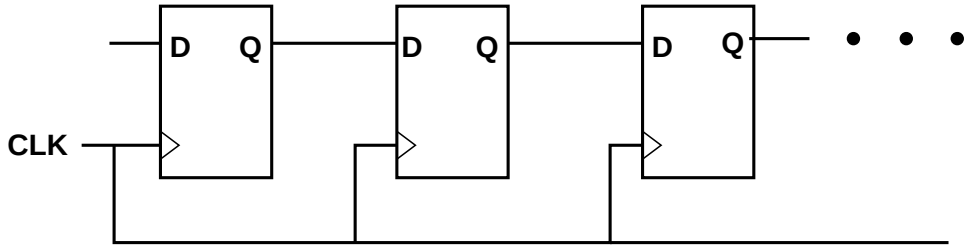

(a) How fast can this circuit be clocked?

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(b) What is the limit on the hold time of the flops at this frequency?

Hold time < ☐ **ps**

(c) What is the limit on the hold time of the flops at a frequency of 1 GHz?

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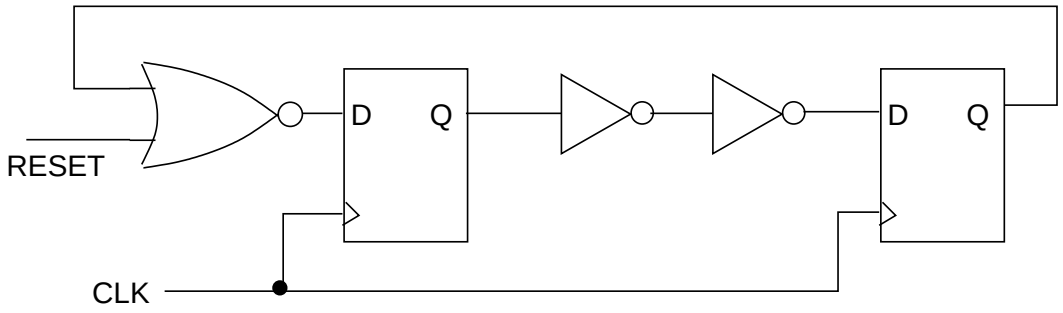

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(b) If the two inverters are removed (the Q of the first flop is connected to the D of the second), what will be the highest frequency at which the circuit can be operated. Explain your answer.

Maximum Clock frequency = ☐ **MHz**

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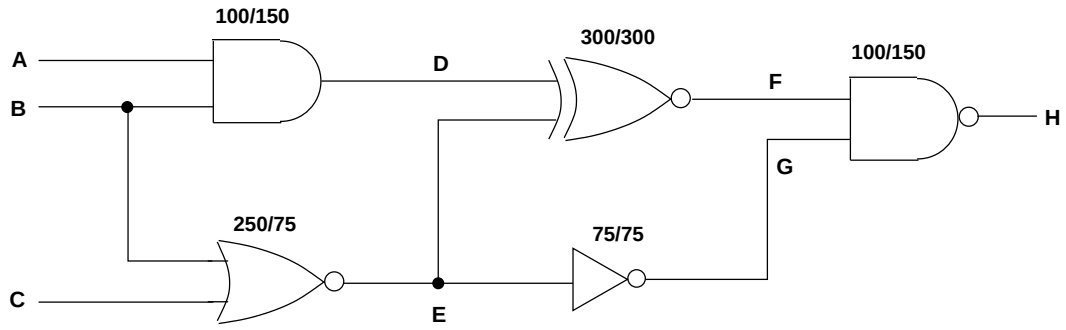

For example, the paths from input A to the output, and the delays are:

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(ii) Rising input on B, path BEFH

Spring 2006 | VLSI Design EXAM. I | J. Abraham March 1, 2006

Name: Student, A

Open Book, Open Notes. Time Limit: 75 minutes (pace yourself). Check for 5 pages in exam.

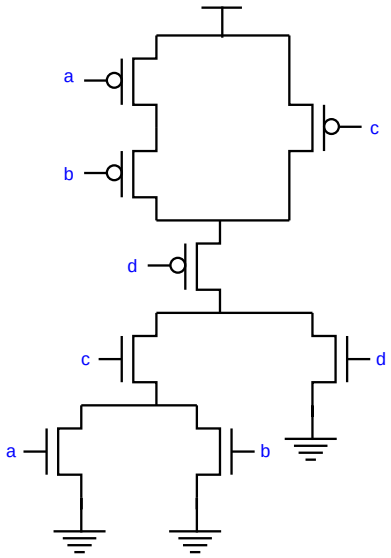
Write all your answers in the spaces/boxes provided.

Show any calculations in these pages using the back of the pages if needed. State clearly any assumptions made.

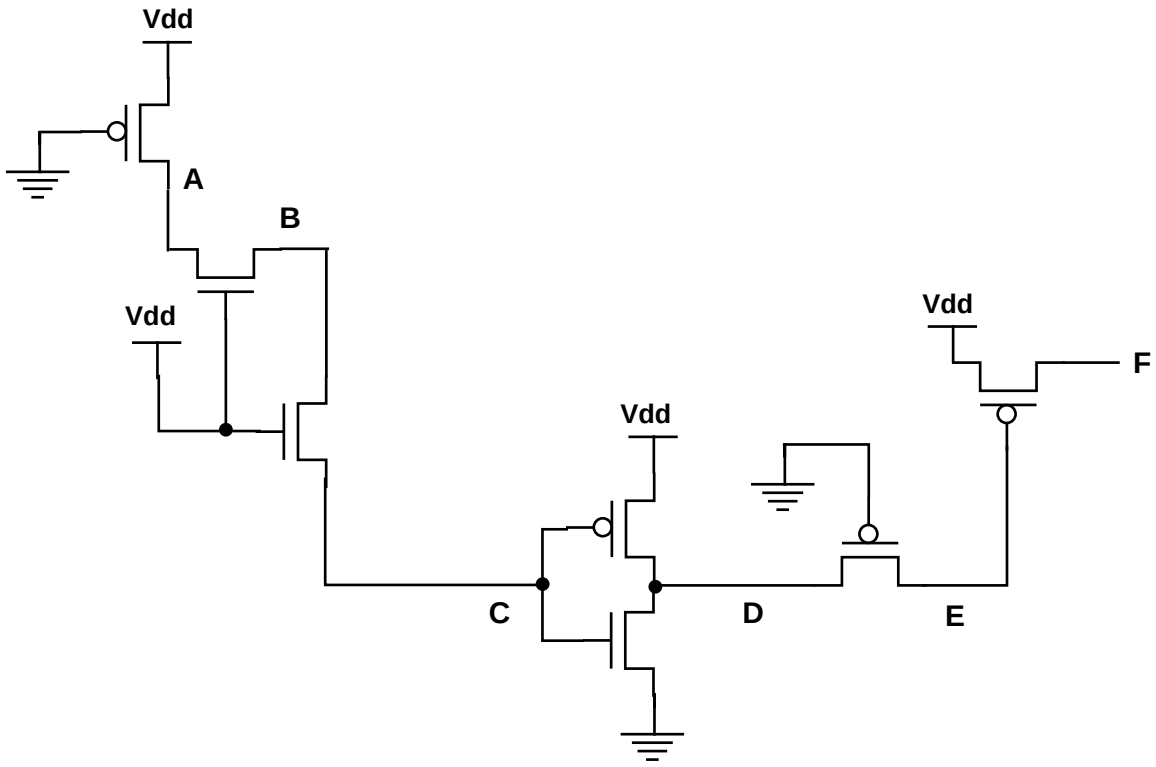
PROBLEM	MAX	POINTS
1	15	
2	20	
3	20	
4	25	
5	20	
TOTAL	100	

1. (15 points)

Size the transistors in the circuit below so that it has the same drive strength, in the worst case, as an inverter that has PW = 3 and NW = 2. Use the smallest widths possible to achieve this ratio. Write down the size next to each transistor.



2. (20 points) Find the voltages at each of the nodes, A, B, C, D, E and F below. Use the following circuit parameters:
$V_{dd} = 5V$, $V_{tn} = 0.5V$, $|V_{tp}| = 1.5V$.



A = ____

B = ____

C = ____

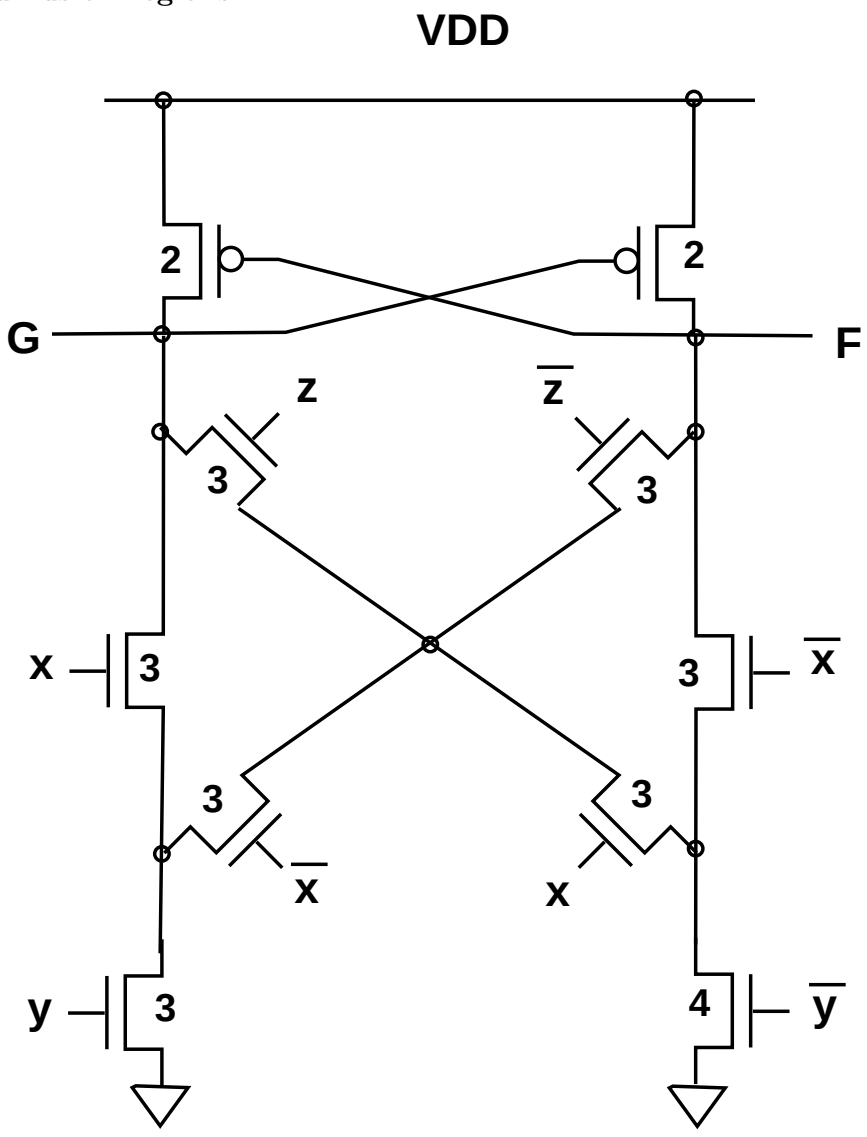
D = ____

E = ____

F = ____

3. (20 points)

Use the Elmore delay approximation to find the worst-case fall delay at output F for the following circuit. The gate sizes of the transistors are shown in the figure. Use the assumption that the diffusion capacitance is equal to the gate capacitance and that a minimum sized transistor has gate and diffusion capacitance equal to C. The resistance of a nMOS transistor with unit width is R. Also assume NO sharing of diffusion regions.

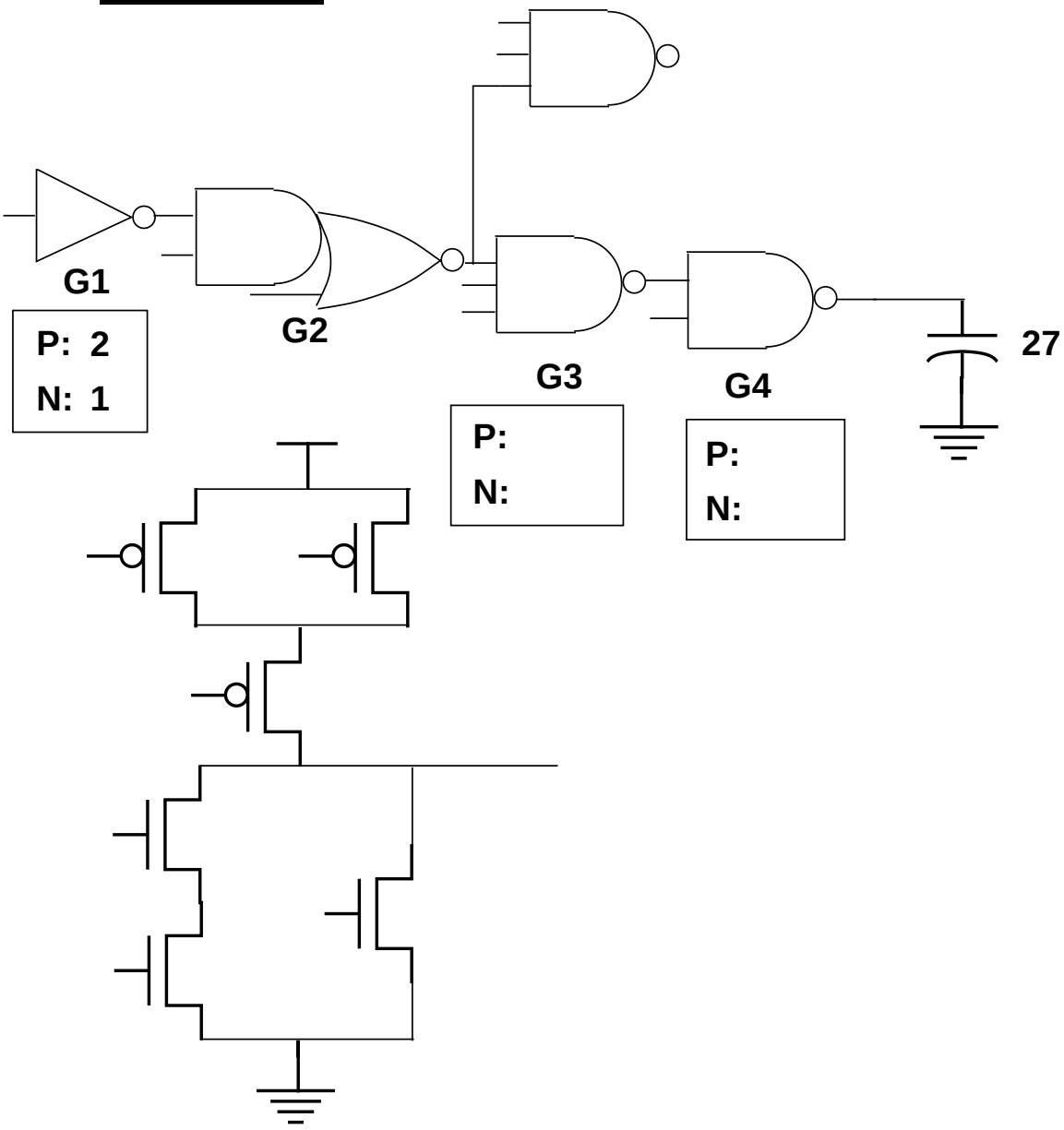


Delay = $\boxed{}$

4. (25 points)

Find the sizes of the transistors for the circuit below for the least delay from the input to the output. Label the sizes in the boxes for the simple gates and besides the transistors in the figure for the compound AOI21 gate.

Delay =



5. (20 points)

A four-level circuit has been designed to have the least delay, D, from input to output, which can be written as the sum of the path effort delay and the path parasitic delay, $D = D_F + P$.

(a) If the output capacitance is now 2 times the original capacitance, with all other parameters remaining the same, what will be the increase in delay of the circuit as a multiple of the original path effort delay, D_F?

Increase in Delay = ☐

(b) What will be the increase in delay if the output capacitance is the same, but the parasitic delay is now 2 times the original?

Increase in Delay = ☐

(c) If the original circuit is designed using 3-input NAND gates, what will be the increase in delay, as a fraction of D_F if each gate is replaced with a 3-input NOR gate (with the output capacitance remaining the same)?

(Delay Increase)/D_F = ☐

Spring 2006 | VLSI Design EXAM. I | J. Abraham March 1, 2006

Name: Student, A

Open Book, Open Notes. Time Limit: 75 minutes (pace yourself). Check for 5 pages in exam.

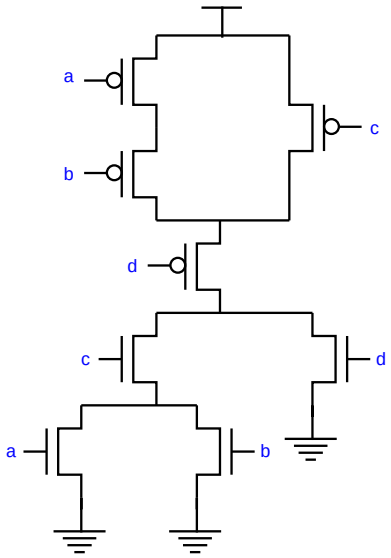
Write all your answers in the spaces/boxes provided.

Show any calculations in these pages using the back of the pages if needed. State clearly any assumptions made.

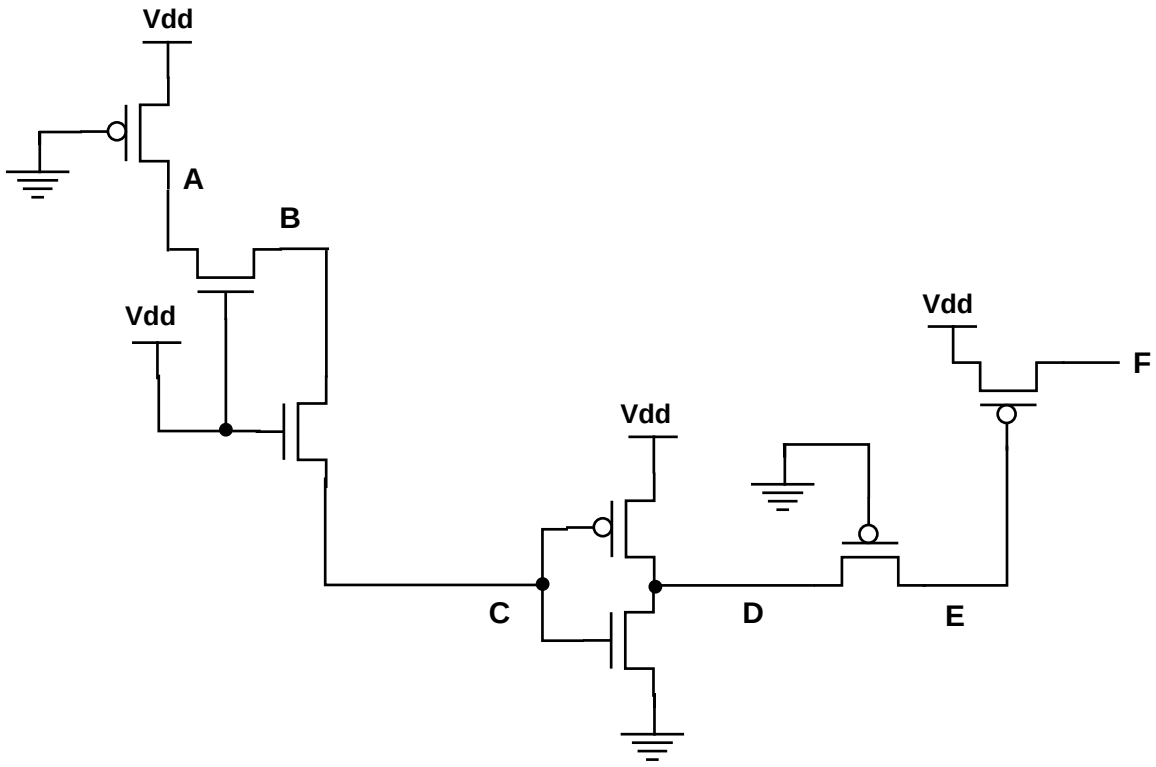
PROBLEM	MAX	POINTS
1	15	
2	20	
3	20	
4	25	
5	20	
TOTAL	100	

1. (15 points)

Size the transistors in the circuit below so that it has the same drive strength, in the worst case, as an inverter that has PW = 3 and NW = 2. Use the smallest widths possible to achieve this ratio. Write down the size next to each transistor.



2. (20 points) Find the voltages at each of the nodes, A, B, C, D, E and F below. Use the following circuit parameters:
$V_{dd} = 5V$, $V_{tn} = 0.5V$, $|V_{tp}| = 1.5V$.



A = ____

B = ____

C = ____

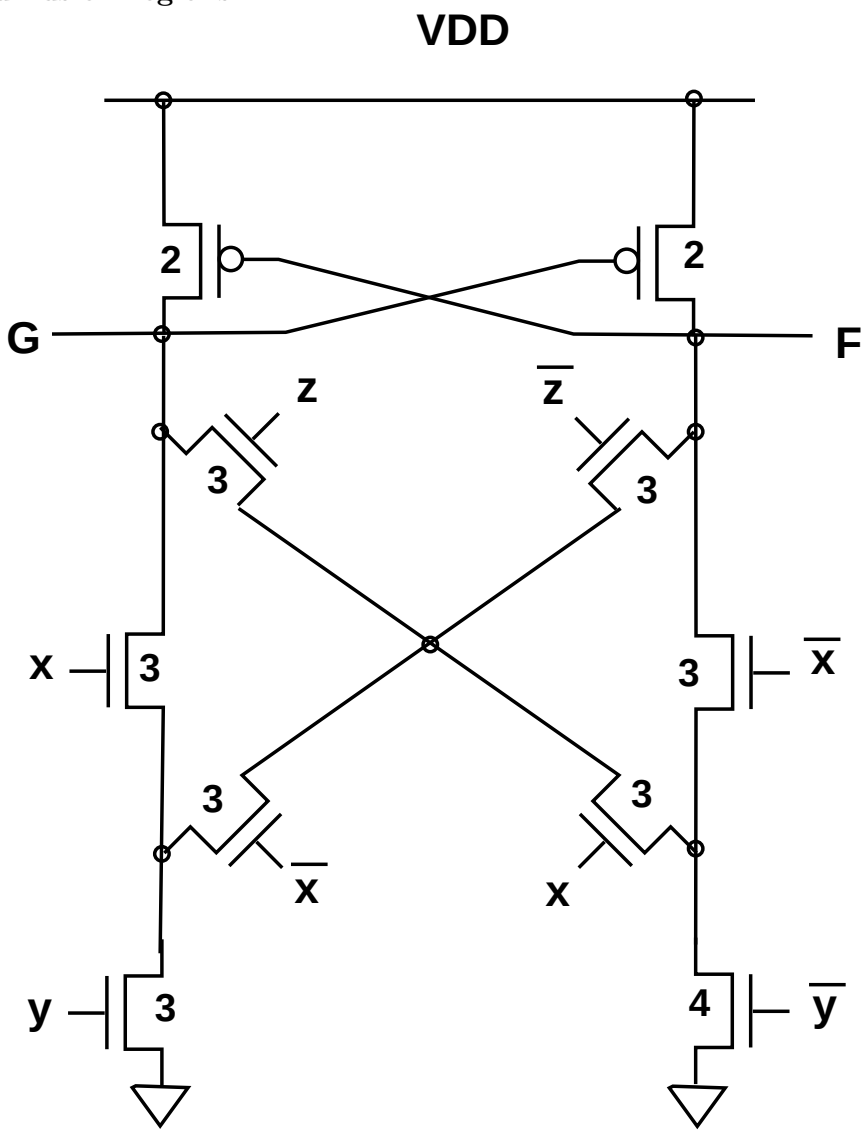
D = ____

E = ____

F = ____

3. (20 points)

Use the Elmore delay approximation to find the worst-case fall delay at output F for the following circuit. The gate sizes of the transistors are shown in the figure. Use the assumption that the diffusion capacitance is equal to the gate capacitance and that a minimum sized transistor has gate and diffusion capacitance equal to C. The resistance of a nMOS transistor with unit width is R. Also assume NO sharing of diffusion regions.

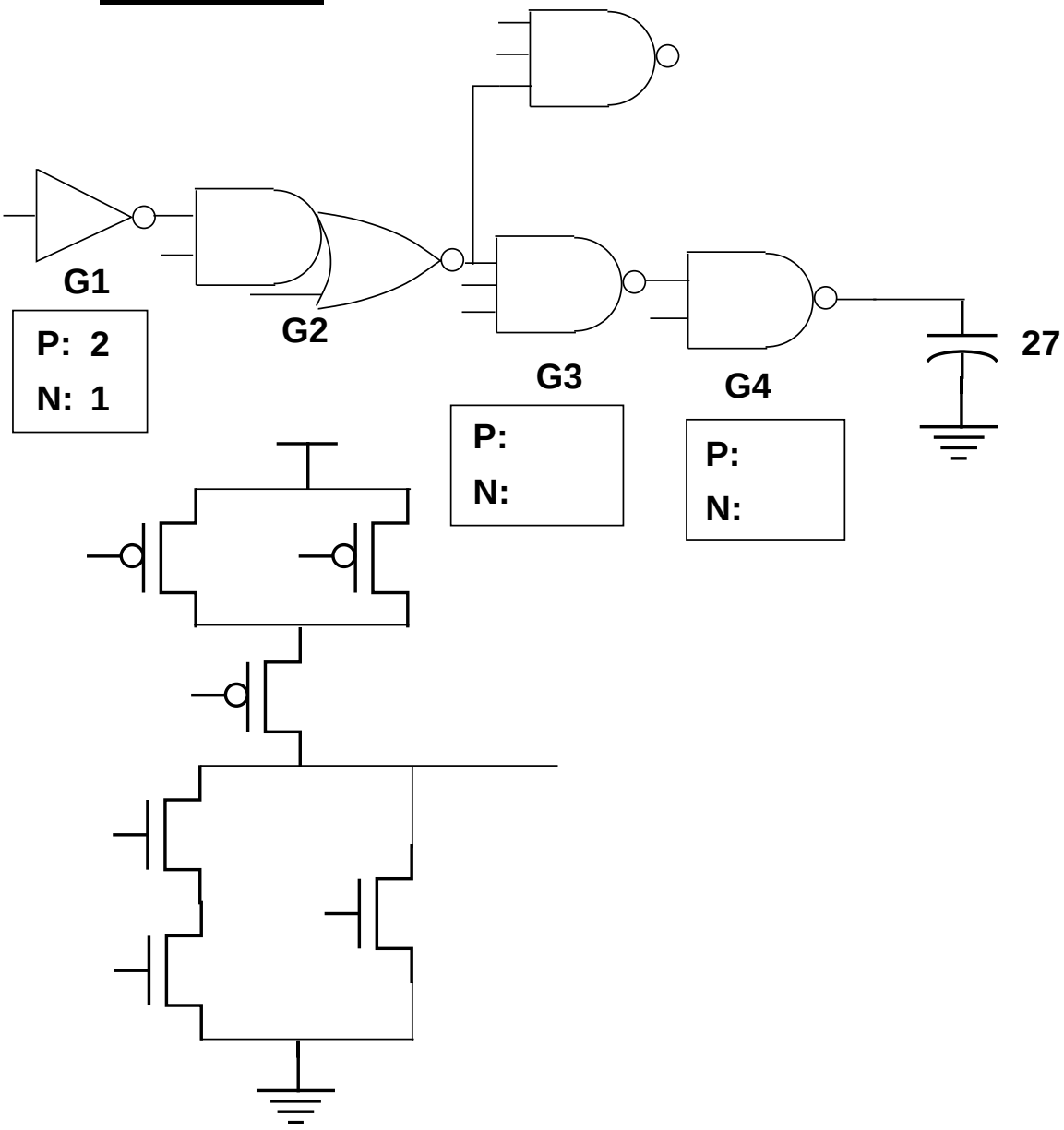


Delay = $\boxed{}$

4. (25 points)

Find the sizes of the transistors for the circuit below for the least delay from the input to the output. Label the sizes in the boxes for the simple gates and besides the transistors in the figure for the compound AOI21 gate.

Delay =



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Increase in Delay = ☐

(b) What will be the increase in delay if the output capacitance is the same, but the parasitic delay is now 2 times the original?

Increase in Delay = ☐

(c) If the original circuit is designed using 3-input NAND gates, what will be the increase in delay, as a fraction of D_F if each gate is replaced with a 3-input NOR gate (with the output capacitance remaining the same)?

(Delay Increase)/D_F = ☐

NAME:

- Time = 180 mins
- Closed book/notes; one crib sheet
- Write your answers on the exam
- Show your work and give explanations
- Absolutely no questions will be entertained—if you feel a question is ambiguous or incomplete, make and state reasonable assumptions.

Manufacturing

Write 2–3 sentence descriptions of the following terms:

- Lithography

- Chemical-mechanical polishing

- Ion-implantation

6 marks

Layout

Draw the mask defining the polysilicon of a unit inverter in a 100nm process.

5 marks

Transistor theory

Suppose you designed a unit inverter in a 0.1μ CMOS process. The inverter is designed in static CMOS (i.e., the standard way) for equal rise and fall times, specifically, the nmos device is minimum length and width, and the pmos device is minimum length and $2\times$ minimum width.

The manufacturing process can result in upto

- a 10% variation in the width, and
- a 25% variation in the length

for the actual device that is fabricated.

(This is true for both nmos and pmos devices, and the variations are independent.)

Assume that the supply voltage is 1 Volt, and $|V_T| = 0.2V$ for both nmos and pmos devices.

Recall that in the absence of variation, the inverter switching threshold voltage[1] will be $V_{DD}/2$.

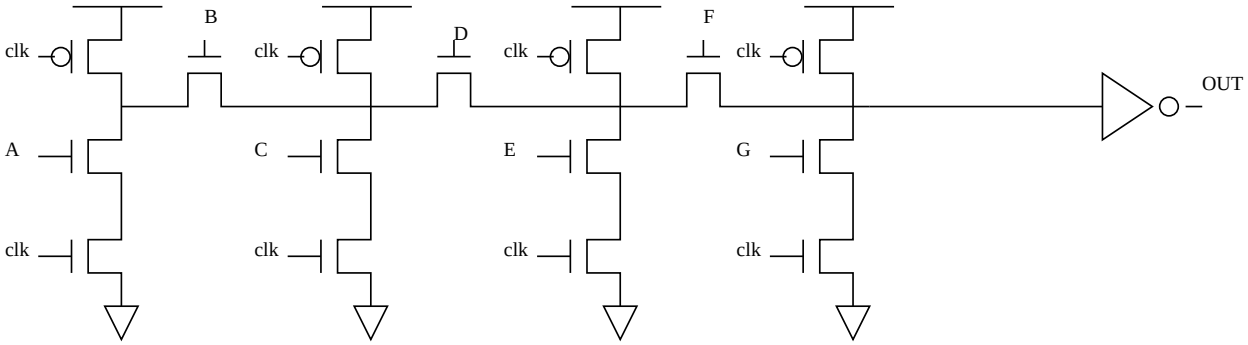
In the presence of variation within the ranges above, what is the minimum and maximum switching threshold?

12 marks

[1] the inverter switching threshold voltage is the input voltage for which $V_{out} = V_{DD}/2$

Circuit families

1. For the dynamic circuit below, write the function computed at the output as a function of the inputs.



8 marks

2. Describe how the circuit above could be used in a high-performance adder.

5 marks

Datapath

You are to design logic that takes 8 bits of input $A_0, A_1, \ldots, A_7$, and outputs 8 bits of output $B_0, B_1, \ldots, B_7$.

The outputs are defined by the following equation:

$$B_i \;=\; A_0 + A_1 + \cdots + A_i$$

You are required to use nothing but 2-input OR gates.

You must compute the outputs using as few OR gates as possible, subject to the constraint that there are no more than 3 gates on any path from input to output.

12 marks

Adders

A full-adder has 3 inputs and 2 outputs; the outputs implement the following two logic equations:

$$\begin{aligned} C_{out} &= A \cdot B \ + \ B \cdot C_{in} \ + \ A \cdot C_{in} \\ S_{out} &= A \oplus B \oplus C_{in} \end{aligned}$$

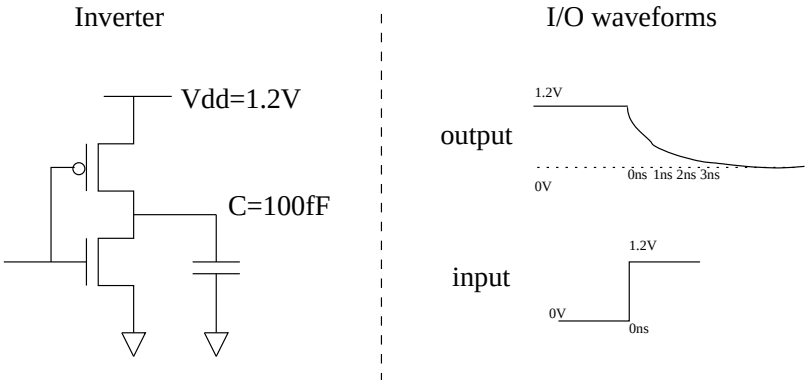
Show that if the inputs to the full-adder are inverted, then so are the outputs.

Use this fact to design a 4-bit ripple carry adder in static CMOS with reduced delay.

12 marks

Delay Analysis

Consider the circuit shown below. From the plot of V_{out} vs. time, estimate the effective resistance of the NMOS transistor. (Assume that all the capacitance seen on the output of the inverter is lumped into C.)



6 marks

RAMs

1. Draw a 6-T SRAM cell at the transistor level.

2. What must the relative sizes of the transistors in a 6-T SRAM cell be to guarantee read-stability and write stability? Explain how these sizes guarantes read-stability and write-stability.

15 marks

Test/Verification

1. What is the most common way in which a chip fails because of manufacturing defects?

4 marks

2. Describe BIST. Specifically address benefits and shortcomings, in addition to the underlying principles.

12 marks

Power

Consider a ROM in a 100 nm process, with a 1.2 V supply. The ROM has 64 words, each 32 bits wide.

The ROM uses pseudo-nmos decoders. The pmos pull-up transistor has a β of $75\mu A/V^2$ and $|V_{tp}| = 0.4V$.

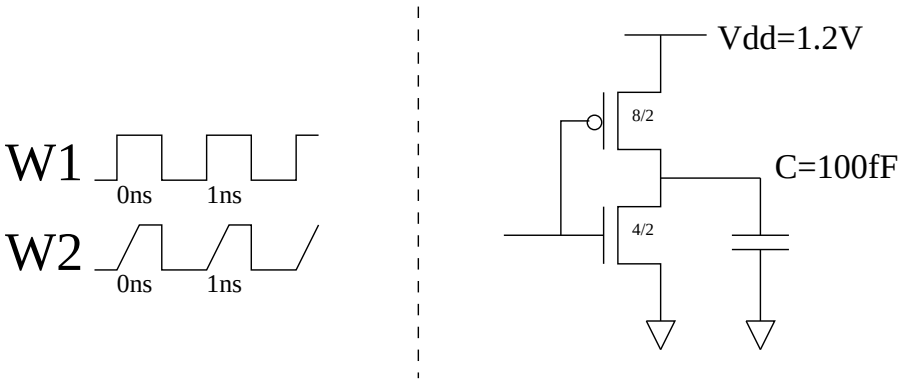
Compute the static power drawn by the ROM decode logic.

10 marks

Power

The inverter is implemented in a 100 nm process. Compute the power consumed by the inverter below when it is driven by the input $W1$—a square wave which swings from 0V to supply, with a duty cycle of 50% and frequency of 1 Ghz..

Does the power increase, decrease or stay the same when the input is $W2$?



10 marks

Scaling

1. Give the single most important reason why gate oxide thickness has reduced as processes have scaled.

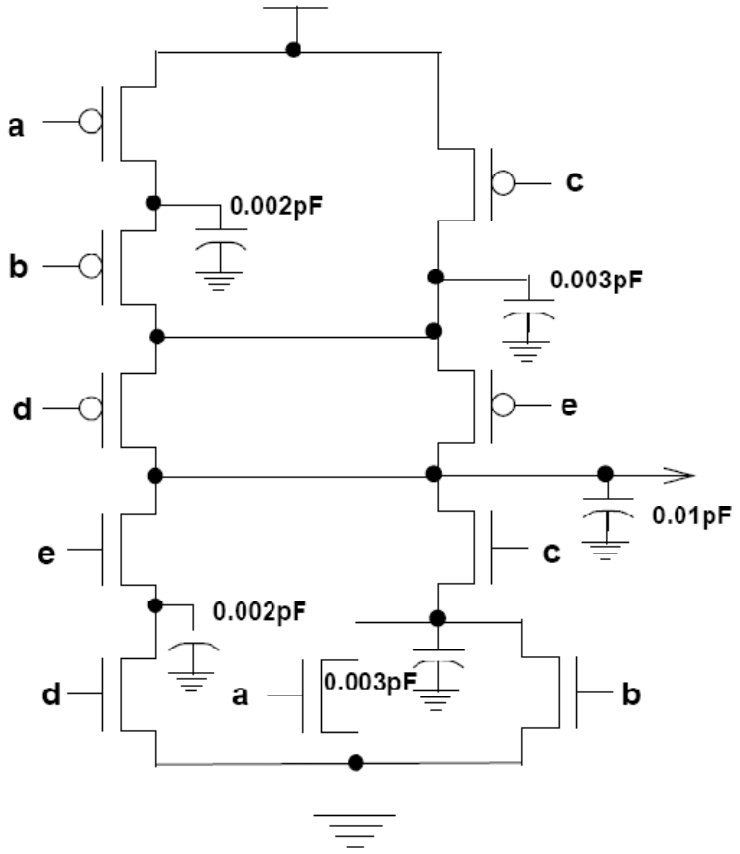
4 marks

2. In a 65nm process, under the best of circumstances—highest metal layer, optimum repeatering, no coupling, etc.—the delay of interconnect is of the order of 50 ps/mm. This translates into a delay of 1000 ps for a wire traveling from one end of a 10mm x 10mm die to the diagonally opposite end. Does this imply that such a design cannot run faster than 1 Ghz?

6 marks

Previous EE360R Final Exam Questions

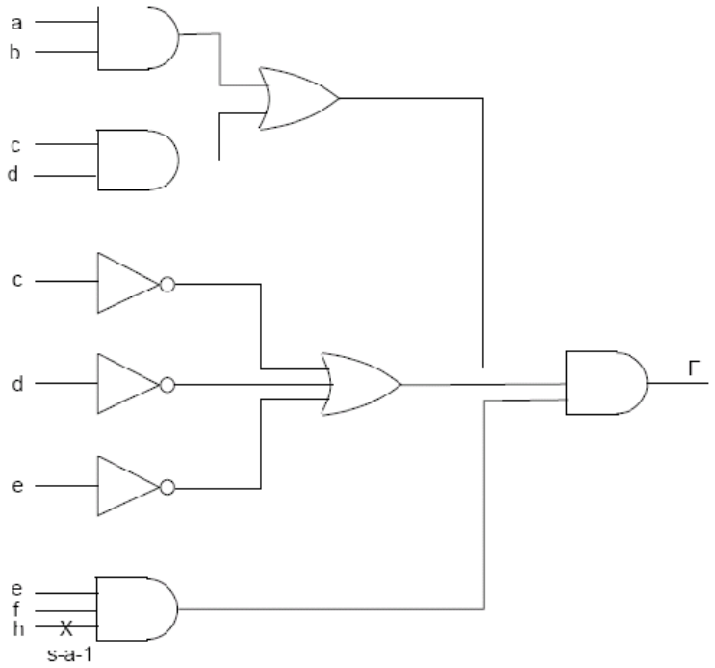
In the static CMOS circuit below, the on-resistance of each n-channel transistor is 5 KOhms and that of a p-channel transistor is 10 KOhms. The gate capacitance of an n-channel transistor is 0.02pF and p-channel transistor is 0.03pF. The source/drain capacitance of an n-channel transistor is 0.001pF and for a p-channel transistor is 0.002pF. The routing capacitances for interconnections are lumped at the nodes as shown.



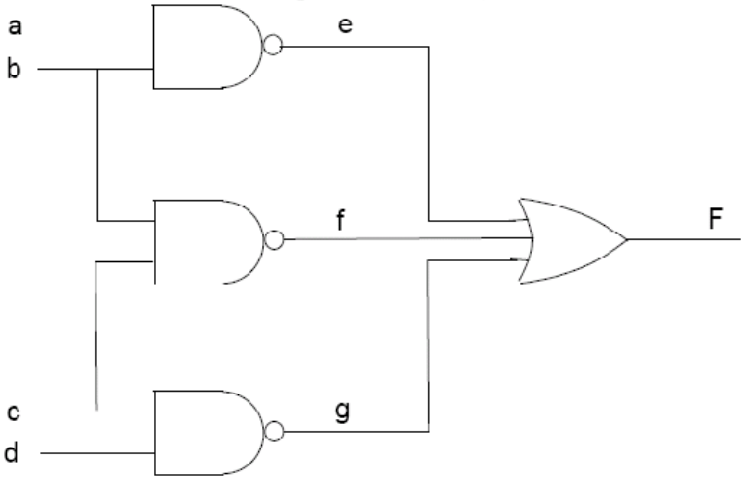
(a) Find the delay when (a b c d e) makes the following transitions:
0 0 0 0 0 ⇒ 0 0 0 1 1 ⇒ 0 0 0 0 1.

Previous EE360R Final Exam Questions

(a) Find a test for the line h stuck-at-1 in the figure below.



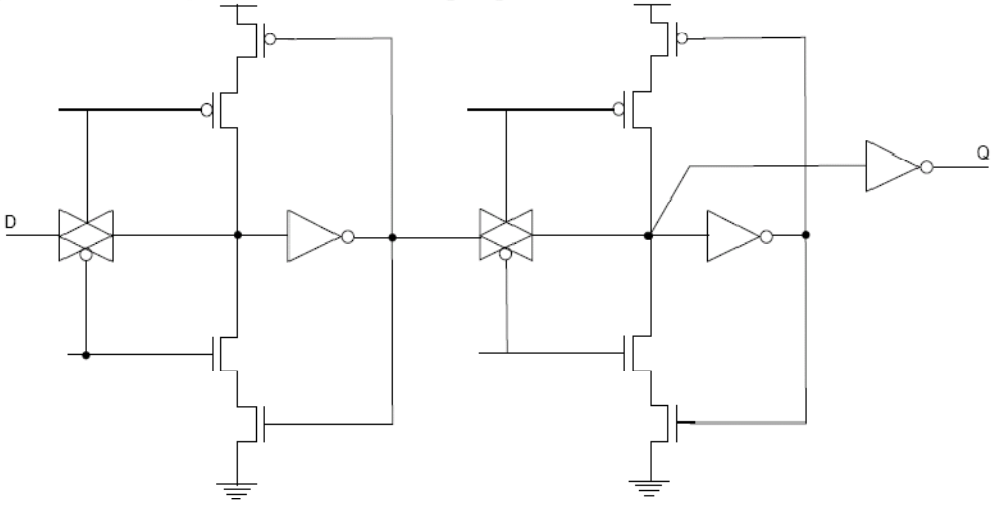
(b) Perform test generation for the following faults and explain the results.



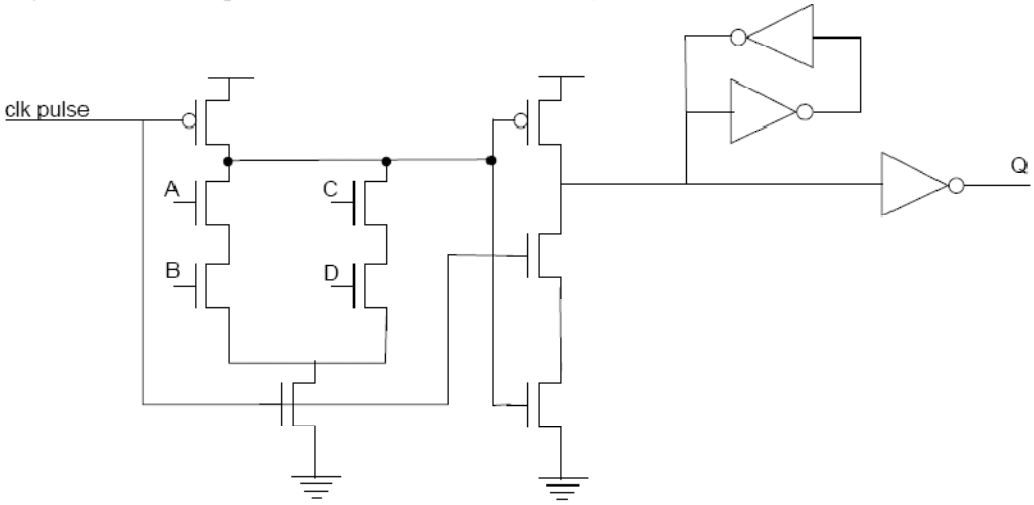
(i) g s-a-0
(ii) e s-a-1
(iii) f s-a-0

Previous EE360R Final Exam Questions

(a) Label the four inputs in the circuit below with the clock symbols CLK and CLKB (complement of CLK) so that the flop latches at the falling edge of the clock.



(b) Analyze the following circuit and write down the equation for its function.



Previous EE360R Final Exam Questions

a) Draw the schematic for a static CMOS network for the following function using the minimum number of transistor. Do NOT assume that the inverted inputs are available.

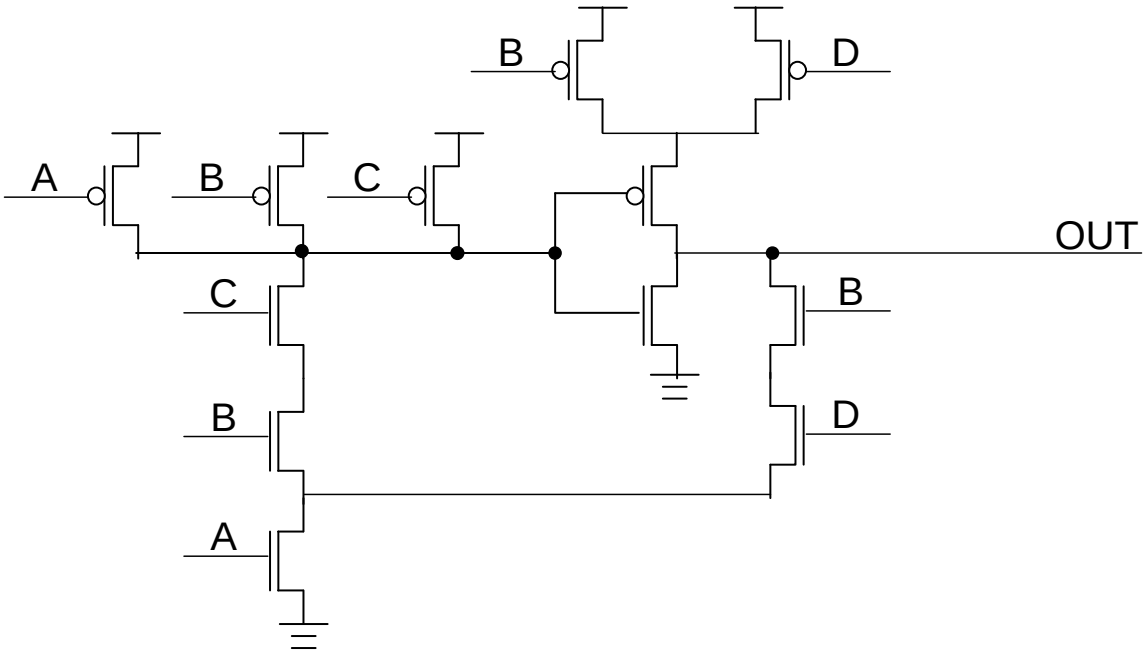
Y = A'B'C' + ABC' + A'B'C + ABC

b) Draw a Domino CMOS schematic (with PMOS precharge and feedback hold device) of the following functions F1 and F2 using the minimal number of transistors.

F1 = (M·N + W) · P · (Q·R + S·T)

F2 = T·S + R·Q

Previous EE360R Final Exam Questions

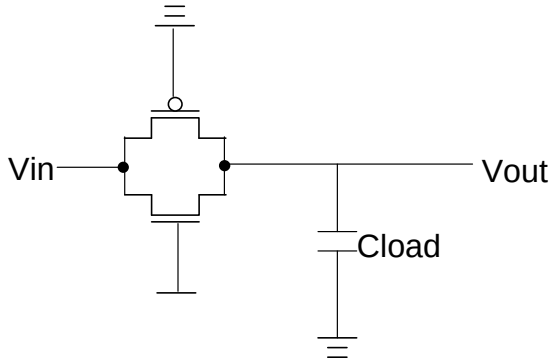


a) Write down the function OUT implemented by the circuit below:
Minimize the number of transistors and draw the new schematic. Do NOT assume that the complementary inputs are available.

Previous EE360R Final Exam Questions

Describe the regions of operation for the NMOS and PMOS device in the transmission gate shown below in terms of linear, saturation and cutoff as the capacitor is charged or discharged:

Vtn = 1.0V Vtp=1.0V



a) Initial conditions: Vin = 5.0V Vout = 0.0V

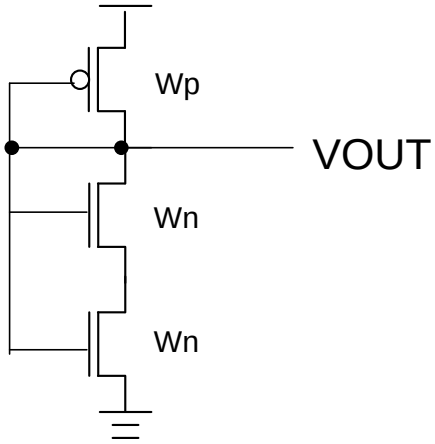
Condition	PMOS Region	NMOS Region
Vin = 5.0V Vout = 0.0V		
Vin = 5.0V Vout = 2.5V		
Vin = 5.0V Vout = 5.0V		

b) Initial conditions: Vin = 0.0V Vout = 5.0V

Condition	PMOS Region	NMOS Region
Vin = 0.0V Vout = 5.0V		
Vin = 0.0V Vout = 2.5V		
Vin = 0.0V Vout = 0.0V		

Previous EE360R Final Exam Questions

a) Determine the voltage on node VOUT.



Assume: $\mu_n = 2 \cdot \mu_p$ Ln = Lp Vtn = Vtp

Both transistors are operating in the saturation region.

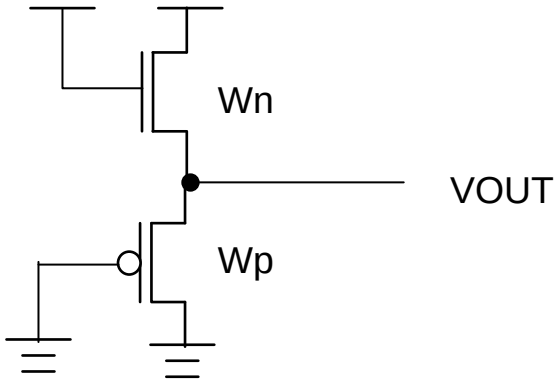
Express value on VOUT as a function of Wn, Wp and VDD

b) Determine the voltage on node VOUT.

Assume $\mu_n = 2 \cdot \mu_p$ Ln = Lp Vtn = 1.0V Vtp = 1.0V

Both transistors are operating in the saturation region.

Express value on VOUT as a function of Wn, Wp and VDD



Previous EE360R Final Exam Questions

a) Explain how the parasitic (field) transistor is formed between two n-channel transistors. How would you reduce the effects of these parasitic transistors?

b) How does a "dummy collector" prevent latch up?

a) Explain how the shape of the input waveform to a CMOS inverter alters the delay through the gate.

b) Explain how you would estimate and plan the clock distribution scheme in a chip. Summarize the parameters that are relevant and explain how your scheme deals with these.

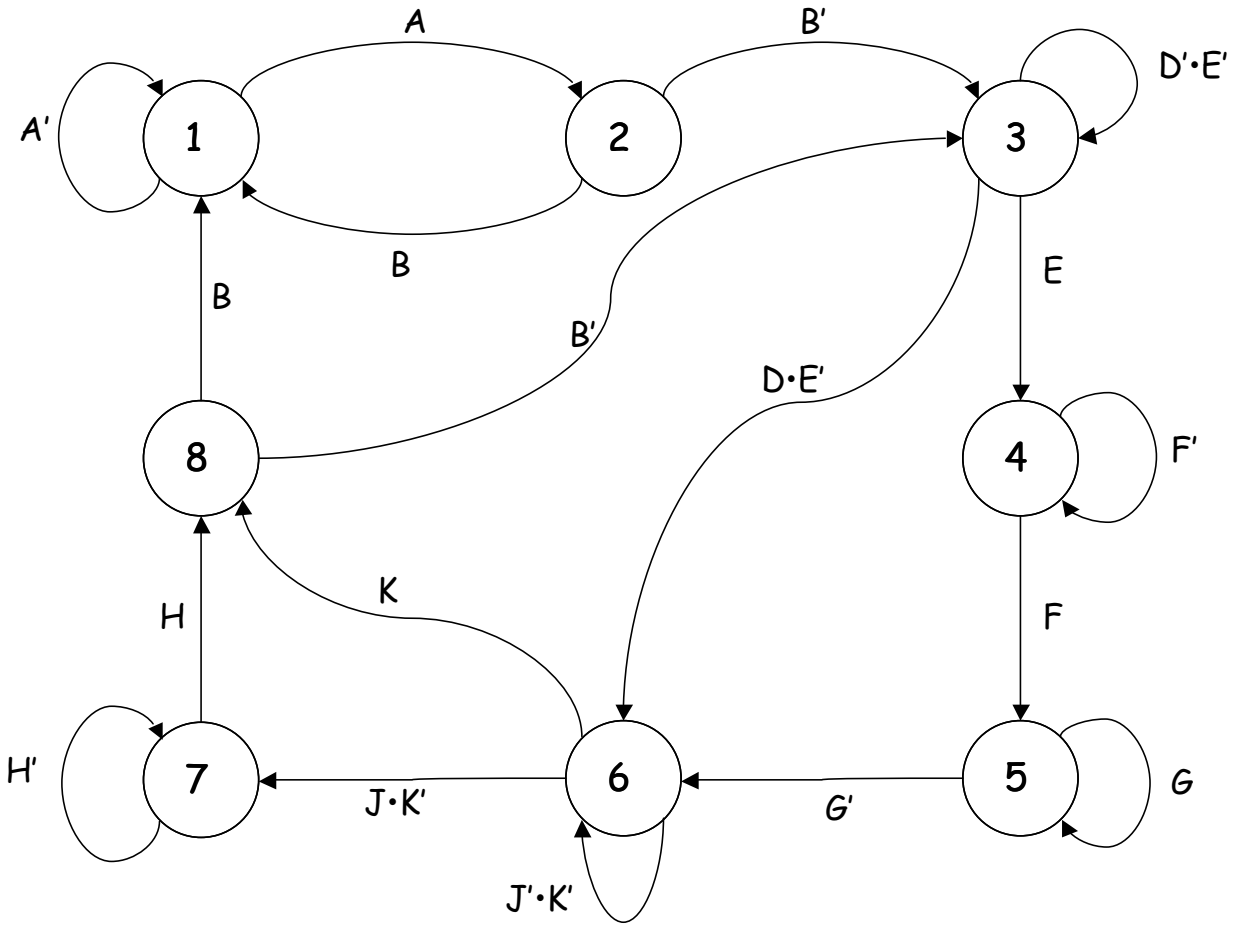
a) What limits the VDD supply voltage in a CMOS technology (i.e., how low or high can you set it)? Explain what you expect the effects of these two voltage extremes to be on the internal circuits. Suggest situations where both of these voltage extremes might be of use.

b) Suggest the approaches you would take to reduce the power dissipation of a CMOS chip.

Previous EE360R Final Exam Questions

a) Complete the following state diagram for arcs: 8->3 6->7 3->6

Confirm that all other arcs are correct. If not, correct the equation(s).



b) How many memory elements (Flip-Flops) are required to implement the state machine for:

One-Hot Encoding:

Fully Encoded:

c) How many inputs are required for the state machine including state inputs for:

One-Hot Encoding:

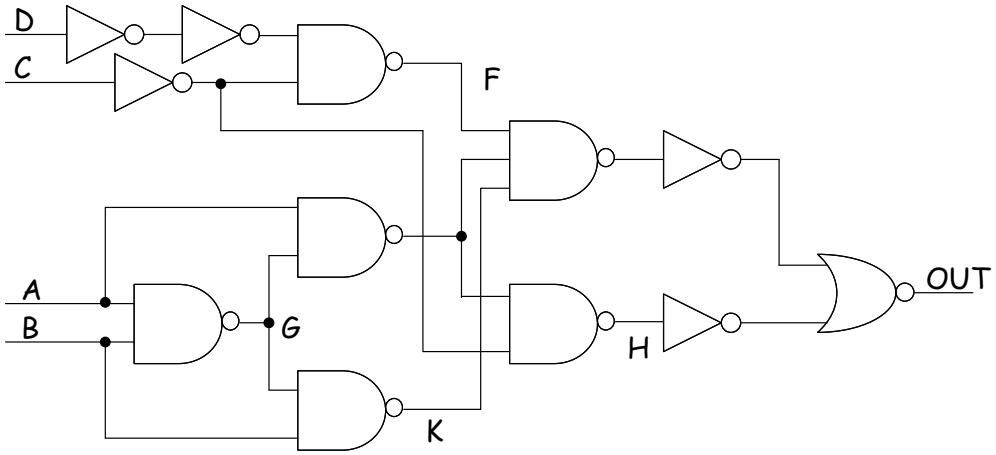
Fully Encoded:

Previous EE360R Final Exam Questions

d) Fill out the following State Table for the state machine described above:

Current State	*A*	B	D	E	F	G	H	J	K		*Next* State
1	0										1
1	1										2
2		1									1
2		0									3
3			0	0							3
3				1							4
3			1	0							6
4					0						4
4					1						5
5						1					5
5						0					6
6								0	0		6
6								1	0		7
6									1		8
7							0				7
7							1				8
8		0									3
8		1									1

Previous EE360R Final Exam Questions



a) Find vector(s) that allow the detection of a SA-1 and SA-0 fault on node F.

SA-1: Cannot detect.

SA-0: ABCD { 001X, 111X } D is a don't care

b) Find vector(s) that allow the detection of a SA-1 and SA-0 fault on node G.

SA-1: ABCD {11XX } C & D are don't care

SA-0: ABCD { 1000, 101X, 011X }

c) Find vector(s) that allow the detection of a SA-1 and SA-0 fault on node H.

SA-1: ABCD { 0101, 0100, 0001, 1101 }

SA-0: ABCD { 011X, 10XX }

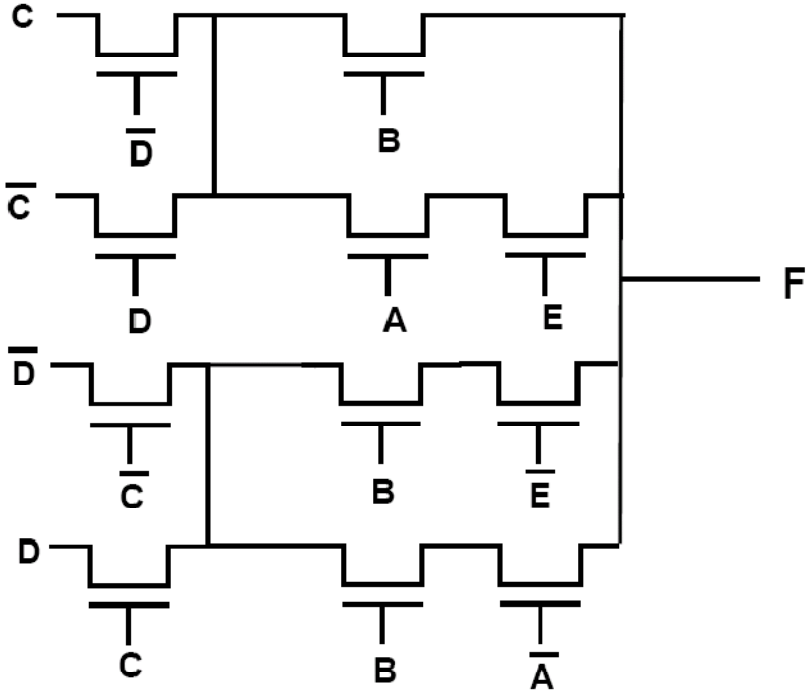
d) Find vector(s) that allow the detection of a SA-1 and SA-0 fault on node K.

SA-1: ABCD {011X }

SA-0: ABCD { 001X, 111X }

Previous EE360R Final Exam Questions

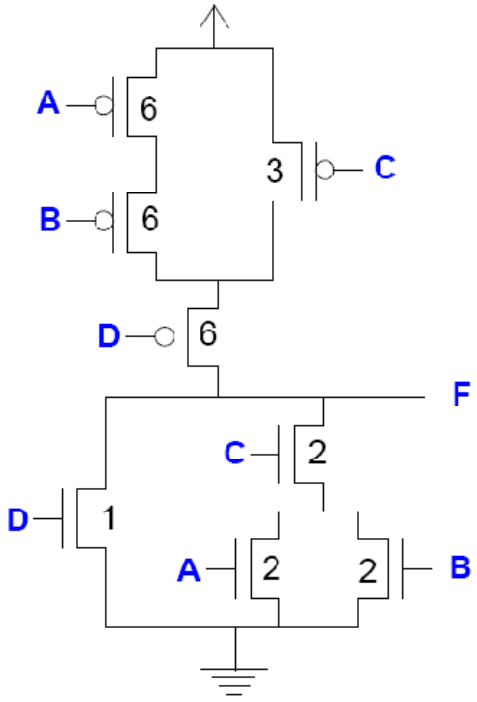
Write down the logic function implemented by the circuit below; use parantheses in the expression to reduce the number of literals.



F =

Previous EE360R Final Exam Questions

Find the largest as well as contimination delays for both 0-1 and 1-0 transitions for the circuit below. The widths of the transistors are given. Assume that a minimum width transistor will have an on-resistance of **R** and a gate capacitance of **C**; the source and drain capacitances are also C, and there is **no** sharing of diffusions. Give the input combinations which produce the respective delays (assuming that the internal nodes are charged or discharged as appropriate).



Input (ABCD) producing the largest rise delay:

Largest rise delay =

Input (ABCD) producing the largest fall delay:

Largest fall delay =

Input (ABCD) producing the smallest rise delay:

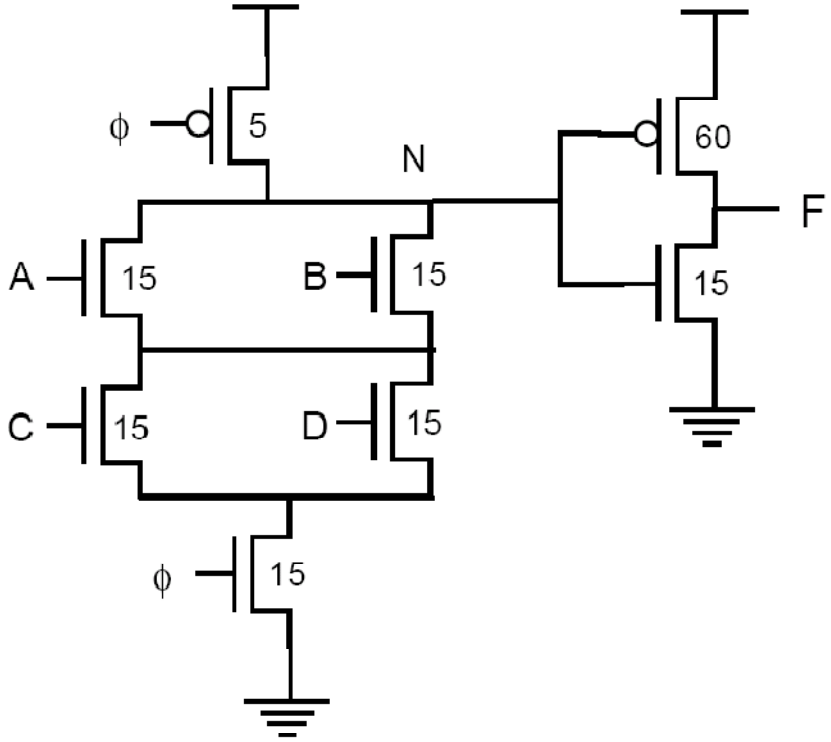
Contamination rise delay =

Input (ABCD) producing the smallest fall delay:

Contamination fall delay =

Previous EE360R Final Exam Questions

The domino circuit has the widths of the transistors shown next to them. Assume that a minimum width transistor has a gate capacitance of C, with the source and drain capacitances also each equal to C. Assume no sharing of diffusion.



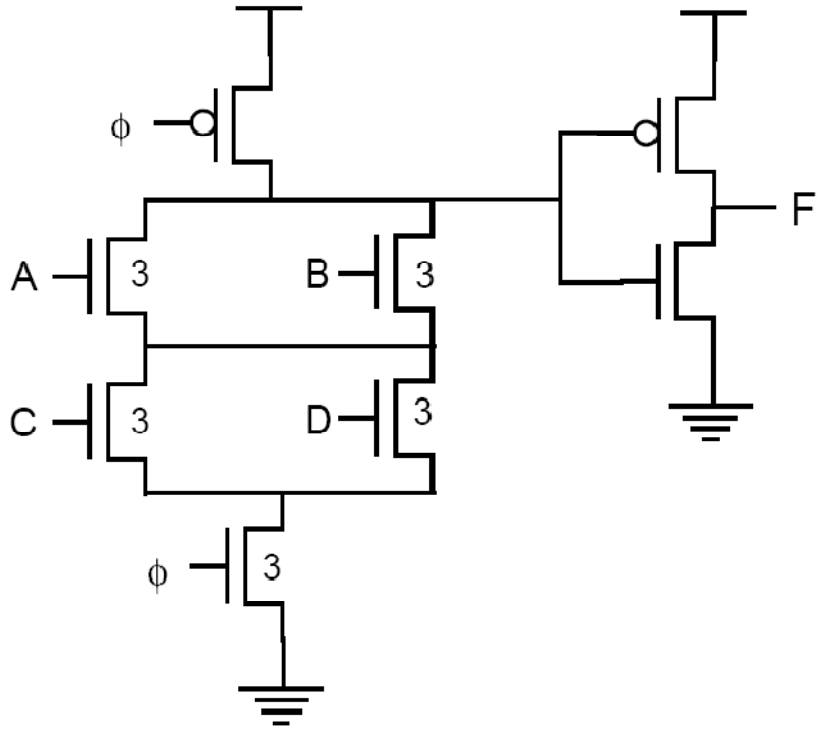
(a) Under the worst-case input sequence, what is the largest voltage drop on the dynamic node, N?

(b) Give a sequence of inputs (ABCD) which will cause the voltage drop on N.

(c) How should the static inverter be sized to cause a voltage drop (noise) of at most 20% on the node N?

Previous EE360R Final Exam Questions

The best stage effort for a domino circuit has been found to be between 2.0 and 2.76 (for unfooted and footed blocks). The circuit below has the transistor widths labeled for the dynamic portion. The static inverter is a standard Hi-Skew with a logical effort of 5/6.



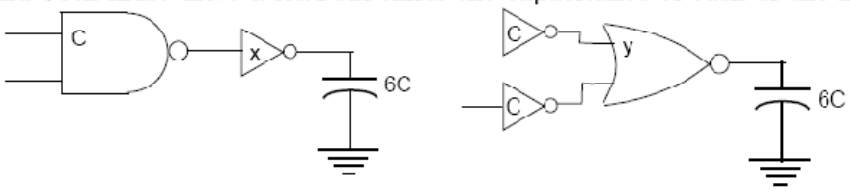
(a) If the stage effort is 2.5, what would be the corresponding path electrical effort, H (using the standard logical effort formulation)?

(b) What would be the delay of the circuit for the design in (a)?

(c) What would be the sizes of the P and N transistors in the static inverter (for the same design)?

Previous EE360R Final Exam Questions

Consider the two different implementations of an AND gate below. Both have an input capacitance of C and both must drive a load six times the capacitance of each of the inputs.



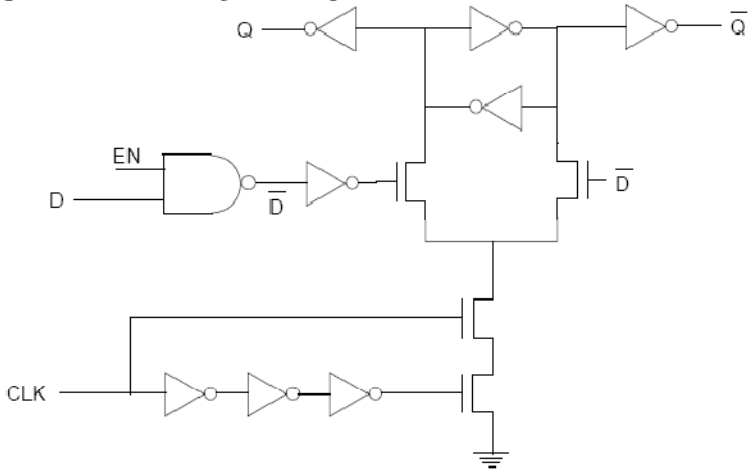
(a) What is the path effort of each design?

(b) Which design will be the fastest? Explain.

(c) Compute the sizes of the logic gates, x and y to achieve the least delay.

Previous EE360R Final Exam Questions

The inverters in the flip-flop below have rise and fall delays of 50 pS. The NAND gate has a rise delay of 100 pS and a fall delay of 150 pS.



Neglecting the delay of the nMOS transistors, what are the parameters of the flip-flop?

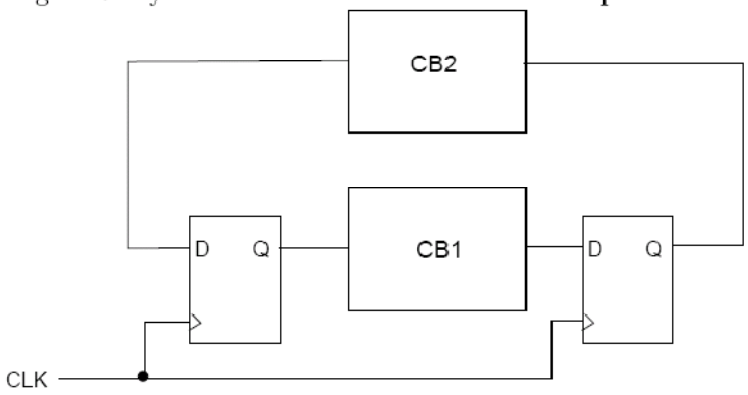
(a) Setup time

(b) Hold time

(c) CLK-Q delay

Previous EE360R Final Exam Questions

The sequential circuit below has two flops and two combinational blocks, CB1 and CB2. The design is made using a library which includes inverters with a 25 pS rise and fall delay.



The parameters of the flops are: $t_{pcq} = 100pS, \quad t_{ccq} = 20pS, \quad t_{setup} = 50pS, \quad t_{hold} = 100ps$

The parameters of the combinational block are as follows.
CB1: $t_{pd} = 250pS, t_{cd} = 100pS$
CB2: $t_{pd} = 350pS, t_{cd} = 50pS$

(a) Will the circuit work correctly? Explain and, if not, suggest a fix which will not affect the maximum frequency at which the circuit can be operated.

(b) If the circuit can be operated correctly, what is the maximum frequency at which it will work correctly?

(c) Suggest a modification to the clock circuitry to increase the frequency found in (b). Explain.

Previous EE360R Final Exam Questions

An embedded hardware accelerator in a system-on-chip is designed in a 1 V, 90 nm process, and has 1 million logic transistors with an average width of 12λ. The gate capacitance, $C_g = 2fF/\mu m$. The gates have an activity factor of 0.2.

(a) What is the maximum clock frequency if the dynamic power should not exceed 20 mW?

(b) If the subthreshold leakage is $20nA/\mu m$ and the gate leakage is $2nA/\mu m$, and if half the transistors are off (on average), what is the leakage power?

360R — Final

Name:

- Time = 180 mins, Max marks 111
- Closed book/notes; one crib sheet
- Write your answers on the exam
- Show your work and give explanations

Figures are shown on separate pages at the end.

Layout

The cross-sectional view of an inverter is given in Figure Cross-Section. Identify the various regions as being SiO2, Poly, Metal, VDD, Gnd, n+, p+, n-well, and p-substrate.

12 marks

Transistor theory

Suppose you were to design an NMOS transistor in a 0.5μm CMOS process. The transistor width is 2.0μm, and length is 0.5μm.

The manufacturing process could result in a 25% variation in the threshold voltage, a 20% variation in the oxide thickness, and a 0.1μm variation in the width and in the length, for the actual device that is fabricated.

Assume that $V_{GS} = V_{DS} = 3V$; the threshold voltage is 0.5V.

What is the ratio of the maximum value of the drain current to the minimum value of the drain current that could flow through the fabricated device when it is in saturation?

12 marks

Circuit families

1. What problem with dynamic logic does domino dynamic logic overcome, and what is the primary limitation of domino dynamic logic?

5 marks

2. Give a transistor level schematic for a domino logic implementation of the function $A \cdot B \cdot C \cdot D \cdot E \cdot F$. No domino gate should have more than two inputs.

   (You are not required to specify devices sizes, just draw the transistors and the connections between them.)

10 marks

Datapath

The FF1 ("find-first-one") function takes an n-bit input vector $A[n-1:0]$, and returns and n-bit output $B[n-1:0]$, where $B[i] = 1$ if and only if $A[i] = 1$ and for all $j > i$, $A[j] = 0$.

Describe how you would implement the "find-first-one" (FF1) function on n inputs using static gates, specifically 2-input NAND, 2 i/p NOR, and INVERTERs.

Credit will be given to *efficient* solutions.

15 marks

Adders

Recall that a full-adder implements the following two logic equations:

$$\begin{aligned} C_{out} &= A \cdot B \ + \ B \cdot C_{in} \ + \ A \cdot C_{in} \\ S_{out} &= A \oplus B \oplus C_{in} \end{aligned}$$

It is easy to show (e.g., by examining the truth table for these equations) that if the inputs to the full-adder are inverted, then so are the output.

How can this fact be used to reduce the delay of a ripple-carry adder? Illustrate your reasoning on a 4-bit ripple carry adder.

15 marks

Delay Analysis

Consider the circuit shown in Figure Delay-Analysis. From the plot of V_{out} vs. time, estimate the effective resistance of the NMOS transistor. (Assume that all the capacitance seen on the output of the inverter is lumped into C.)

7 marks

RAMs

1. Describe three **similarities** between SRAMs and DRAMs. What is the single biggest **difference** between an SRAM and DRAM? How do SRAMs and DRAMs **compare** in performance and in density?

9 marks

2. Describe how you would use a 32 entry 8-bit word SRAM to implement a queue. Assume the queue read and writes are exclusive. Your queue has to signal whether it's full or empty. (You can use additional registers and logic.)

9 marks

Test/Verification

1. How do scan flops help simplify the problem of manufacturing test?

4 marks

2. Suppose you were designing a microprocessor.

   One approach to functionally verifying the processor is to ignore the internal units (e.g., the cache, the ALU, the pipeline control logic, et.c), and simply write large sets of test programs, and run them on both the RTL and the golder reference model (typically written in C).

   What are the two most significant benefits to verifying the internal units additionally?

4 marks

Deep Submicron

Suppose you were designing a chip in 45 nm technology, and you wanted to minimize power consumption.

The manufacturing process offers you two kinds of transistors—type F, which has a low V_T and a thin gate oxide, and type S, which has a high V_T and a thick gate oxide.

How do the type F and S transistors differ in terms of their power consumption and performance? How would you exploit them to reduce power in your design? (Be specific.)

9 marks

VLSI Design **J. Abraham**

Fall 2006 **EXAM. I** **October 16, 2006**

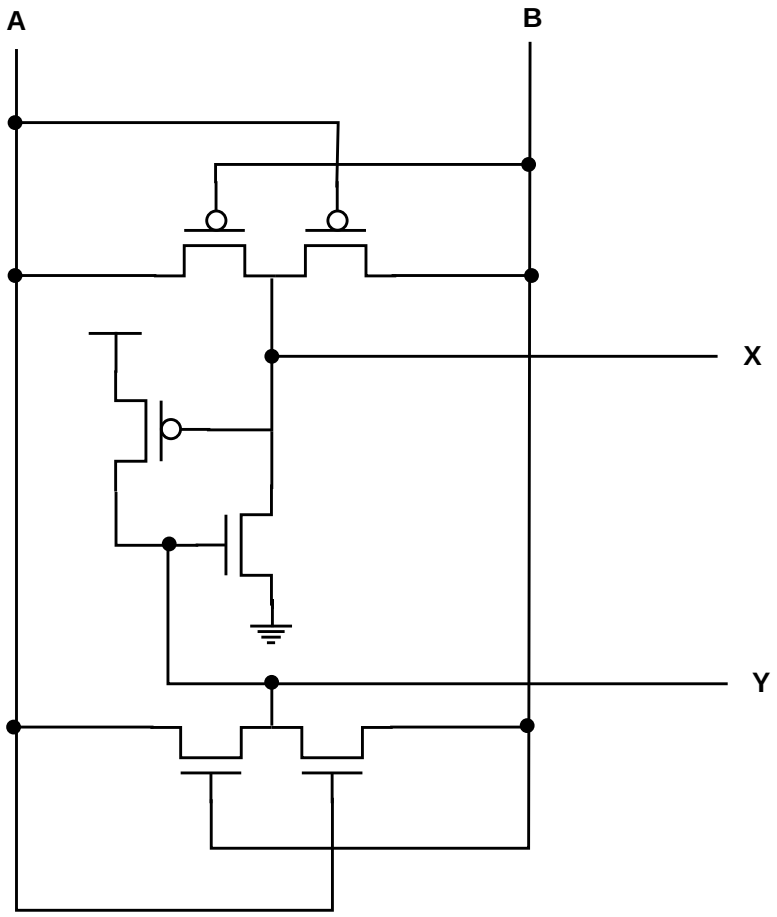
Name: Student, no. 4

- **Open Book, Open Notes.**
- **Time Limit: 75 minutes (pace yourself).**
- **Check for 6 pages in exam.**
- **Write all your answers in the spaces/boxes provided.**
- **Show any calculations in these pages using the back of the pages if needed.**
- **State clearly any assumptions made.**

PROBLEM	MAX	POINTS
1	20	
2	20	
3	20	
4	20	
5	20	
TOTAL	100	

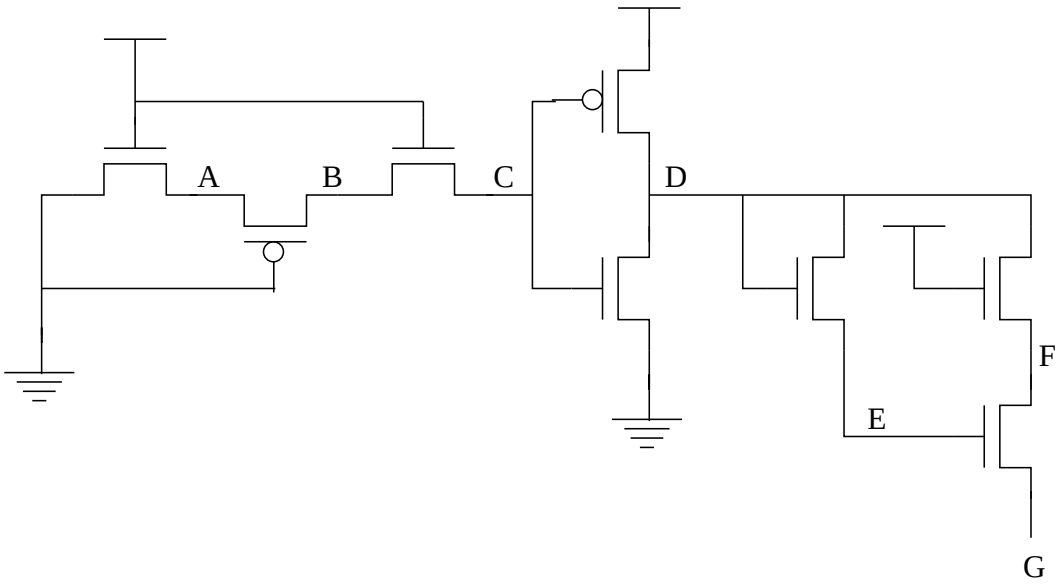
1. (20 points)

Find the functions X and Y implemented by the following circuit.



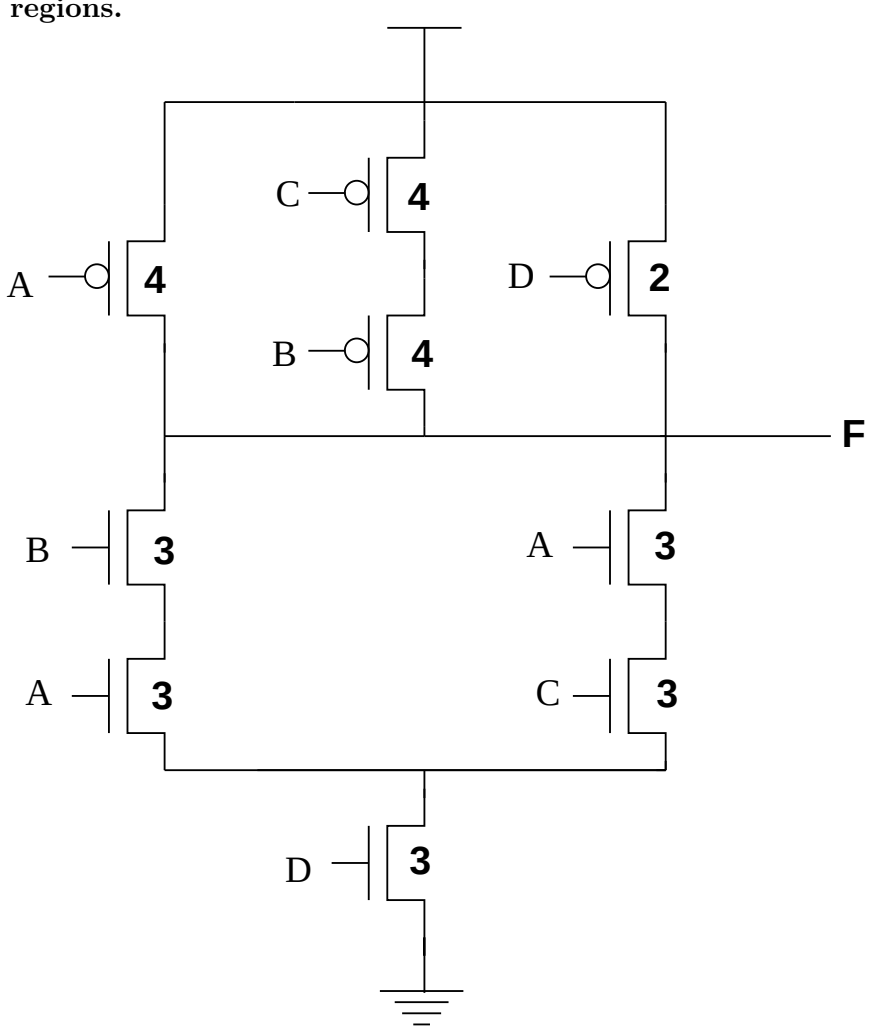
2. (20 points)

Write down the voltages at A, B, C, D, E, F, G in the following circuits, assuming that the initial voltage on each node is 1.5 volts. The relevant transistor parameters are, $V_{dd} = 3V$, $V_{tn} = 0.5V$ and $|V_{tp}| = 0.7V$.



3. (20 points)

Use the Elmore delay approximation to find the *worst-case* rise and fall delays at output F for the following circuit. The gate sizes of the transistors are shown in the figure. Use the assumption that the diffusion capacitance is equal to the gate capacitance and that a minimum sized transistor has gate and diffusion capacitance equal to C. The resistance of a nMOS transistor with unit width is R and the resistance of a pMOS transistor with width of 2 is also R. Also assume NO sharing of diffusion regions.



Input for worst-case rise delay (ABCD) = ____

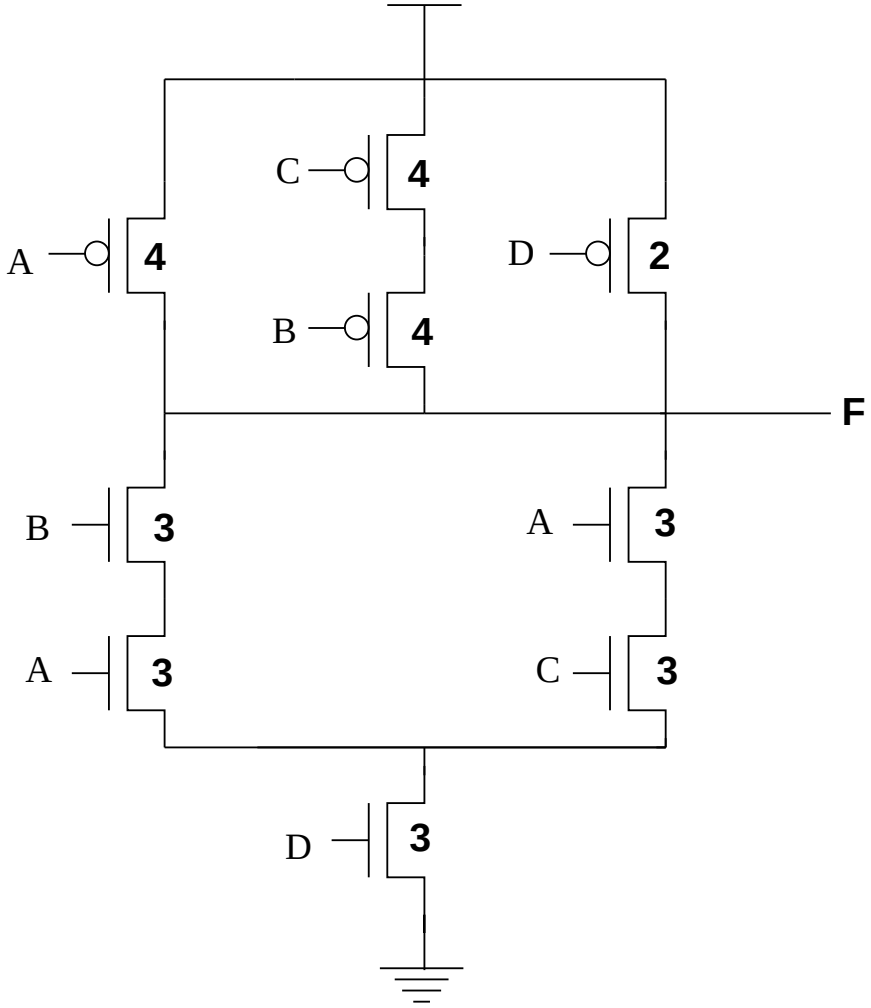
Worst-case rise delay = ____

Input for worst-case fall delay (ABCD) = ____

Worst-case fall delay = ____

4. (20 points)

Find the logical efforts for the inputs, A, B, C, and D in the circuit below.



Logical effort of A = ____

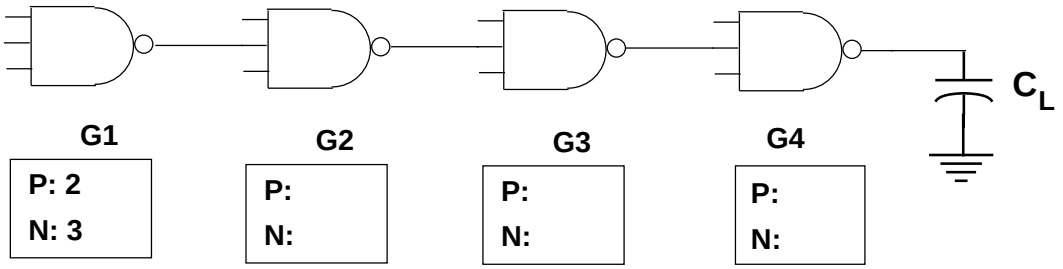
Logical effort of B = ____

Logical effort of C = ____

Logical effort of D = ____

5. (20 points)

(a) Find the sizes of the P and N transistors in the gates below if the output capacitance C_L is 840 units.



(b) If a chain of n inverters, starting with a 2:1 inverter, is driving a load of $3C_L$, what is the input capacitance at each stage for the least delay?

(c) Would the input capacitance in (b) depend on the type of gate being used in each stage? Explain.

	VLSI Design	**J. Abraham**
Fall 2006	**EXAM. II**	**November 20, 2006**

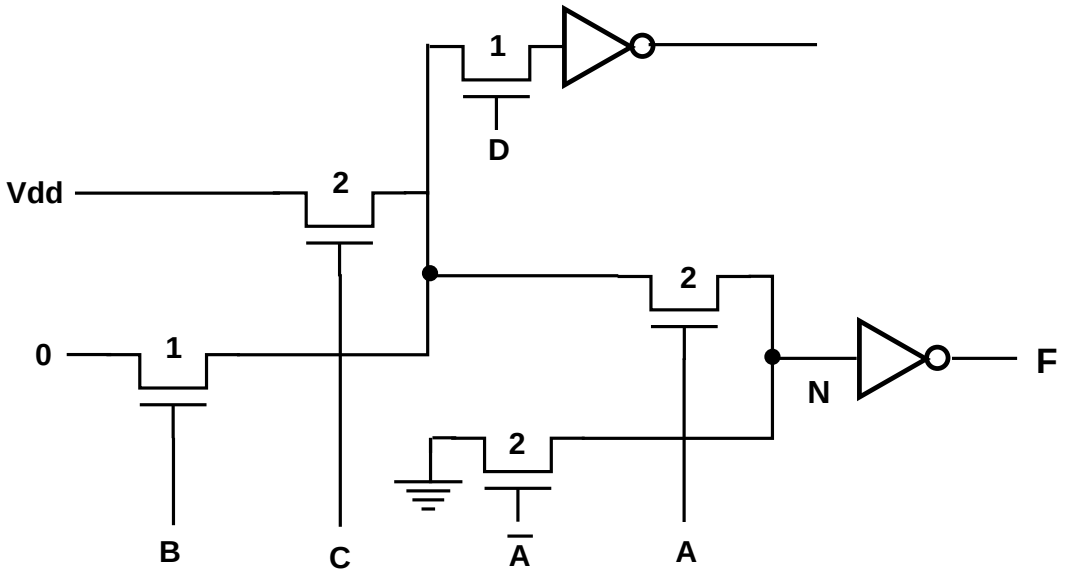
Name: Exam, No. 4

- **Open Book, Open Notes.**
- **Time Limit: 75 minutes (pace yourself).**
- **Check for 6 pages in exam.**
- **Write all your answers in the spaces/boxes provided.**
- **Show any calculations in these pages using the back of the pages if needed.**
- **State clearly any assumptions made.**

---

1. (20 points)

The inverters in the circuit below have minimum-sized transistors and the widths of the pass transistors are shown in the figure. Assume that the diffusion capacitance of a transistor is equal to its gate capacitance, and that a minimum sized transistor has gate and diffusion capacitance equal to C. In addition, $V_{dd} = 2V$, $V_{tn} = 0.3V$ and $|V_{tp}| = 0.4V$.

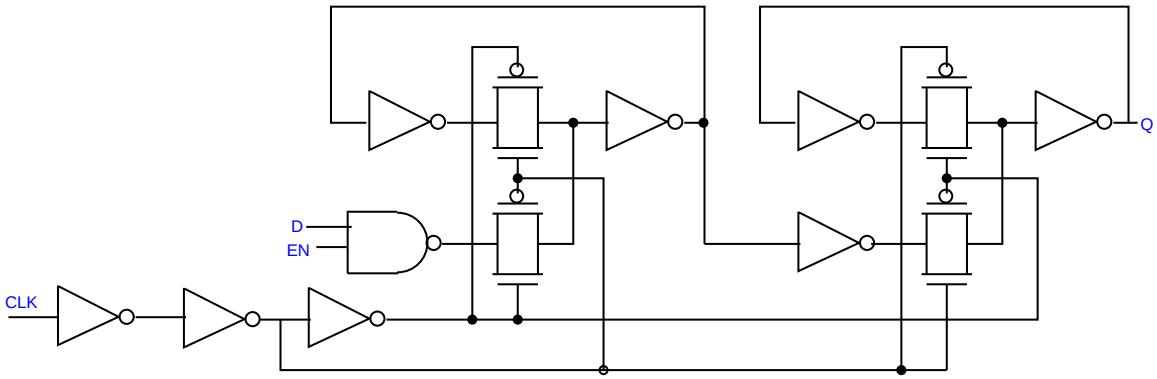


The sequence ABCD = (0011, 1001) is given as input to the circuit. Write down the voltage on node N just after the sequence is applied.

Voltage on Node N = ☐

2. (20 points)

The components of the flip-flop below have the following rise/fall delays (in picoseconds).
Nand gate: 150/200
Transmission gate: 150/150
Inverter: 125/125



What are the values of the following flip-flop parameters (which a designer needs to use to calculate the performance of a system)?

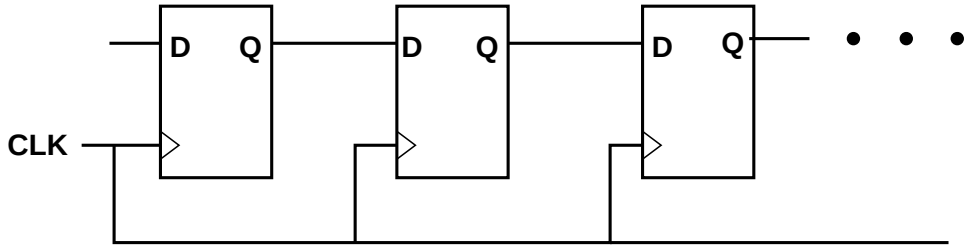
(a) Setup time = ____ **ps**

(b) Hold time = ____ **ps**

(c) Clock-to-Q delay = ____ **ps**

4. (20 points)

The flops used in the shift register below have a setup time of 100 ps, a maximum clock-Q delay of 150 ps, and a minimum clock-Q delay of 100 ps.



(a) How fast can this circuit be clocked?

Clock frequency = ☐ **MHz**

(b) What is the limit on the hold time of the flops at this frequency?

Hold time < ☐ **ps**

(c) What is the limit on the hold time of the flops at a frequency of 1 GHz?

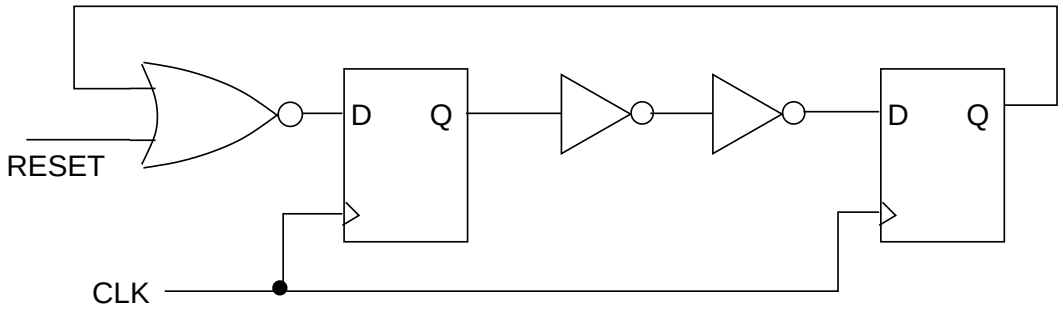
Hold time < ☐ **ps**

(d) What is the limit on the hold time of the flops if the circuit is clocked at a frequency of 100 MHz?

Hold time < ☐ **ps**

3. (20 points)

(a) What is the highest frequency at which the following circuit can be operated correctly? The parameters of the components are as follows.
Inverter: $t_{pd} = 200ps$**,** $t_{cd} = 100ps$
2-input NOR: $t_{pd} = 200ps$**,** $t_{cd} = 150ps$
D-flop: $t_{pd} = 200ps$ $t_{cd} = 0ps$**, Setup time = 300 ps, Hold time = 100 ps.**



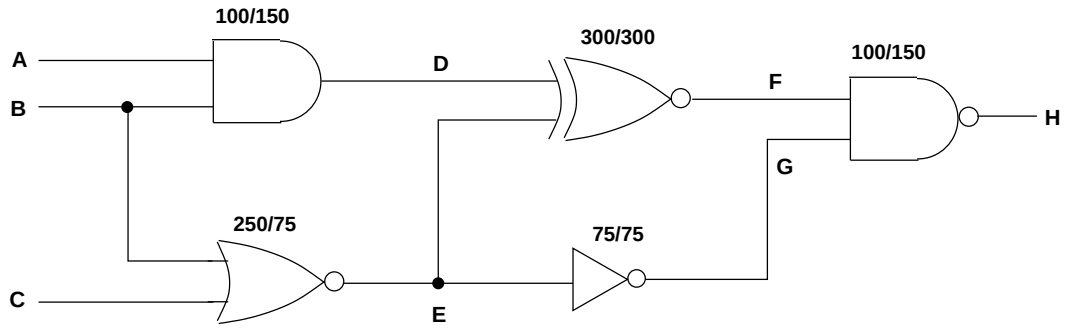
Maximum Clock frequency = ☐ **MHz**

(b) If the two inverters are removed (the Q of the first flop is connected to the D of the second), what will be the highest frequency at which the circuit can be operated. Explain your answer.

Maximum Clock frequency = ☐ **MHz**

5. (20 points)

(a) Write down all the paths from input B to the output and the worst-case and lowest delays for each path in the circuit below. The rise and fall times (in picoseconds) for each gate are shown over the gate symbol as risetime/falltime.



For example, the paths from input A to the output, and the delays are:

Path	Worst-case delay	Lowest delay
ADFH	600 ps	500 ps

(b) Give the test sequences for the following cases:

(i) Rising input on B, path BDFH

(i) Falling input on B, path BEFH

(ii) Rising input on B, path BEFH

VLSI Design **J. Abraham**

Fall 2006 **EXAM. I** **October 16, 2006**

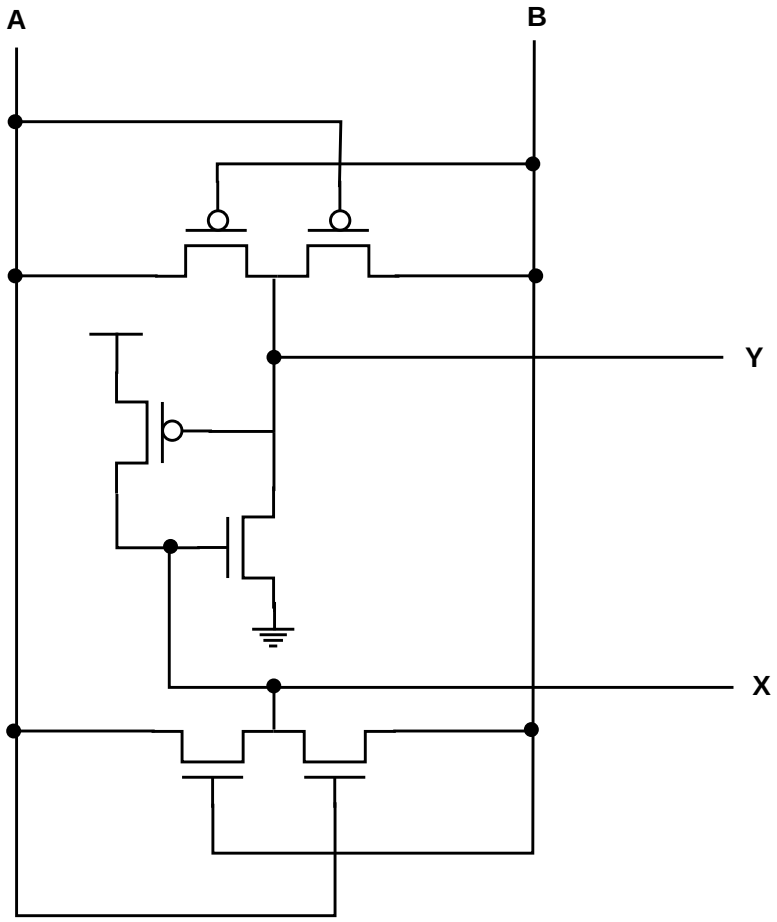
Name: Student, no. 4

- **Open Book, Open Notes.**
- **Time Limit: 75 minutes (pace yourself).**
- **Check for 6 pages in exam.**
- **Write all your answers in the spaces/boxes provided.**
- **Show any calculations in these pages using the back of the pages if needed.**
- **State clearly any assumptions made.**

PROBLEM	MAX	POINTS
1	20	
2	20	
3	20	
4	20	
5	20	
TOTAL	100	

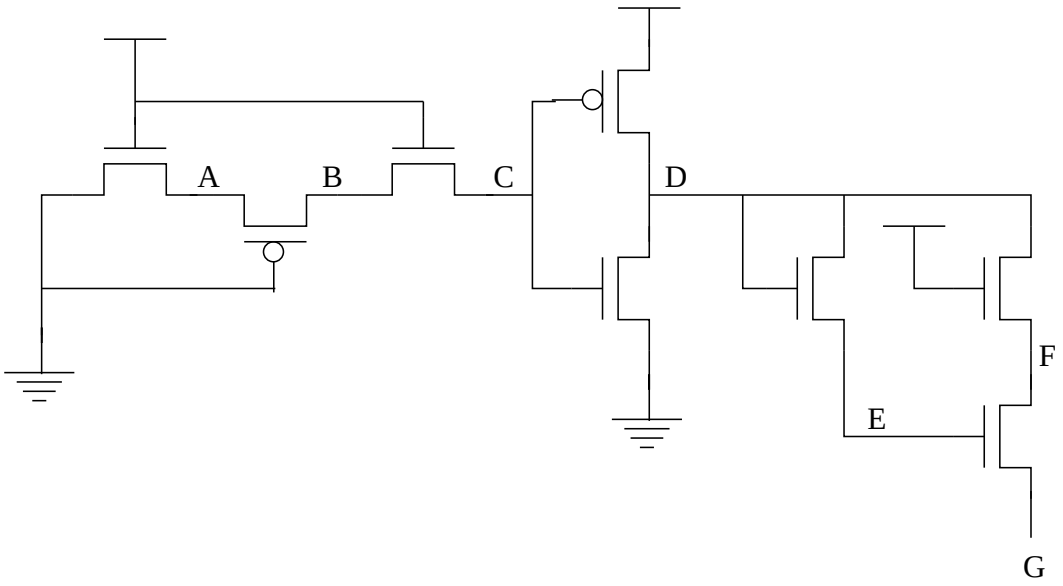
1. (20 points)

Find the functions X and Y implemented by the following circuit and check the appropriate boxes.



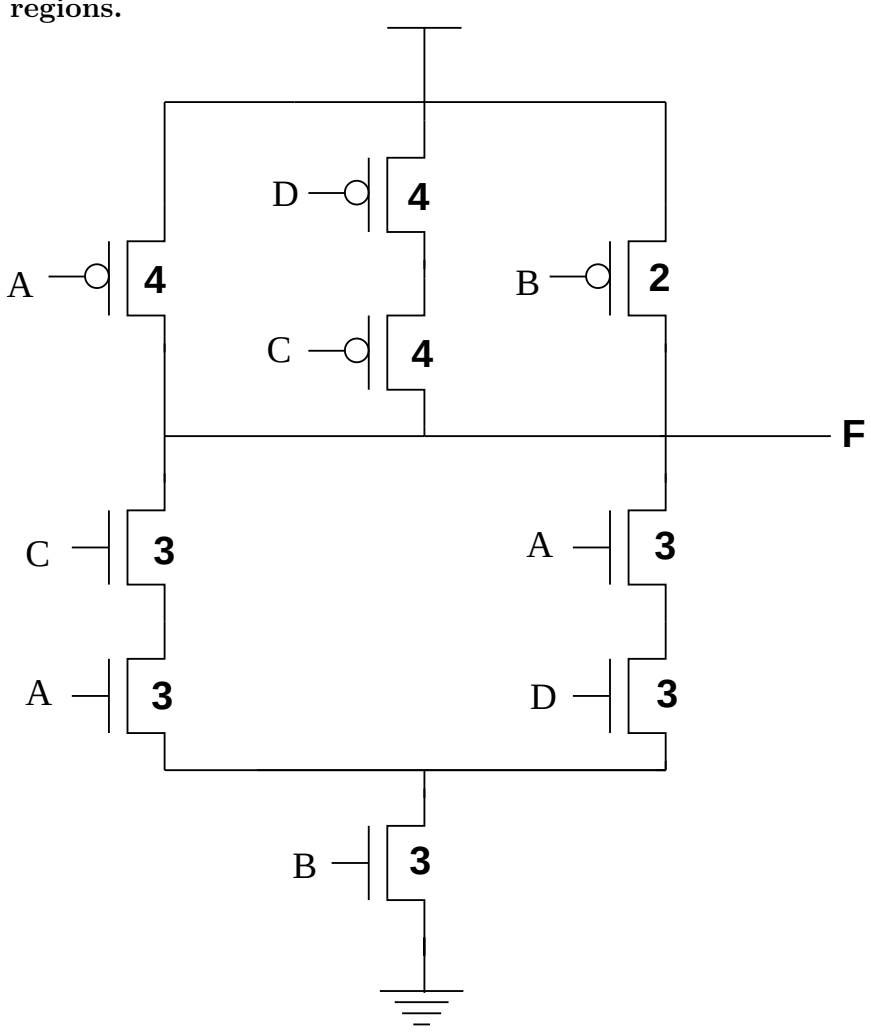
2. (20 points)

Write down the voltages at A, B, C, D, E, F, G in the following circuits, assuming that the initial voltage on each node is 1.0 volts. The relevant transistor parameters are, $V_{dd} = 2V$, $V_{tn} = 0.4V$ and $|V_{tp}| = 0.6V$.



3. (20 points)

Use the Elmore delay approximation to find the *worst-case* rise and fall delays at output F for the following circuit. The gate sizes of the transistors are shown in the figure. Use the assumption that the diffusion capacitance is equal to the gate capacitance and that a minimum sized transistor has gate and diffusion capacitance equal to C. The resistance of a nMOS transistor with unit width is R and the resistance of a pMOS transistor with width of 2 is also R. Also assume NO sharing of diffusion regions.



Input for worst-case rise delay (ABCD) =

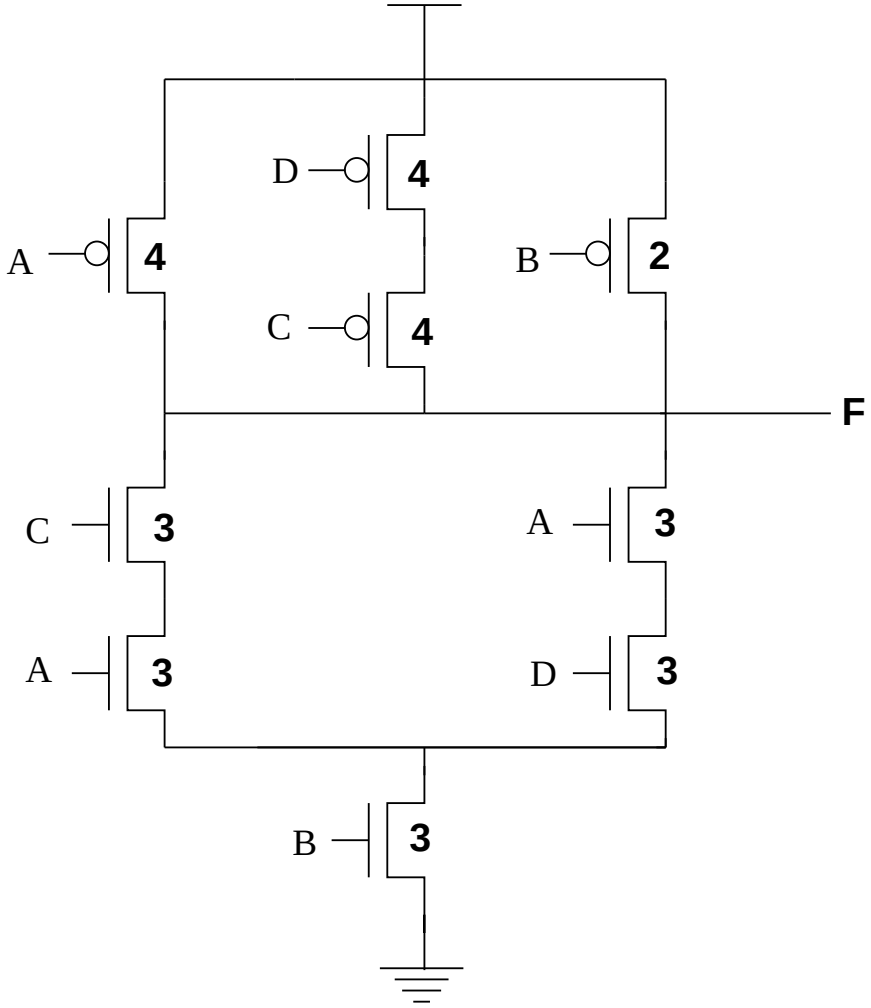
Worst-case rise delay =

Input for worst-case fall delay (ABCD) =

Worst-case fall delay =

4. (20 points)

Find the logical efforts for the inputs, A, B, C, and D in the circuit below.



Logical effort of A = ____

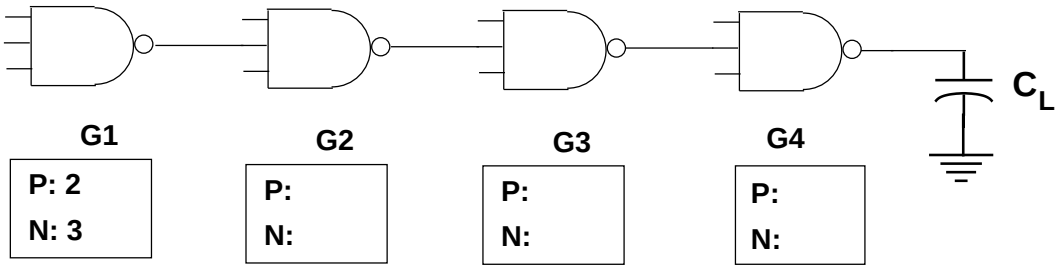
Logical effort of B = ____

Logical effort of C = ____

Logical effort of D = ____

5. (20 points)

(a) Find the sizes of the P and N transistors in the gates below if the output capacitance C_L is 1043 units.



(b) If a chain of n inverters, starting with a 2:1 inverter, is driving a load of $3C_L$, what is the input capacitance at each stage for the least delay?

(c) Would the input capacitance in (b) depend on the type of gate being used in each stage? Explain.

VLSI Design — **J. Abraham**

Fall 2006 — **EXAM. II** — **November 20, 2006**

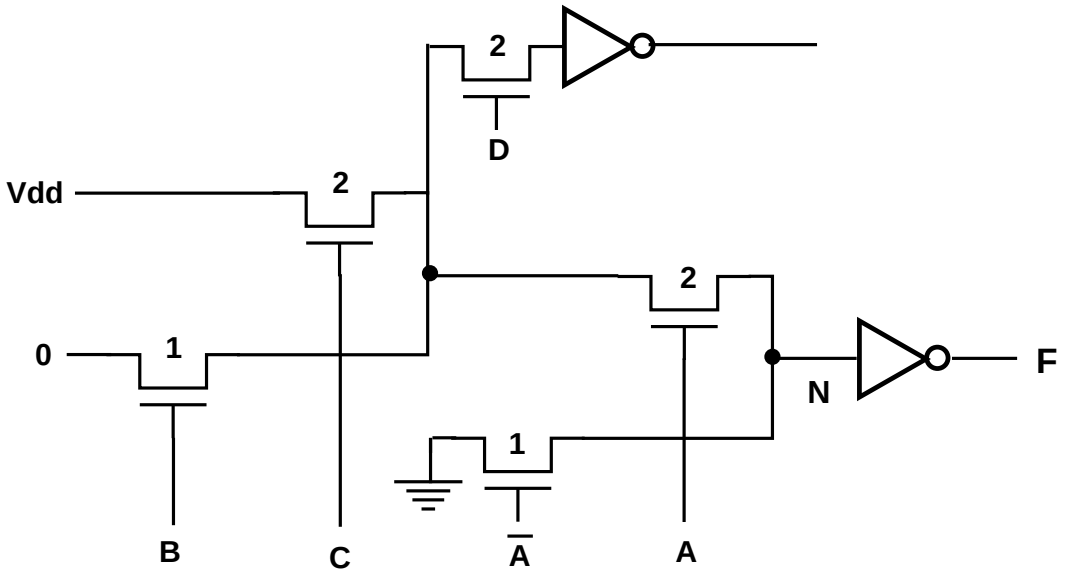
Name: Exam, No. 3

- **Open Book, Open Notes.**
- **Time Limit: 75 minutes (pace yourself).**
- **Check for 6 pages in exam.**
- **Write all your answers in the spaces/boxes provided.**
- **Show any calculations in these pages using the back of the pages if needed.**
- **State clearly any assumptions made.**

---

1. (20 points)

The inverters in the circuit below have minimum-sized transistors and the widths of the pass transistors are shown in the figure. Assume that the diffusion capacitance of a transistor is equal to its gate capacitance, and that a minimum sized transistor has gate and diffusion capacitance equal to C. In addition, $V_{dd} = 2V$, $V_{tn} = 0.3V$ and $|V_{tp}| = 0.4V$.

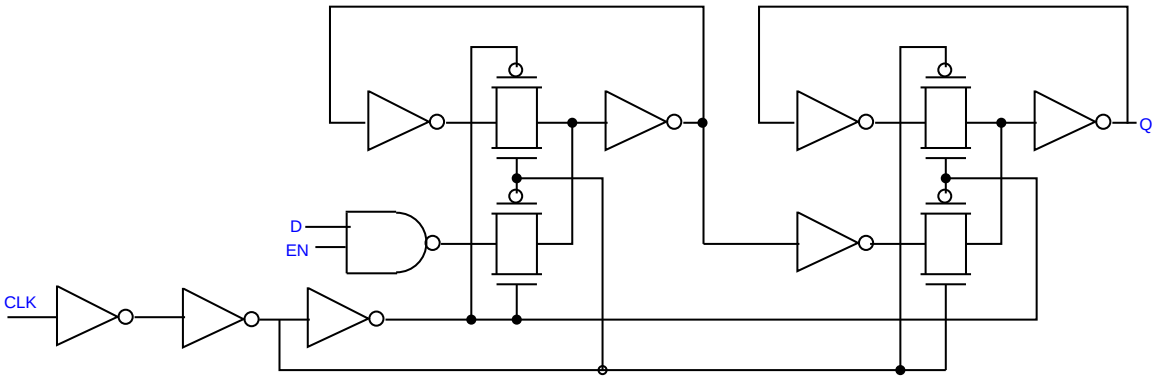


The sequence ABCD = (0011, 1001) is given as input to the circuit. Write down the voltage on node N just after the sequence is applied.

Voltage on Node N = ☐

2. (20 points)

The components of the flip-flop below have the following rise/fall delays (in picoseconds).
Nand gate: 125/175
Transmission gate: 125/125
Inverter: 100/100



What are the values of the following flip-flop parameters (which a designer needs to use to calculate the performance of a system)?

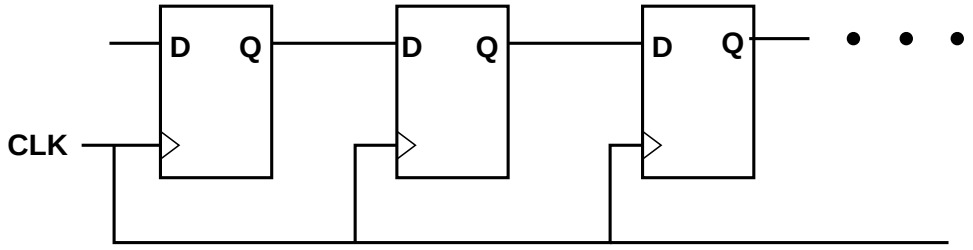
(a) Setup time = ____ **ps**

(b) Hold time = ____ **ps**

(c) Clock-to-Q delay = ____ **ps**

4. (20 points)

The flops used in the shift register below have a setup time of 100 ps, a maximum clock-Q delay of 150 ps, and a minimum clock-Q delay of 100 ps.



(a) How fast can this circuit be clocked?

Clock frequency = ☐ **MHz**

(b) What is the limit on the hold time of the flops at this frequency?

Hold time < ☐ **ps**

(c) What is the limit on the hold time of the flops at a frequency of 1 GHz?

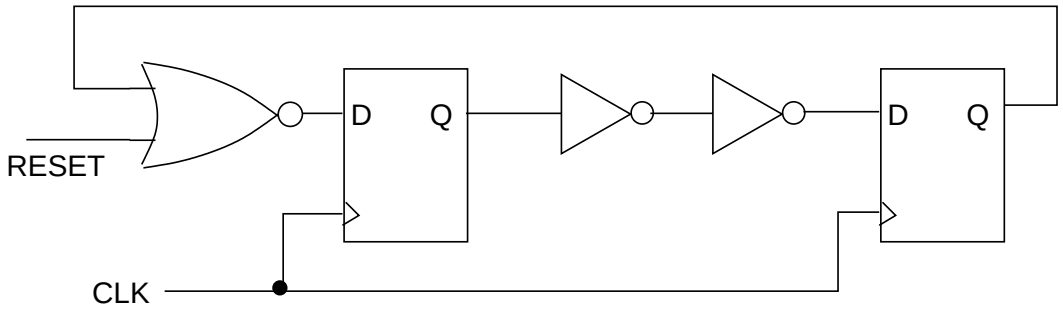
Hold time < ☐ **ps**

(d) What is the limit on the hold time of the flops if the circuit is clocked at a frequency of 100 MHz?

Hold time < ☐ **ps**

3. (20 points)

(a) What is the highest frequency at which the following circuit can be operated correctly? The parameters of the components are as follows.
Inverter: $t_{pd} = 200ps$**,** $t_{cd} = 100ps$
2-input NOR: $t_{pd} = 200ps$**,** $t_{cd} = 150ps$
D-flop: $t_{pd} = 200ps$ $t_{cd} = 0ps$**, Setup time = 300 ps, Hold time = 100 ps.**



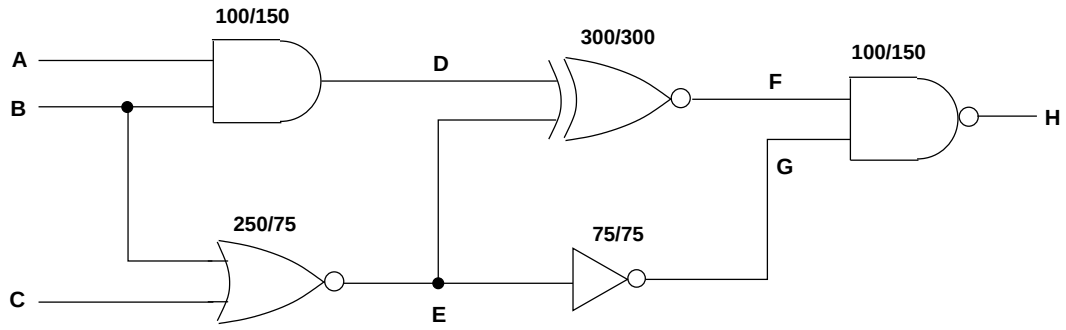
Maximum Clock frequency = ☐ **MHz**

(b) If the two inverters are removed (the Q of the first flop is connected to the D of the second), what will be the highest frequency at which the circuit can be operated. Explain your answer.

Maximum Clock frequency = ☐ **MHz**

5. (20 points)

(a) Write down all the paths from input B to the output and the worst-case and lowest delays for each path in the circuit below. The rise and fall times (in picoseconds) for each gate are shown over the gate symbol as risetime/falltime.



For example, the paths from input A to the output, and the delays are:

Path	Worst-case delay	Lowest delay
ADFH	600 ps	500 ps

(b) Give the test sequences for the following cases:

(i) Rising input on B, path BDFH

(i) Falling input on B, path BEFH

(ii) Rising input on B, path BEFH

EE360R/EE382M	**Introduction to VLSI Design**	**J. A. Abraham, R. S. Tupuri**
Fall 2001	**Exam. I**	**October 4, 2001**

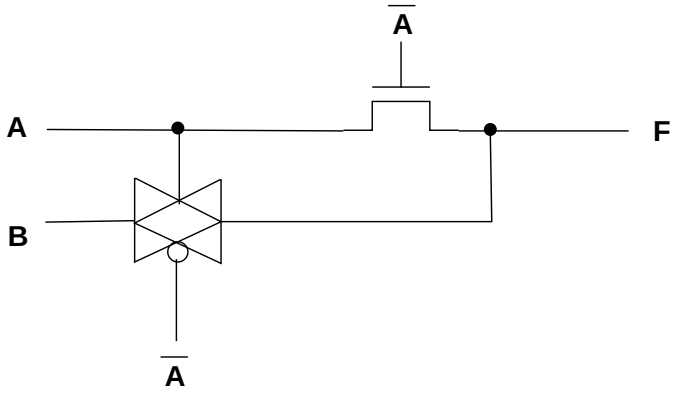
Name: _____

Open Book, Open Notes. Time Limit: 1 hour, 15 minutes (pace yourself). Check for 5 pages in exam.

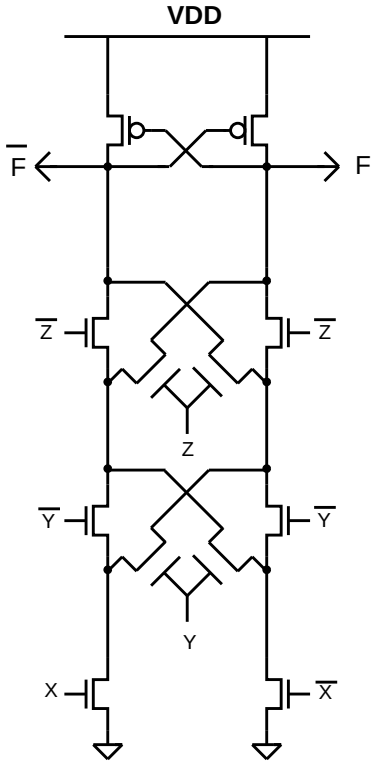
Write your work and all your answers in these pages. Use the back of the pages for scratch work if needed. State clearly any assumptions made.

1. (20 points) Write down the functions, F and G, implemented by the circuits below.

(a)



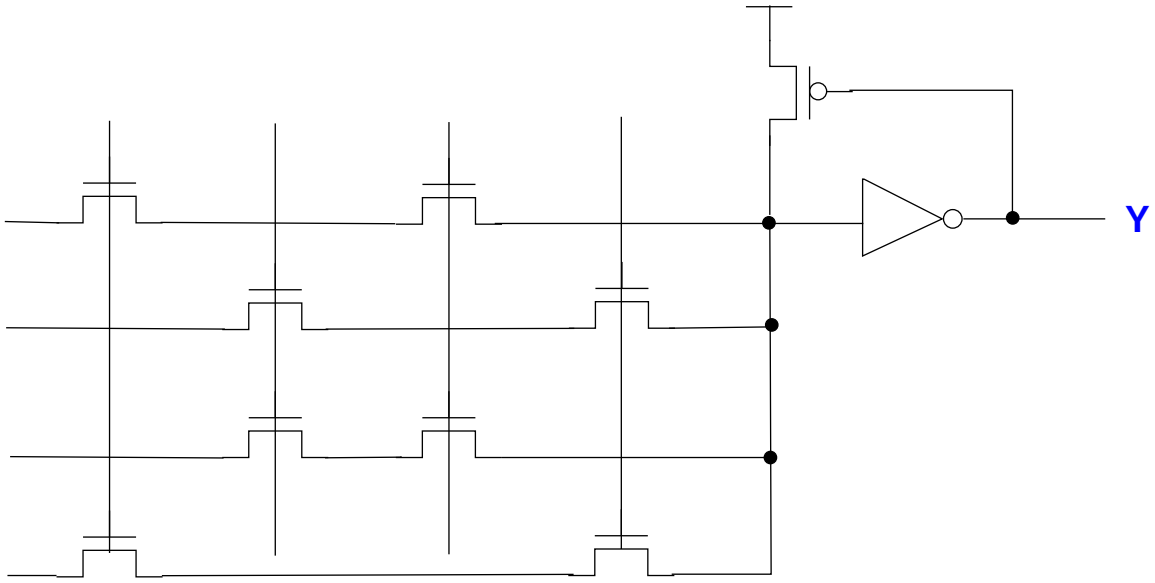
(b)



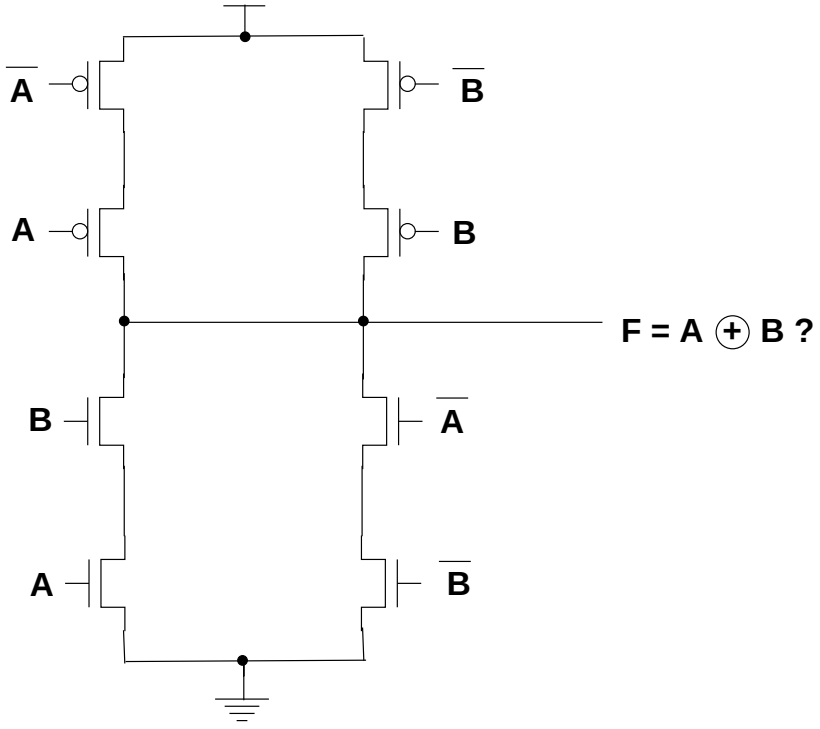
2. (20 points)

(a) The following circuit is supposed to implement the function
$Y = abc + \overline{a}\overline{b}c + \overline{a}b\overline{c} + a\overline{b}\overline{c}$

Label the inputs in the figure below so that the circuit correctly implements the function.

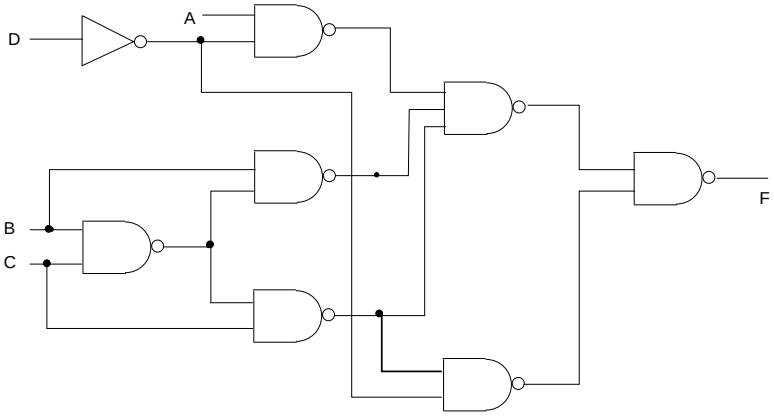


(b) The CMOS network below was supposed to implement the function $F = A \oplus B$. Point out the mistake in the design, and correct it **without increasing the delay**.



3. (20 points)

A circuit and the parameters of its library cells are given below.



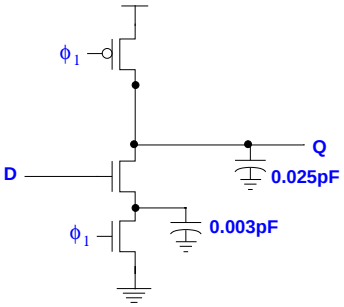
Gate	Fanout	Rise Delay	Fall Delay
Inverter	1	100	80
Inverter	2	120	100
Inverter	3	160	130
Nand	1	140	140
Nand	2	150	160
Nand	3	160	180
Nor	1	220	180
Nor	2	240	200
Nor	3	280	230

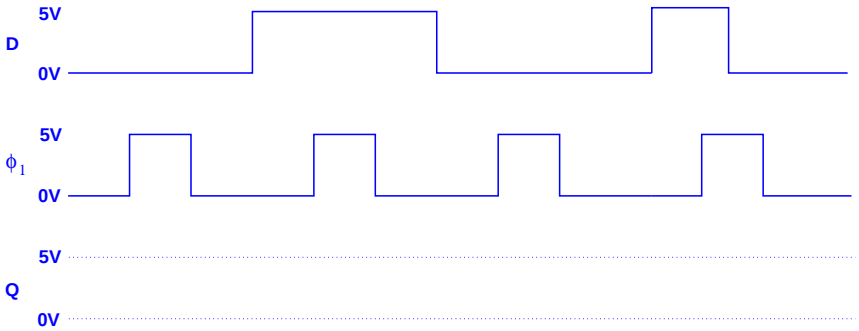
Find the longest **functional paths** from inputs B and D to F. Write down the logic values on in inputs which will propagate a transition through the longest paths, and give the rise and fall delays for the paths.

4. (20 points)

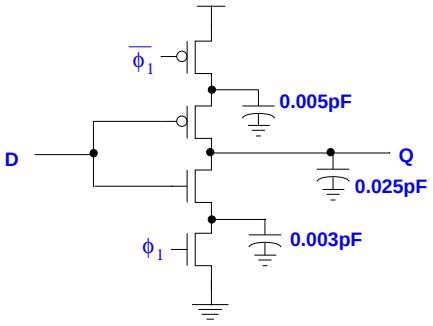
Draw the waveform at the output Q in the circuit below, in response to the input and clock waveform shown. Indicate the approximate value of the voltage at the transitions of ϕ_1 whenever it changes significantly. The TOTAL capacitance at the nodes, including drain and parasitic capacitances, is indicated in the figures.

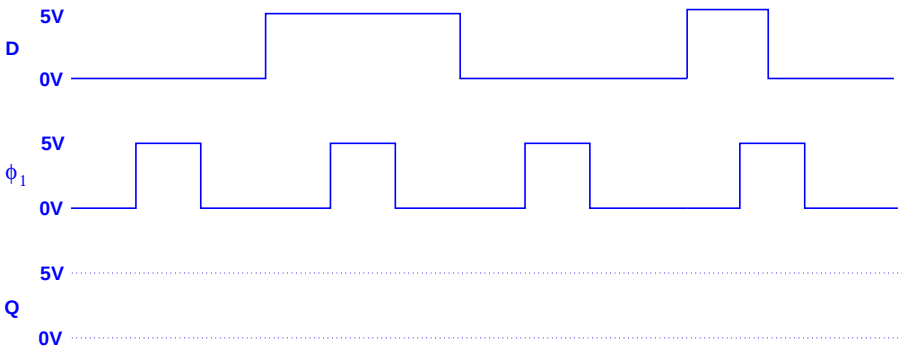
(a)





(b) Assume an initial value of 0V on Q.



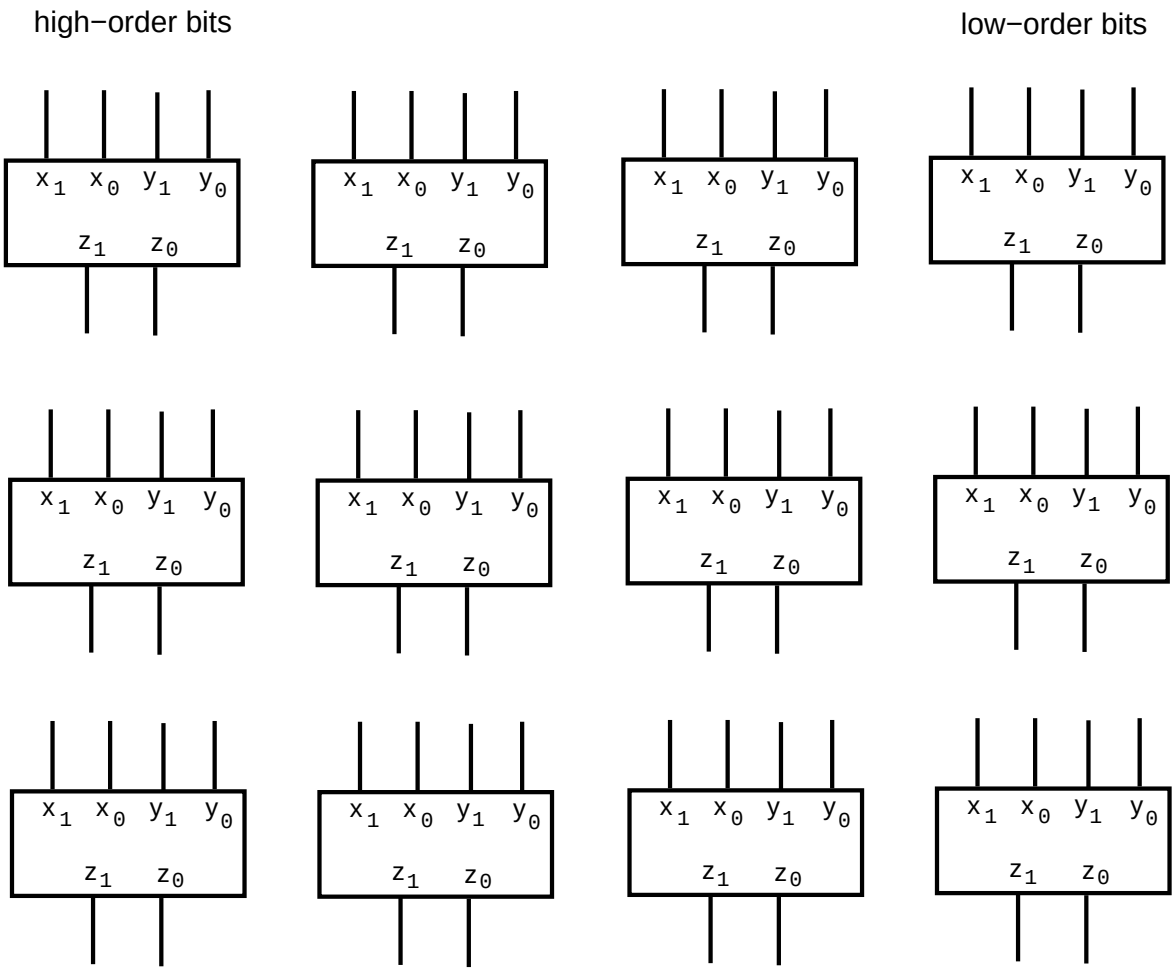


5. (20 points)

A 2-bit comparator cell which takes inputs $X = x_1x_0$ and $Y = y_1y_0$, and produces a 2-bit result Z can be specified as follows:

X > Y, Z = 10
X < Y, Z = 01
X = Y, Z = 00 or 11.

If each cell has some fixed delay, show how the cells may be interconnected to compare two 8-bit numbers with three cell delays (**you should use ONLY the cells, and do not need to use all of them**).



EE82M	**VLSI I**	**J. Abraham**
Fall 2002	**EXAM. I**	**October 14, 2002**

Name: EXAM, No. 1

Open Book, Open Notes. Time Limit: 50 minutes (pace yourself). Check for 6 pages in exam.

Write all your answers in the spaces/boxes provided.

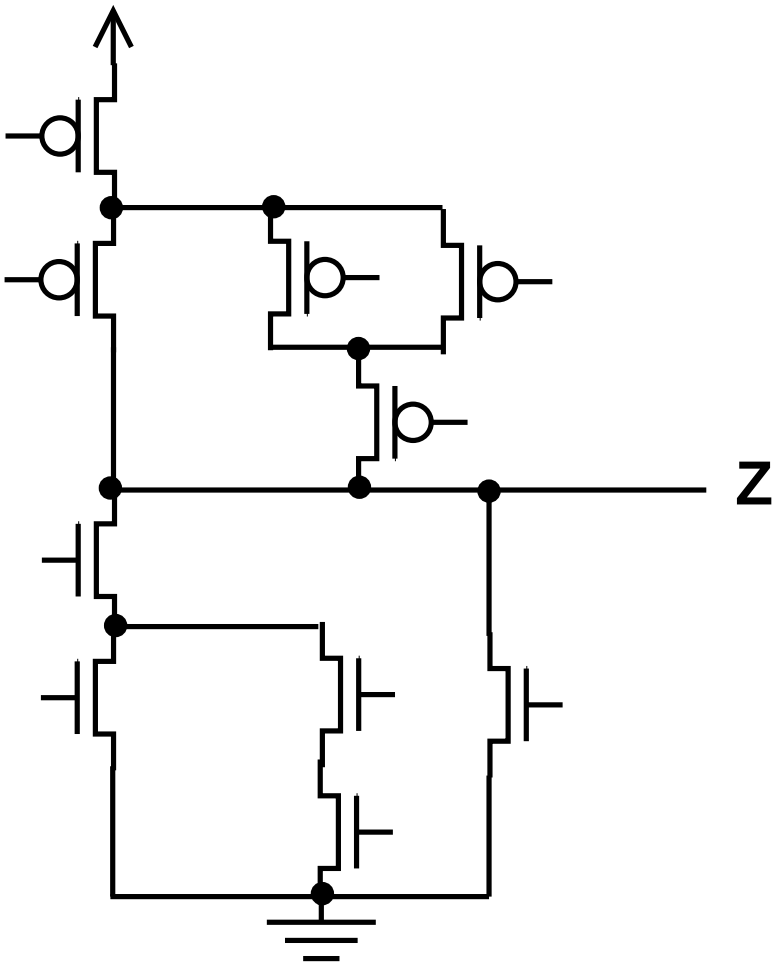
Show any calculations in these pages using the back of the pages if needed. State clearly any assumptions made.

PROBLEM	MAX	POINTS
1	15	
2	20	
3	20	
4	20	
5	25	
TOTAL	100	

1. (15 points)

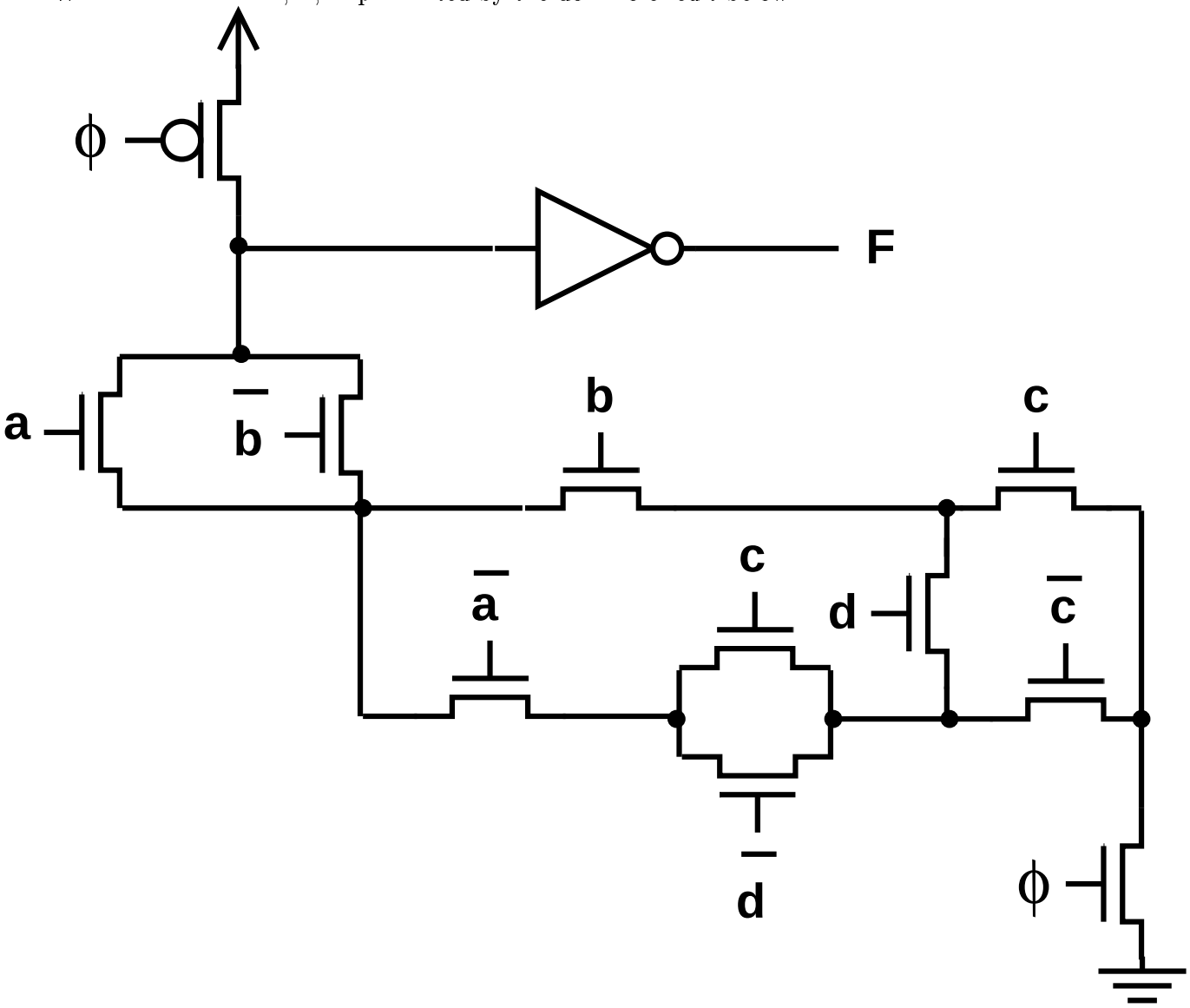
Label the inputs of the static CMOS circuit below so that it implements the following function:

$$Z = \overline{ac + a\bar{c}bd + f + aef}$$



2. (20 points)

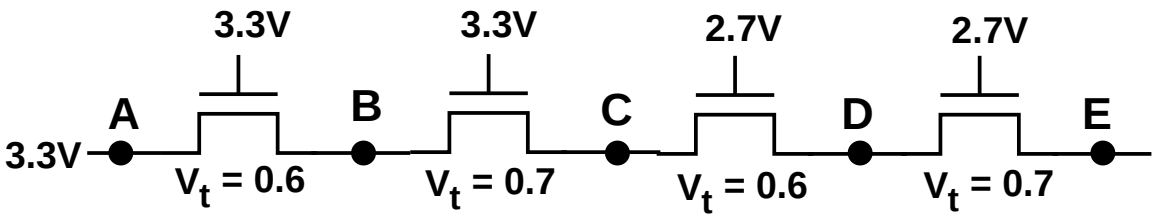
What is the function, F, implemented by the domino circuit below?



- ☐ $F = a\ b\ (c + d) + \overline{a}\ \overline{b}\ \overline{(c \oplus d)}$
- ☐ $F = b\ (c + d) + \overline{a}\ \overline{(c \oplus d)}$
- ☐ $F = b\ c\ (a + d) + \overline{b}\ \overline{c}\ \overline{(a \oplus d)}$
- ☐ $F = b\ (a + d) + \overline{c}\ \overline{(a \oplus d)}$
- ☐ $F = a\ d\ (b + c) + \overline{a}\ \overline{d}\ \overline{(b \oplus c)}$

3. (20 points)

Write down the voltages at the nodes B, C, D and E in the circuit below, given the voltages at A and the gate inputs of the transistors. Each transistor is labeled with its V_t value.



Voltage at B = ☐

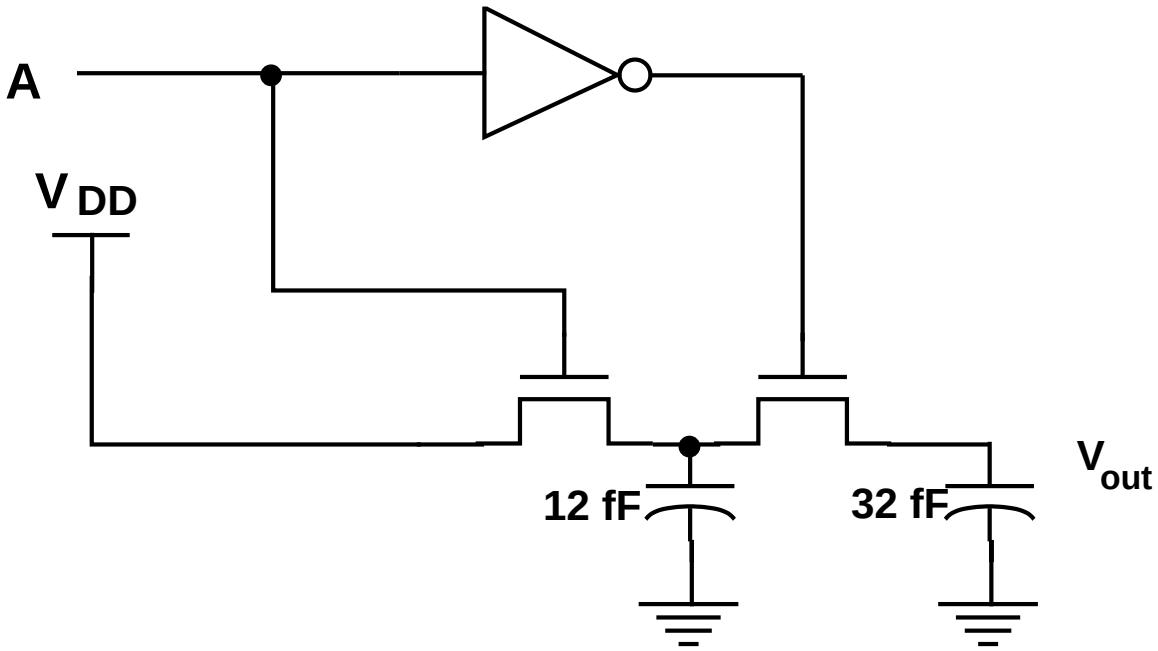
Voltage at C = ☐

Voltage at D = ☐

Voltage at E = ☐

4. (20 points)

In the circuit below, V_{DD} is 3 Volts, and V_{tn} is 0.25 Volts.



Initially, $V_{out} = 0$, and A is logic 1 (at V_{DD}).

Find the value of V_{out} after A becomes logic 0.

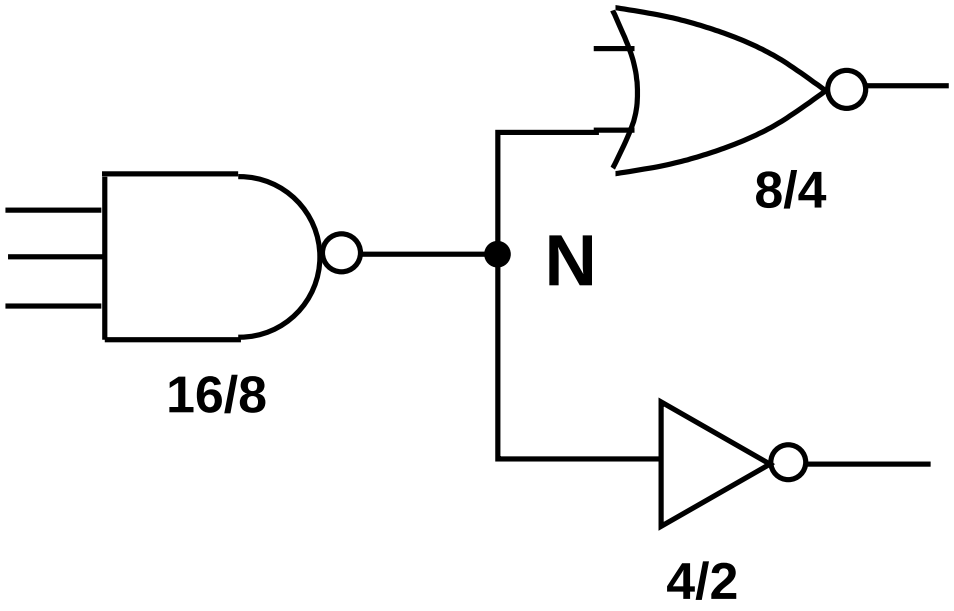
$V_{out} =$ ☐

5. (25 points)

Find the capacitance (gate and diffusion) at the node N in the circuit below, implemented in static CMOS technology, in terms of *unit squares of gate capacitance*.

Each transistor in the circuit has minimum length (of 1 unit), and each gate is labeled with the widths of the P and N transistors (P width/N width), in units of the minimum length. (For example, a gate labeled 16/8 would have P-channel transistors with a width of 16 units and the N-channel transistors would have a width of 8 units.)

Each diffusion area extends 2 units from the polysilicon. The diffusion capacitance has the following characteristics:
Area: 1 square of diffusion = 0.25 unit gate capacitance
Periphery: 1 unit of diffusion = 0.1 unit gate capacitance.



Gate capacitance portion: ____ squares.

Diffusion capacitance portion: ____ squares.

EE382M	**VLSI I**	**J. Abraham**
Fall 2003	**EXAM. I**	**October 7, 2003**

Name: STUDENT1, GRAD1

Open Book, Open Notes. Time Limit: 75 minutes (pace yourself). Check for 7 pages in exam.

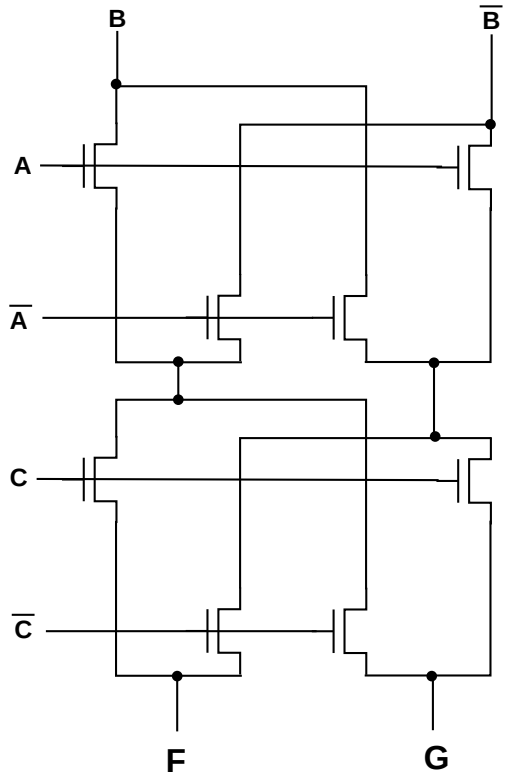
Write all your answers in the spaces/boxes provided.

Show any calculations in these pages using the back of the pages if needed. State clearly any assumptions made.

PROBLEM	MAX	POINTS
1	15	
2	15	
3	15	
4	20	
5	20	
6	15	
TOTAL	100	

1. (15 points)

Find the functions F and G implemented by the following circuit and check the appropriate boxes.



☐ $F = \overline{A}\ \overline{B}\ C + A\ \overline{B}\ \overline{C} + \overline{A}\ B\ \overline{C} + \overline{A}\ \overline{B}\ \overline{C}$

☐ $F = \overline{A}\ \overline{B}\ C + \overline{A}\ B\ \overline{C} + A\ \overline{B}\ \overline{C} + A\ B\ C$

☐ $F = \overline{A}\ \overline{B}\ \overline{C} + A\ \overline{B}\ C + \overline{A}\ B\ C + A\ B\ \overline{C}$

☐ $F = A\ B\ \overline{C} + \overline{A}\ B\ C + A\ \overline{B}\ C + A\ B\ C$

☐ $G = \overline{A}\ \overline{B}\ C + A\ \overline{B}\ \overline{C} + \overline{A}\ B\ \overline{C} + \overline{A}\ \overline{B}\ \overline{C}$

☐ $G = \overline{A}\ \overline{B}\ C + \overline{A}\ B\ \overline{C} + A\ \overline{B}\ \overline{C} + A\ B\ C$

☐ $G = \overline{A}\ \overline{B}\ \overline{C} + A\ \overline{B}\ C + \overline{A}\ B\ C + A\ B\ \overline{C}$

☐ $G = A\ B\ \overline{C} + \overline{A}\ B\ C + A\ \overline{B}\ C + A\ B\ C$

2. (15 points)

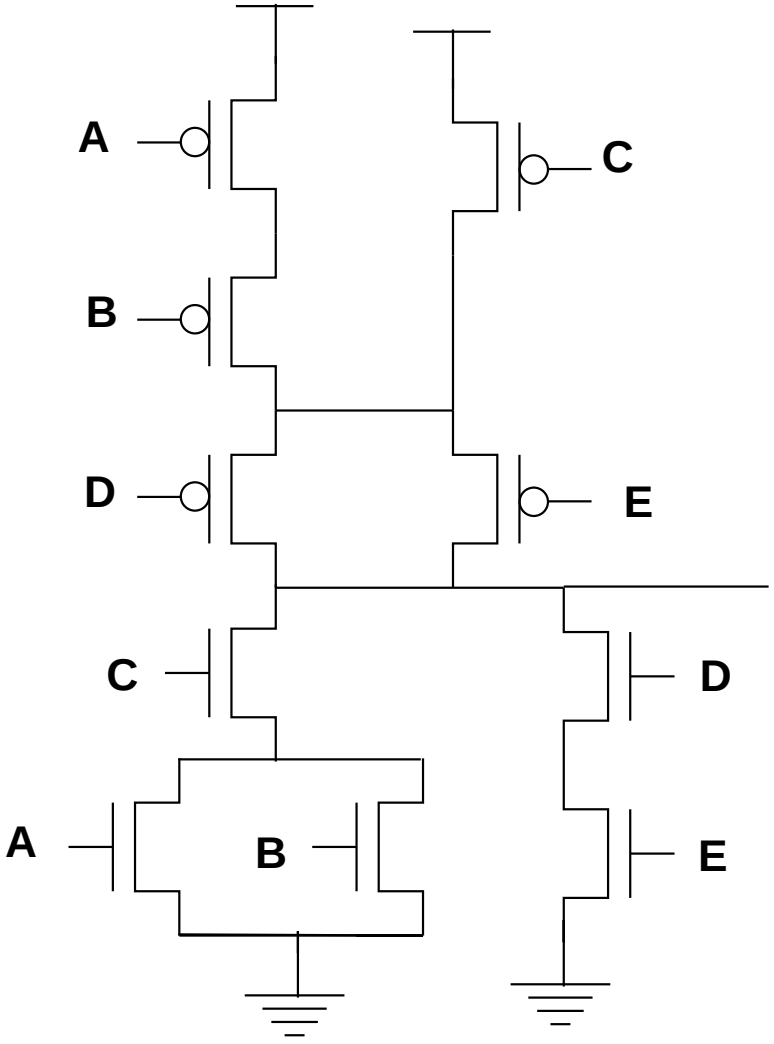
A design decision was made to change the V_T of the PMOS transistor in an inverter. The transistor has a threshold voltage of -0.4V with zero substrate bias, and its γ is -0.4. Find the substrate bias which will change the V_T to -0.50V. (Use $2\Phi_F = 0.6V$)

Substrate Bias = 

3. (15 points)

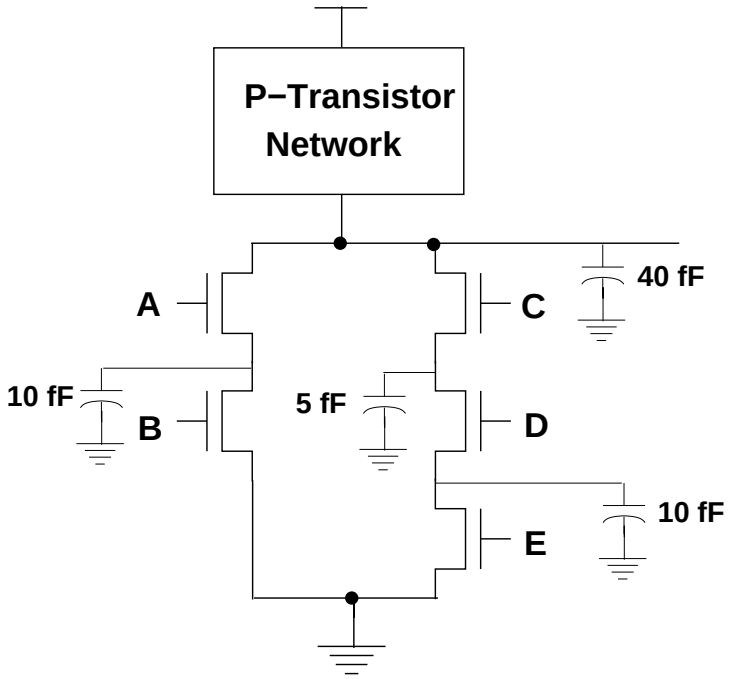
Size the following gate such that it has the same drive strength as inverter that has a PW=3 and NW=2.

(PW, NW are the widths of the PMOS and NMOS transistors, respectively.)



4. (20 points)

The n-channel transistors in the following portion of a CMOS circuit have an on-resistance of 5 $K\Omega$. The total source and drain (diffusion) capacitances of an n-channel transistor are 5 fF each. The parasitic (wiring, etc.) capacitances are shown lumped at the internal nodes. The output load capacitance includes the diffusion capacitance of the P-Network, wiring capacitances, and the output load capacitances.



(a) Assume that all load and internal capacitances have been charged to V_{DD}. Which of the following input vectors will result in the longest t_{pHL}?

☐ ABCDE = 00111

☐ ABCDE = 10111

☐ ABCDE = 11000

☐ ABCDE = 11111

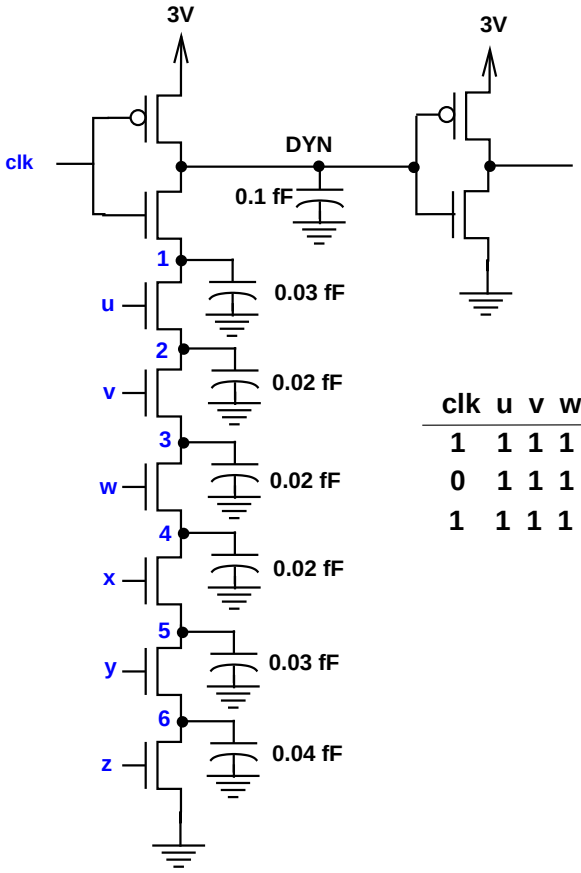
☐ ABCDE = 01111

(b) Assuming all the capacitors are initially charged to V_{DD}, use the Elmore delay approximation to find the value of t_{pHL} for the input vector ABCDE = 01111.

t_{pHL} = ☐

5. (20 points)

Calculate the voltages on the node **DYN** in the circuit below under the initial condition and input **sequence** shown.

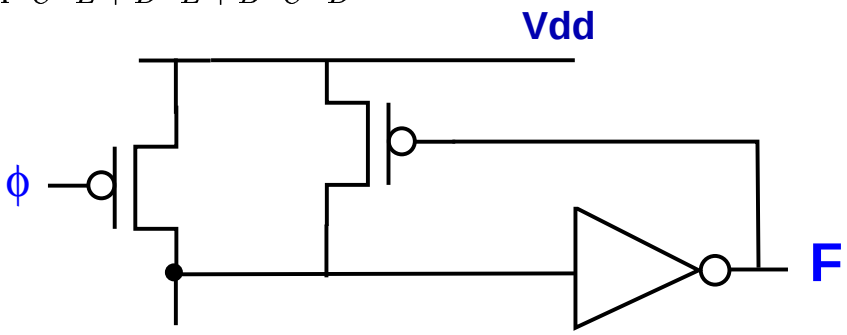


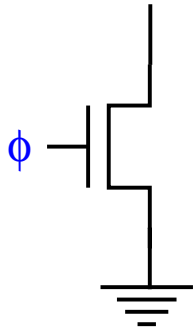
clk	u	v	w	x	y	z	DYN
1	1	1	1	1	1	1	0 Volts
0	1	1	1	1	1	1	
1	1	1	1	1	1	0	

6. (15 points)

The following drawing shows part of a domino CMOS design. Draw the NMOS network which will realize the following function F **using only 5 N-channel transistors**.

$F = A \cdot B + A \cdot C \cdot E + D \cdot E + B \cdot C \cdot D$





EE360R/EE382M **Introduction to VLSI Design** **J. A. Abraham, R. S. Tupuri**
Spring 2002 **Exam. I** **February 28, 2002**

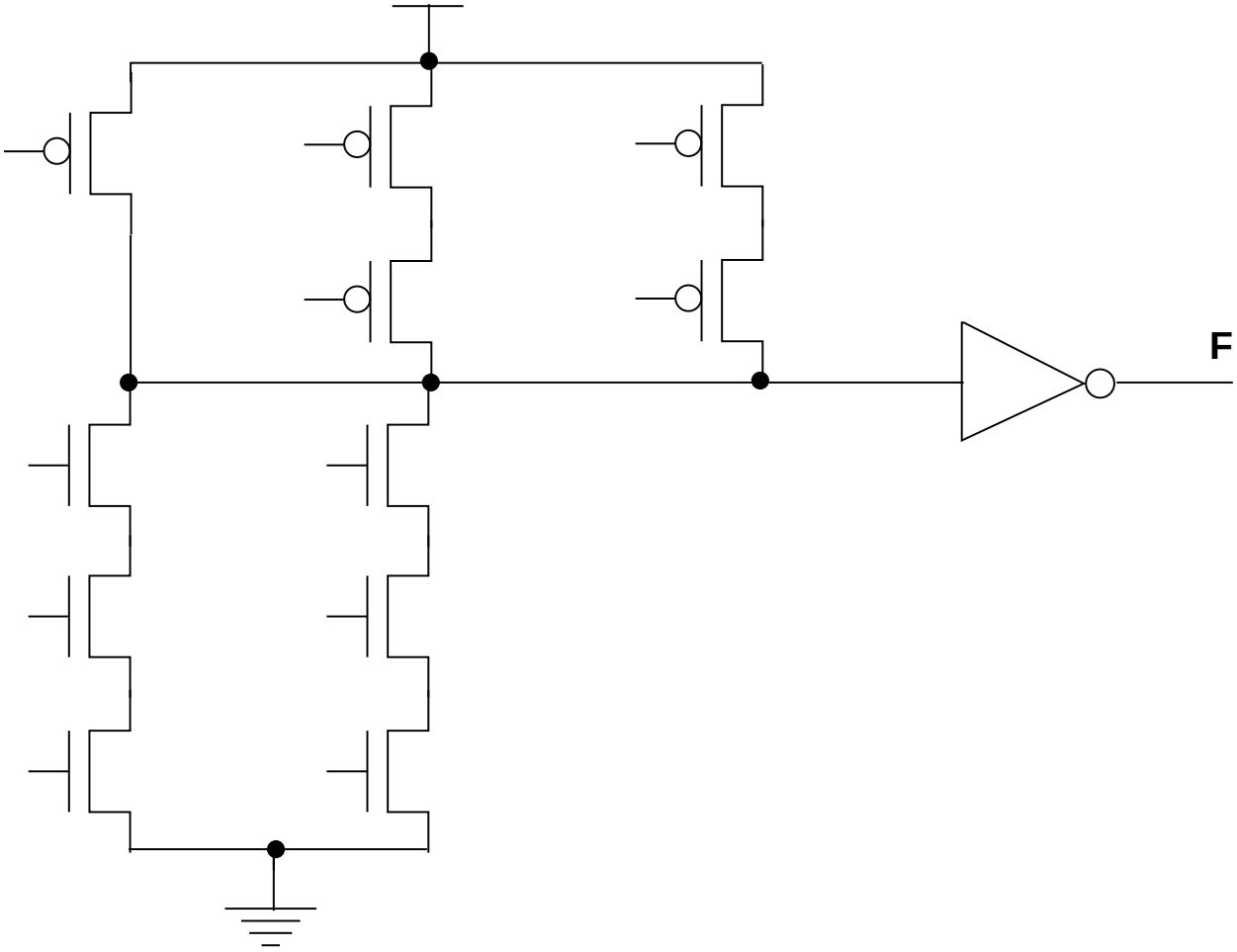
Name: _____

Open Book, Open Notes. Time Limit: 1 hour, 15 minutes (pace yourself). Check for 5 pages in exam.

Write your work and all your answers in these pages. Use the back of the pages for scratch work if needed. State clearly any assumptions made.

1. (20 points) Label the inputs of the circuit below so that it implements the function

$F = a \cdot (b \cdot c + \overline{b} \cdot \overline{c})$



2. (20 points)

Implement the following function, F, using static CMOS logic with the minimum number of transistors.

$F = \overline{(a + b + c) \cdot d \cdot (\overline{a \cdot b})}$

3. (20 points)

Implement the following functions using a single logic network with the minimum number of transistors.

$F_1 = a \cdot \overline{b} \cdot d$

$F_2 = a \cdot \overline{b} \cdot \overline{c} \cdot d + (\overline{a} + b + \overline{d}) \cdot c$

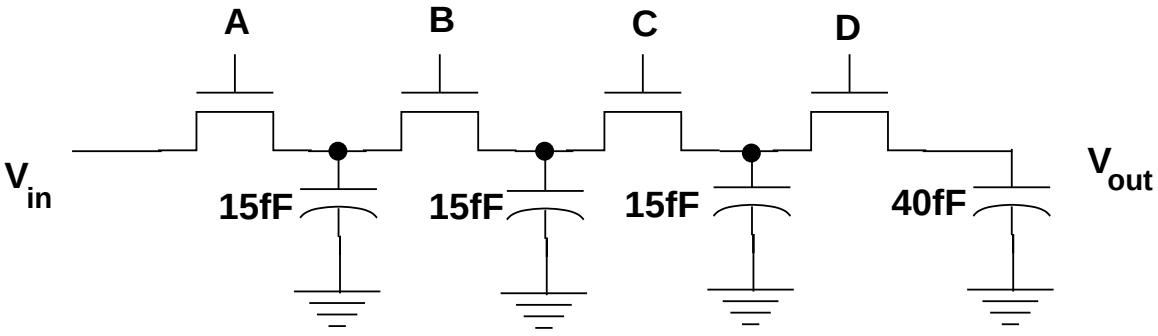
4. (20 points)

Four n-channel transistors in a pass transistor chain are shown below. The input voltage, V_{in} is set to 3 Volts, and V_{tn} is 0.25 Volts.

Initially, V_{out} is 0 Volts, and ABCD = 1110.

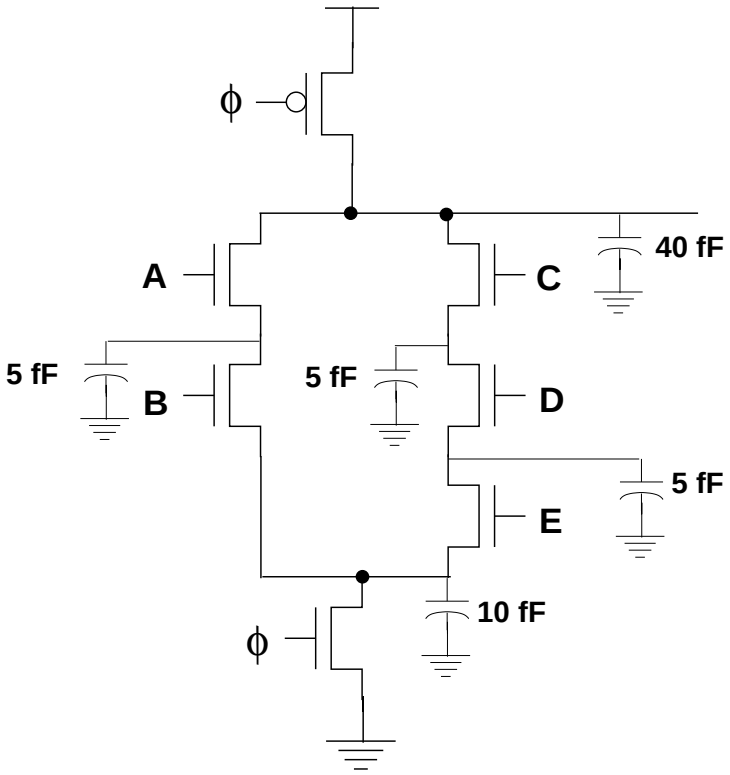
Then, the inputs are switched to ABCD = 0011.

Find the final value of V_{out}.



5. (20 points)

The n-channel transistors in the following portion of a domino circuit have an on-resistance of 5 $K\Omega$. The source/drain capacitance of an n-channel transistor is 5 fF, and that of the p-channel transistor is 10 fF. The parasitic and output load capacitances are shown lumped at the nodes.



(a) Identify the input combination for the the *worst-case* fall time, and estimate it using the Penfield-Rubenstein approach.

(b) What is the input combination for the *best-case* fall time, and it's estimated value?

Spring 2005 | **VLSI Design** | **J. Abraham**
EXAM. I | **March 2, 2005**

#005 **Class (382M/360R): _____**

Name: _____

Open Book, Open Notes. Time Limit: 75 minutes (pace yourself). Check for 7 pages in exam.

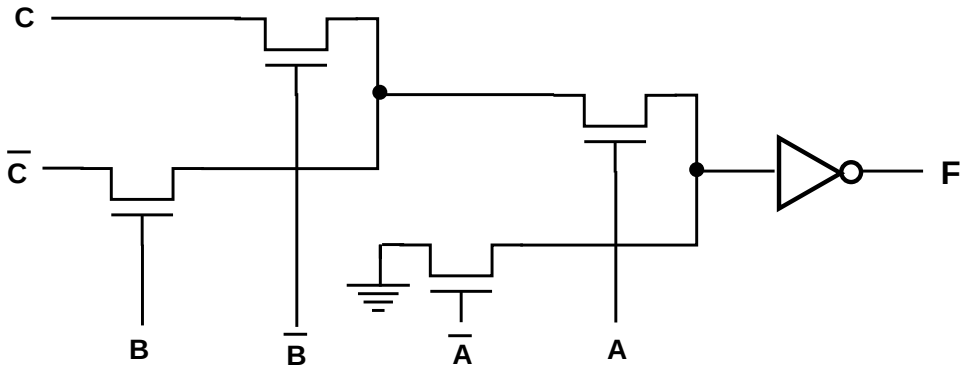
Write all your answers in the spaces/boxes provided.

Show any calculations in these pages using the back of the pages if needed. State clearly any assumptions made.

PROBLEM	MAX	POINTS
1	15	
2	15	
3	15	
4	20	
5	20	
TOTAL	100	

1. (15 points)

Find the function F implemented by the following circuit and check the appropriate box.



☐ $F = \overline{A} + \overline{B}\ C + B\ \overline{C}$

☐ $F = \overline{A} + B\ C + \overline{B}\ \overline{C}$

☐ $F = A + \overline{B}\ C + B\ \overline{C}$

☐ $F = \overline{B} + A\ C + \overline{A}\ \overline{C}$

☐ $F = B + A\ C + \overline{A}\ \overline{C}$

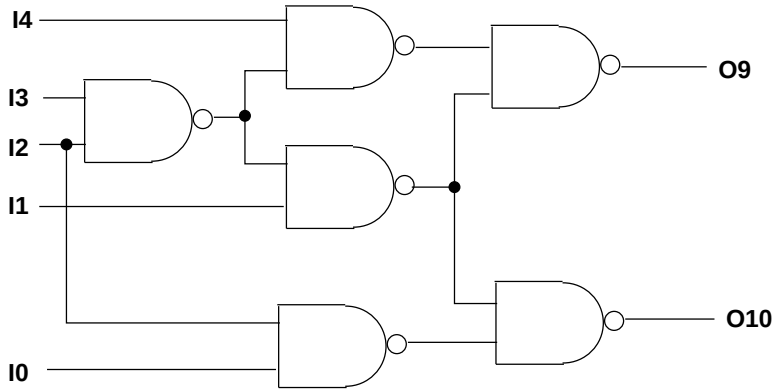
☐ $F = \overline{C} + A\ B + \overline{A}\ \overline{B}$

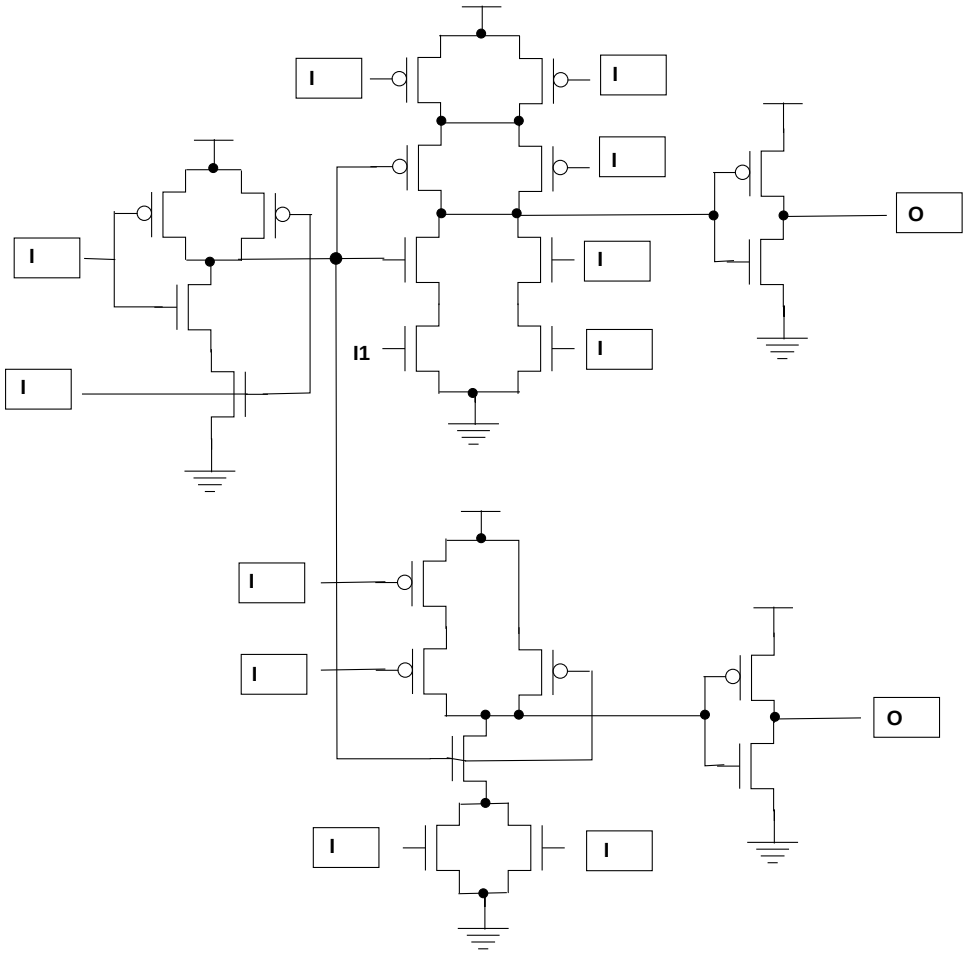
☐ $F = C + A\ B + \overline{A}\ \overline{B}$

☐ $F = A + B\ C + \overline{B}\ \overline{C}$

2. (20 points)

The gate level circuit below has been implemented with the transistor netlist at the bottom. Label the transistor gate inputs and the circuit outputs so that the gate level circuit is correctly implemented by the transistor circuit.





3. (25 points)

Calculate the ratio of *maximum delay* to *minimum delay* for NAND gates of various inputs, for the case where the gates are not driving any load and fill in the table below. Assume that the unit gate capacitance is the same as the unit diffusion capacitance, and that diffusion is shared in the nMOS stack, but NOT in the pMOS network.

Include all the capacitances seen on the output node.

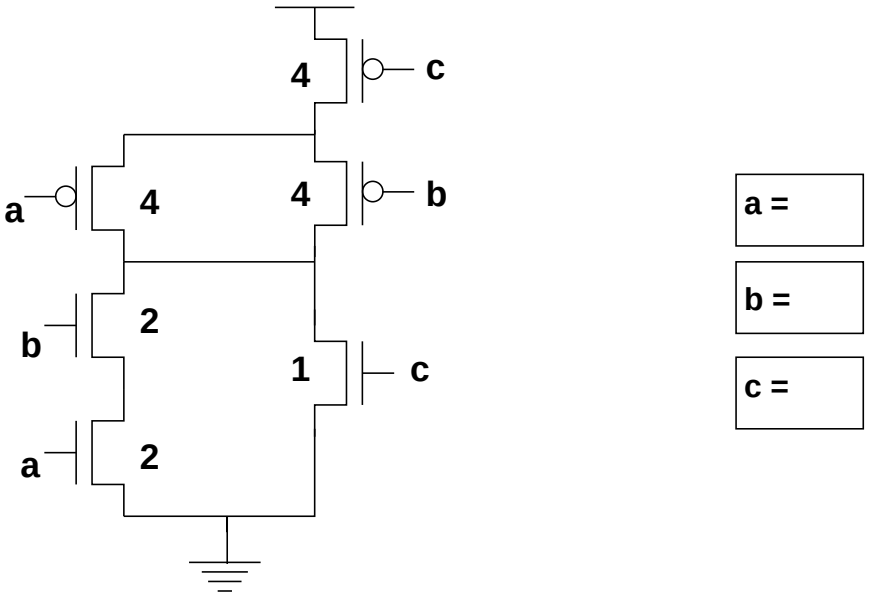
For the minimum delay for the output falling, assume that the latest arriving signal is connected closest to the output, and that the earlier signals have discharged their respective capacitors.

Perform the calculation for NAND gates which are sized so that the equivalent inverter is 2:1.

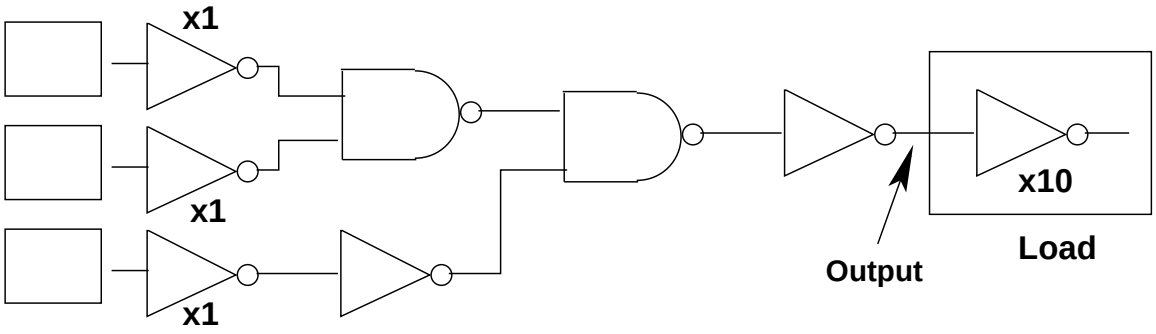
	2-input	3-input	4-input
Output $0 \rightarrow 1$			
Output $1 \rightarrow 0$			

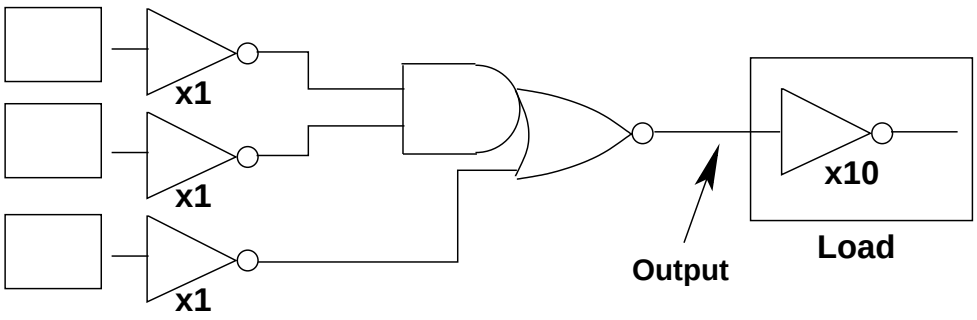
4. (20 points)

(a) Calculate the logical effort of the a, b and c inputs of the following AND-OR-INVERT (AOI) gate.



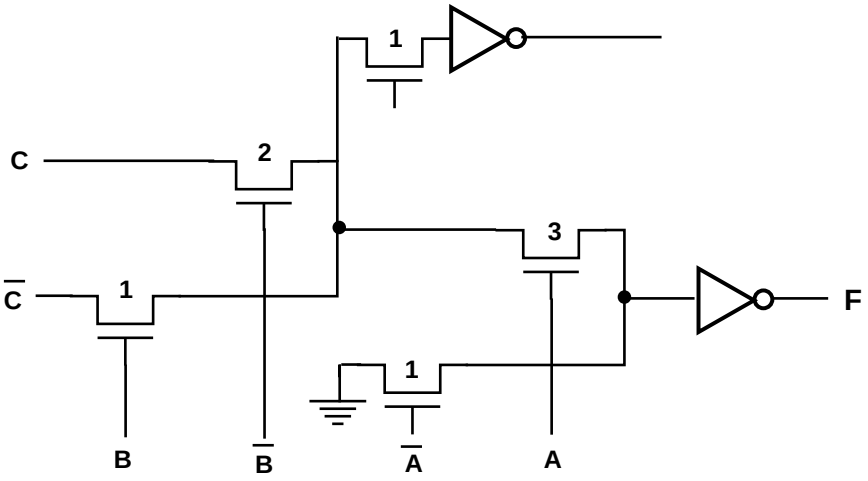
(b) Compute the delays of the following paths (from each input to output (before the load)) using logical effort. The load inverter is ten times bigger than the input inverters. The parasitic delay of the AOI gate is 3, that of a NAND gate is 2 and that of an inverter is 1. Show your work.





5. (20 points)

Calculate the Elmore delay from C to F in the circuit below. The widths of the pass transistors are shown, and the inverters have minimum-sized transistors. Assume that the diffusion capacitance of a transistor is equal to its gate capacitance, and that a minimum sized transistor has gate and diffusion capacitance equal to C.



Delay =

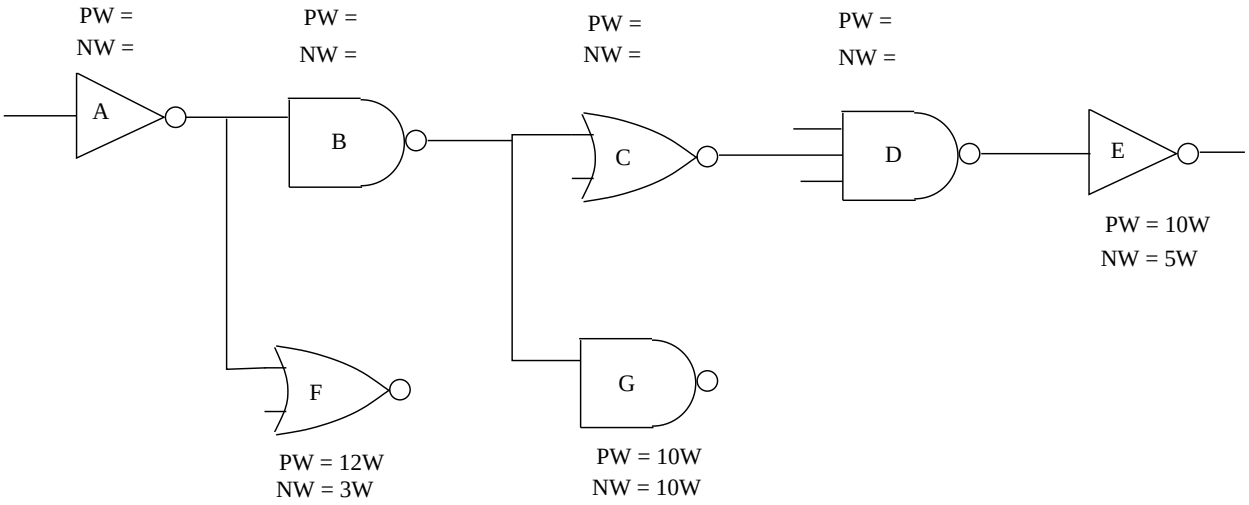
EE360R/EE382M **Introduction to VLSI Design** **J. A. Abraham, R. S. Tupuri**
Fall 2001 **Exam. II** **November 8, 2001**

Name: _____

Open Book, Open Notes. Time Limit: 1 hour, 15 minutes (pace yourself). Check for 5 pages in exam.

Write your work and all your answers in these pages. Use the back of the pages for scratch work if needed. State clearly any assumptions made.

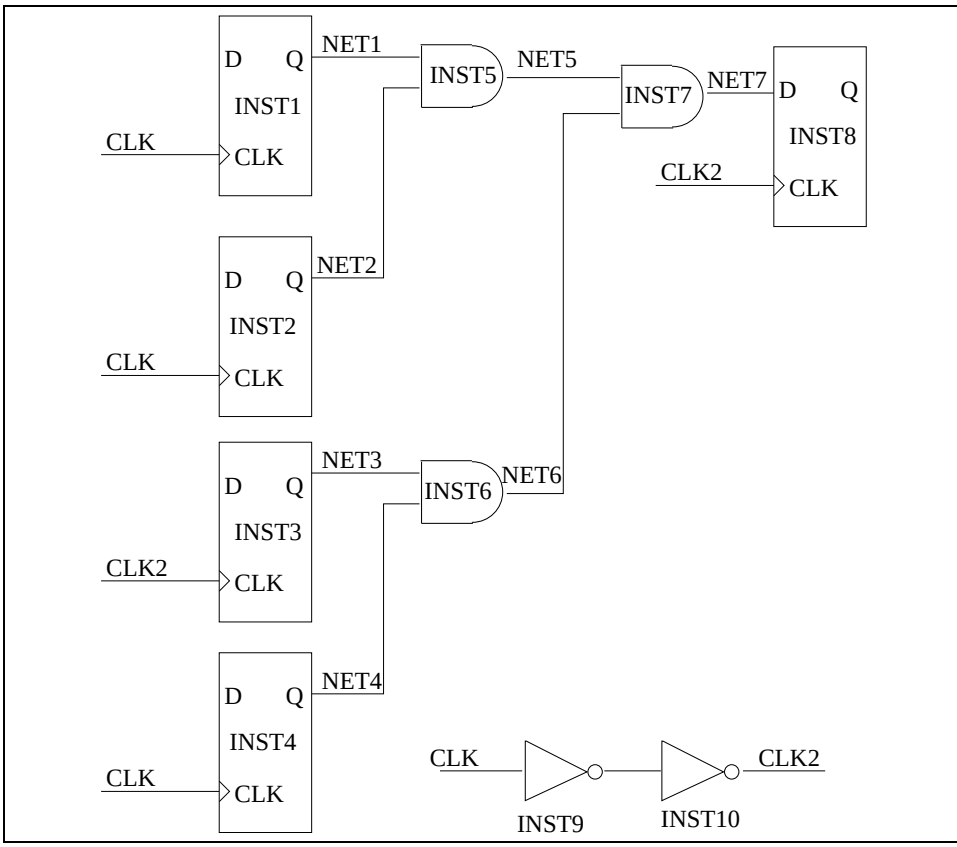
1. (25 points) Size the following path (A, B, C, D) using a 2:1 P:N ratio and a *stage ratio* of 3. Indicate the size of P and N transistors in the gates A, B, C and D.



2. (25 points)

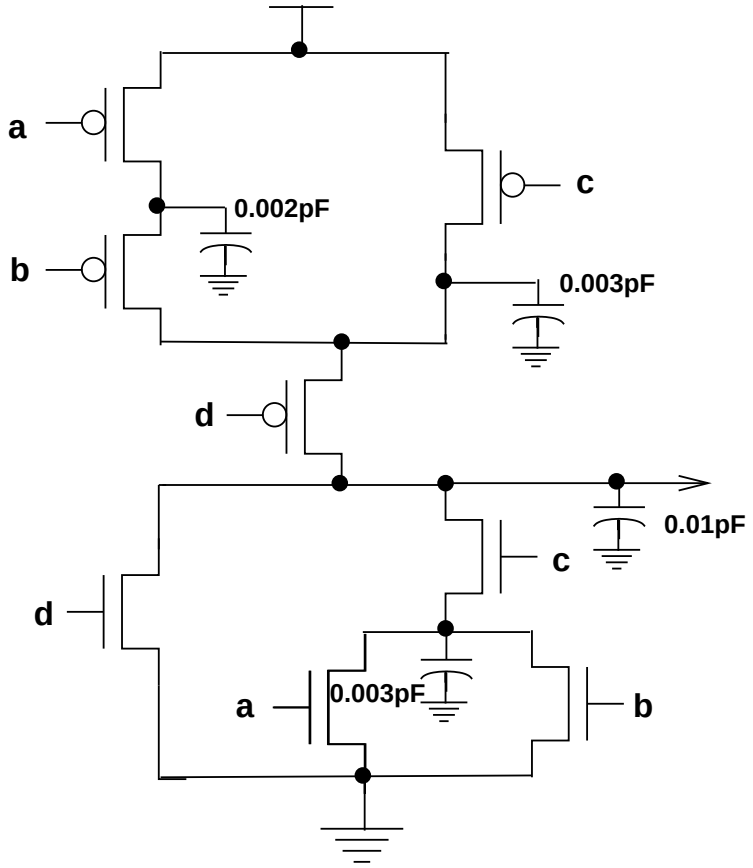
Identify if there are any hold time problems from the source flops (INST1, INST2, INST3 and INST4) to INST8 in the following circuit. If there are any, indicate by how much the hold time is violated and suggest a fix. Use the delays from the table below. Do not insert additional delays for the paths that have no hold violations.

	Rise	Fall
CLK ⇒ Q	370ps	370ps
Flop Hold Time	800ps	800ps
And Gate	300ps	200ps
Inverter Gate	50ps	20ps



3. (25 points)

In the static CMOS circuit below, the on-resistance of each n-channel transistor is 5 KOhms and that of a p-channel transistor is 10 KOhms. The gate capacitance of an n-channel transistor is 0.02pF and p-channel transistor is 0.03pF. The source/drain capacitance of an n-channel transistor is 0.001pF and for a p-channel transistor is 0.002pF. The routing capacitances for interconnections are lumped at the nodes as shown.



(a) A faulty circuit (after manufacture) has a "slow to fall" fault due to the n-channel transistor with input **a** having an abnormally high on-resistance of 50 kOhms. Find a test for the fault.

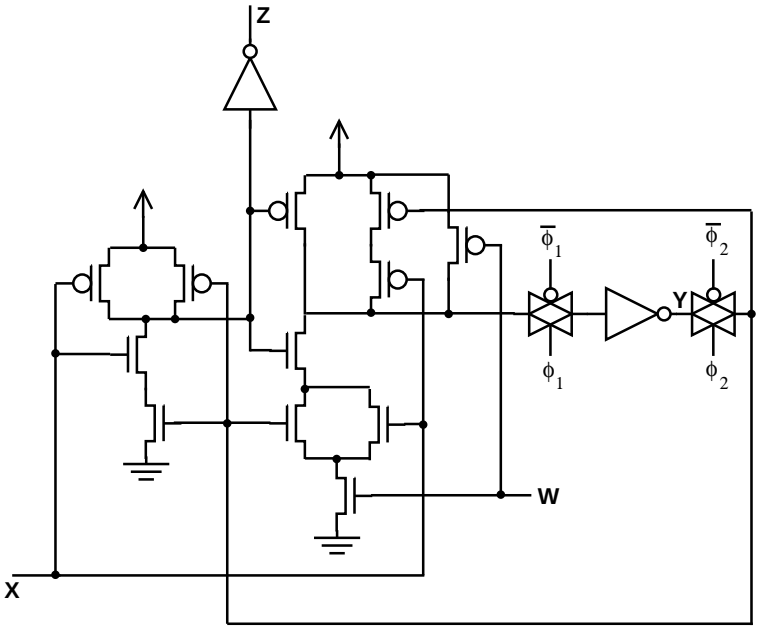
(b) Using the Penfield-Rubenstein technique, find the fall delay for the circuit without a fault, as well as that of the faulty circuit.

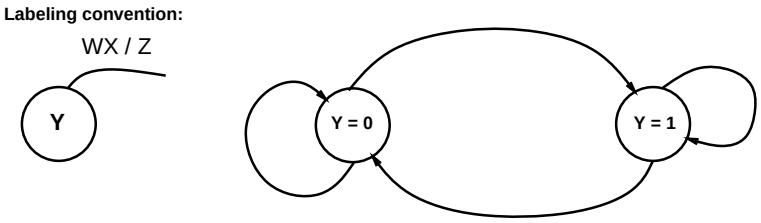
Delay of circuit without fault =

Delay of faulty circuit =

4. (25 points)

(a) The circuit below has two inputs, W and X, and one output Z. It has two states, implemented by the state variable Y. Complete the State Diagram for the circuit, labeling the arcs as indicated with the appropriate binary values of W, X and Z.





(b) What does the circuit do?

EE382M	VLSI I	J. Abraham
Fall 2002	EXAM. II	November 25, 2002

Name: STUDENT, GRADUATE

Open Book, Open Notes. Time Limit: 75 minutes (pace yourself). Check for 7 pages in exam.

Write all your answers in the spaces/boxes provided.

Show any calculations in these pages using the back of the pages if needed. State clearly any assumptions made.

PROBLEM	MAX	POINTS
1	15	
2	10	
3	20	
4	20	
5	15	
6	20	
TOTAL	100	

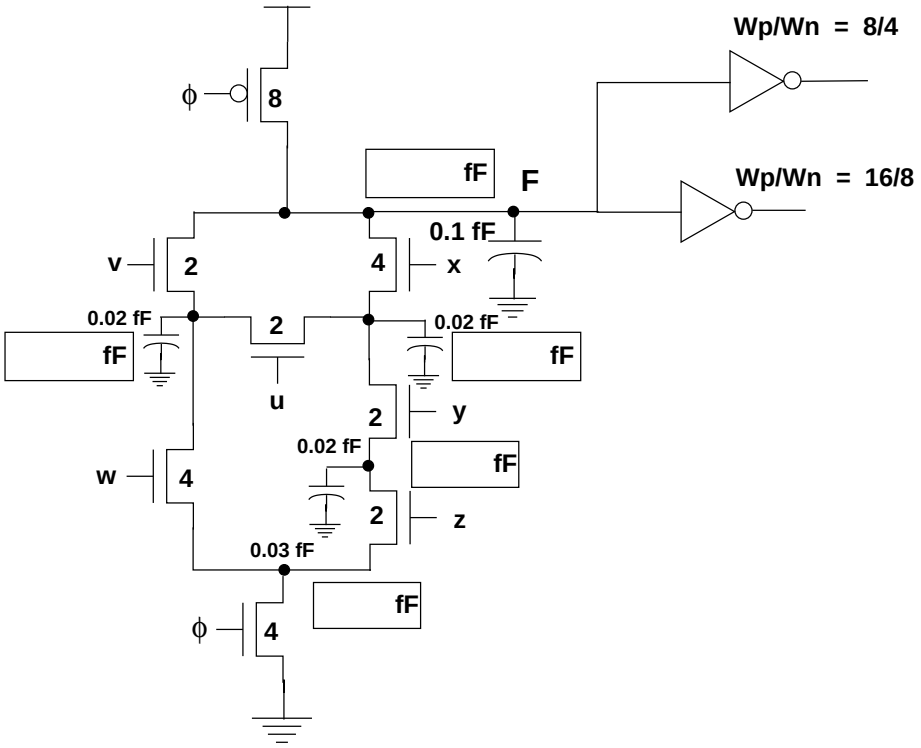
1. (15 points)

Using the Penfield-Rubenstein approach, find the **worst-case** time for the output of the following domino-CMOS gate to fall from 1 to 0 (when the clock ϕ goes from 0 to 1). The widths of the n-channel transistors in the domino circuit as well as the widths of the N- and P-channel transistors in the inverters are indicated in the figure. The parasitic capacitances are lumped at each node as shown. Use the following technology parameters:

On-resistance of n-channel transistor: 1000 $\Omega/\square$
Gate capacitance: 0.3 femtoFarads/$\square$
Approximate the diffusion capacitance (including area and periphery) as 0.25 femtoFarads/unit gate width

Write down the total capacitance at each node (in the box provided).

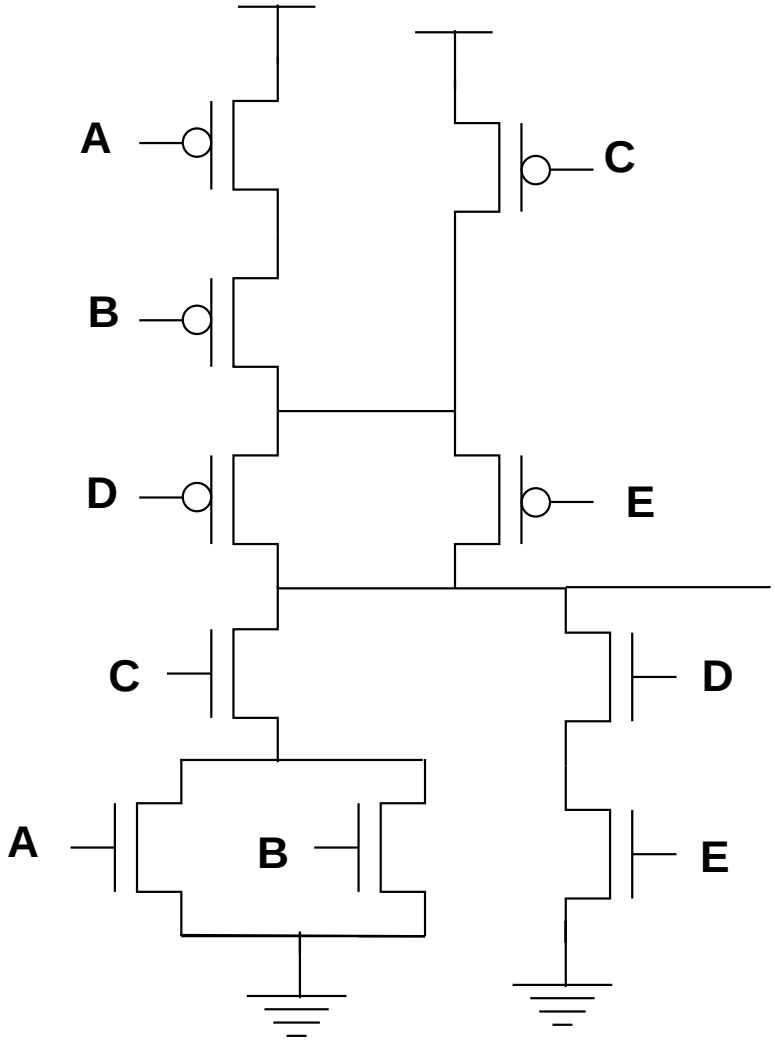
What are the input values which will result in the worst-case delay? uvwxy = [ ]



Total (max.) fall time: [ ] picoseconds.

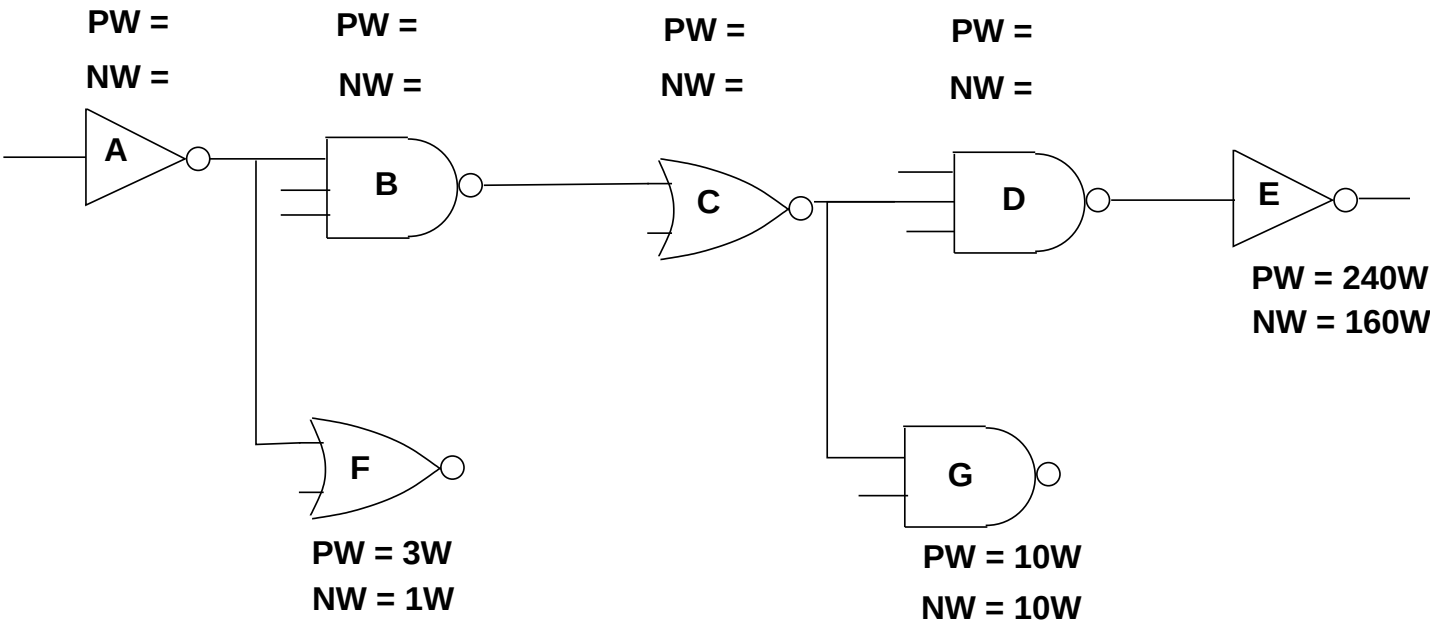
2. (10 points)

Size the following gate such that it has the same drive strength as inverter that has a PW=3 and NW=2.



3. (20 points)

Size the following transistors using a 3:2 P:N ratio and a stage ratio of 4. Indicate the sizes of the P and N transistors in gates A, B, C and D. In the case where the result is a fraction, round up (i.e., 3.2, 3.5 and 3.7 all round up to 4). Note that rounding needs to be done only when you determine PW and NW, and not in the middle of the calculation.

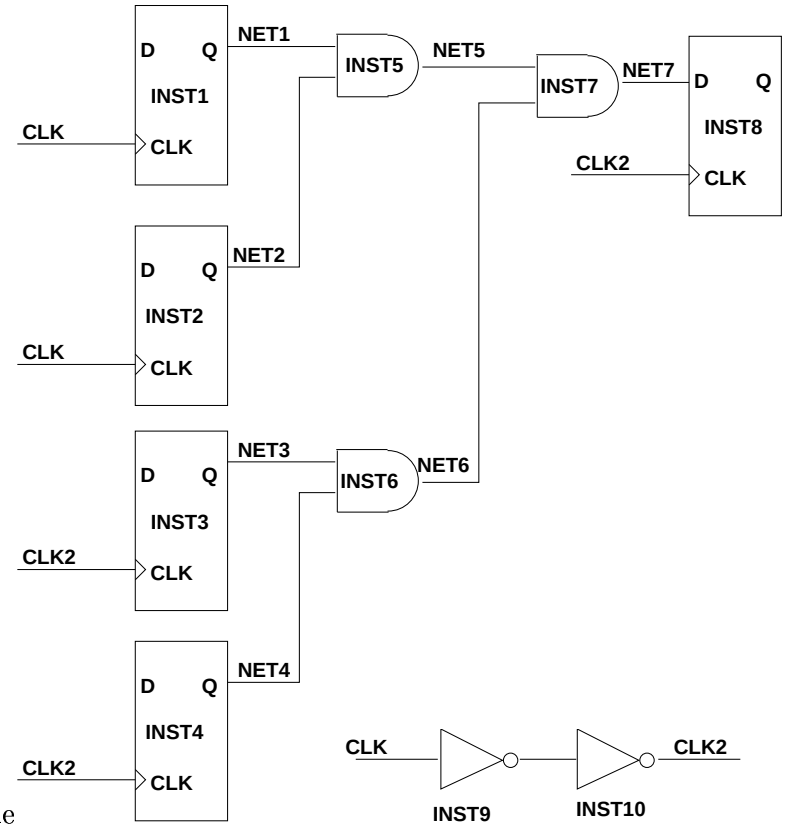


4. (20 points)

Identify if there are any hold time problems from the source flops (INST1, INST2, INST3 and INST4) to INST8 in the following circuit. If there are any, indicate by how much the hold time is violated and suggest a fix. Use the delays from the table below. Do not insert additional delays in the paths that have no hold violations. Identify the longest path delay before and after fixing the hold time violations. **Draw the fix with the lowest cost on the figure.**

	Rise	Fall
CLK → Q	500ps	500ps
Flop Setup Time	0ps	0ps
Flop Hold Time	750ps	750ps
And Gate	150ps	100ps
Inverter Gate	50ps	20ps

(Large numbers are used to illustrate the problem. These delays are not typical.)



centerline

Hold Delay, INST1 → INST 8: _____ picoseconds.

Hold Delay, INST2 → INST 8: _____ picoseconds.

Hold Delay, INST3 → INST 8: _____ picoseconds.

Hold Delay, INST4 → INST 8: _____ picoseconds.

Original Longest Path Delay: _____ picoseconds.

Longest Path Delay after the fix: _____ picoseconds.

5. (15 points)

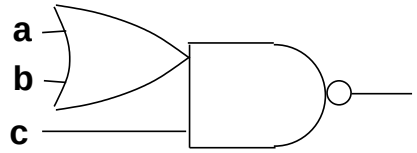


Figure 5.1

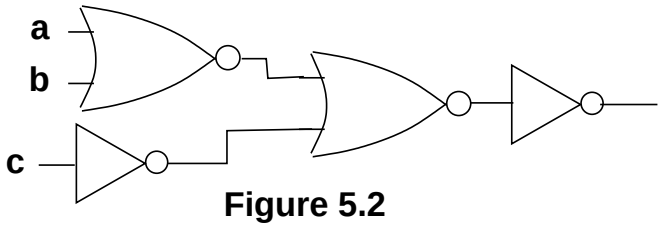


Figure 5.2

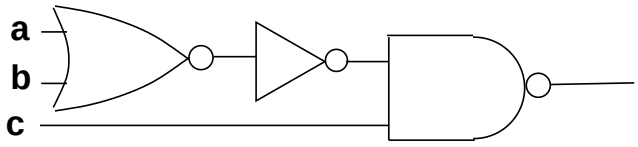


Figure 5.3

Gate	p
OAI21	2
NAND2	2
NOR2	2
INV	1

(a) Find the logical effort of the OAI21 gate inputs in Figure 5.1.

(b) Find the delays from a and c to y for all the three circuits above.

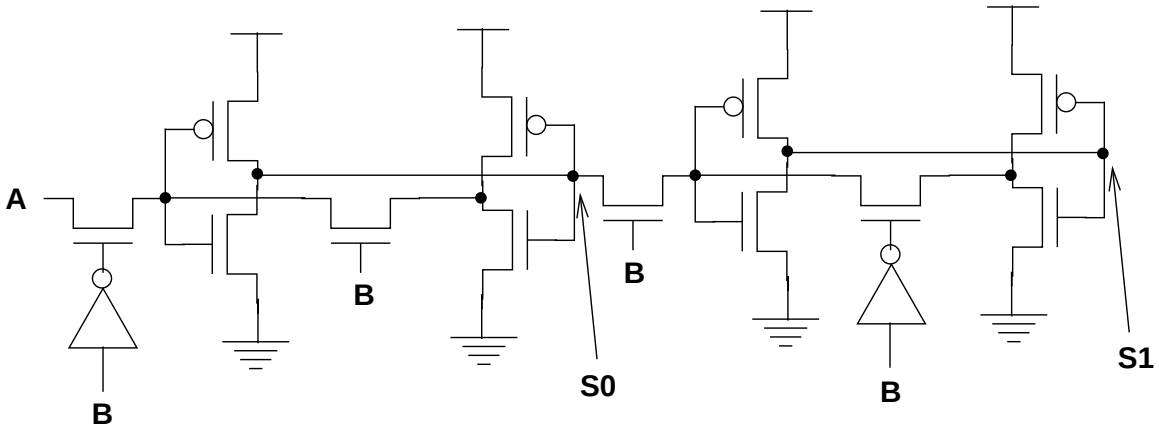
(c) Which of the above circuits do you recommend if the latest arriving signal is connected to

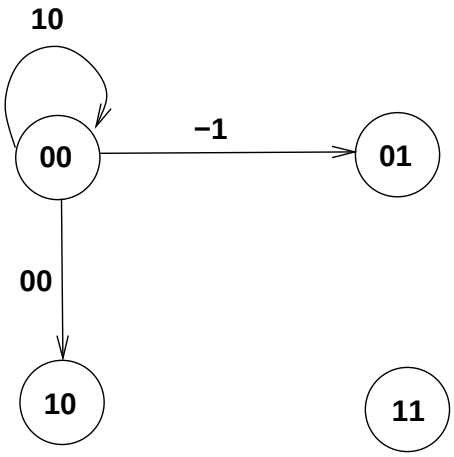
The a input ☐

The b input ☐

6. (20 points)

Complete the state transition diagram for the circuit below ("-" represents a "don't-care").





State: S0 S1

Transition: AB

EE360R **Computer-Aided IC Design** **J. Abraham**
Fall 2003 **EXAM. II** **November 11, 2003**

Name: Student, B

Signature: _____

Open Book, Open Notes. Time Limit: 90 minutes (pace yourself). Check for 6 pages in exam.

Write all your answers in the spaces/boxes provided.

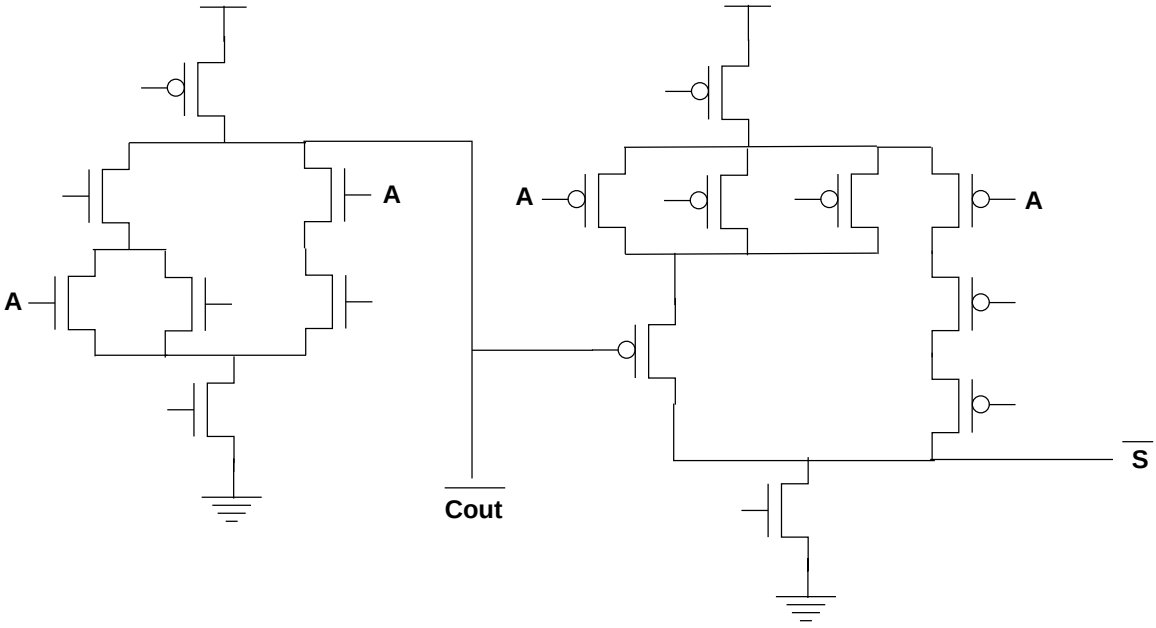
Show any calculations in these pages using the back of the pages if needed. State clearly any assumptions made. You will not receive partial credit if you don't show your steps toward the solution.

PROBLEM	MAX	POINTS
1	20	
2	15	
3	20	
4	20	
5	25	
TOTAL	100	

1. (20 points)

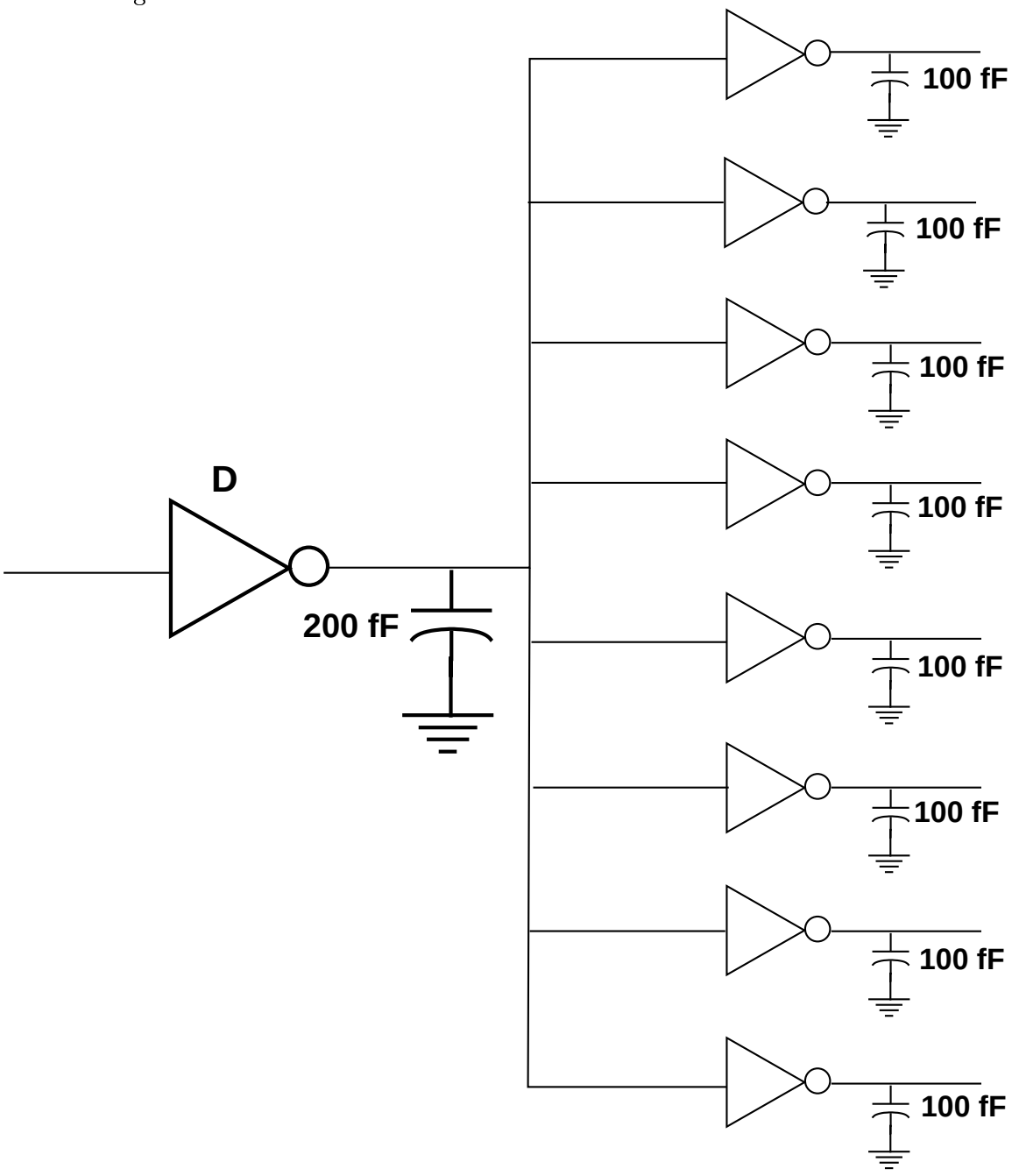
The dynamic circuit below is designed to take inputs A, B and C, and produce the complement of the sum ($\overline{S}$) and Carry out ($\overline{C_{out}}$) signals for a full adder.

Label the appropriate lines with the signals A, B, C, and the clocks, ϕ and $\overline{\phi}$, as appropriate, so that the circuit will perform the function of a full adder.



2. (15 points)

The circuit below is implemented in a 0.18 μ technology with a power supply of 2 Volts. All inverters have the P- and N-channel transistors sized so that the on-resistances are identical. The transistors comprising the inverter labeled D have on-resistances of 50 $\Omega/\square$, and the transistors for the other inverters have on-resistances of 100 $\Omega/\square$. The total capacitance of each of the nets is labeled in the figure.



What is the power consumed in this circuit when operating at 750 MHz?

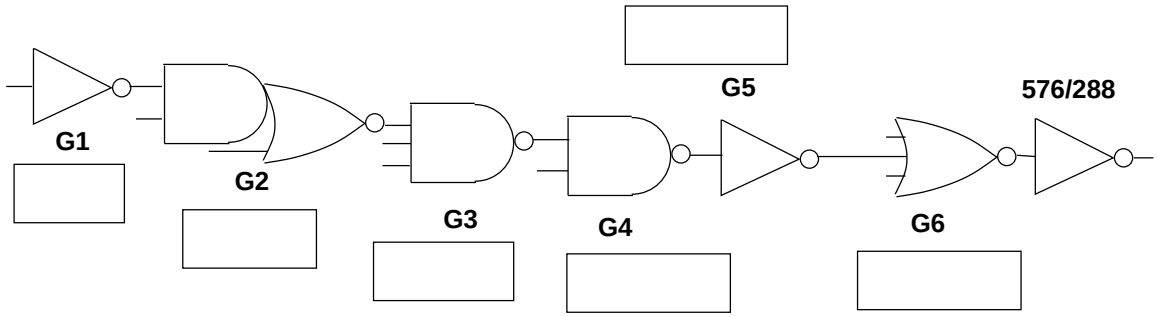
Power = [ ]

3. (20 points)

Size the following paths using:

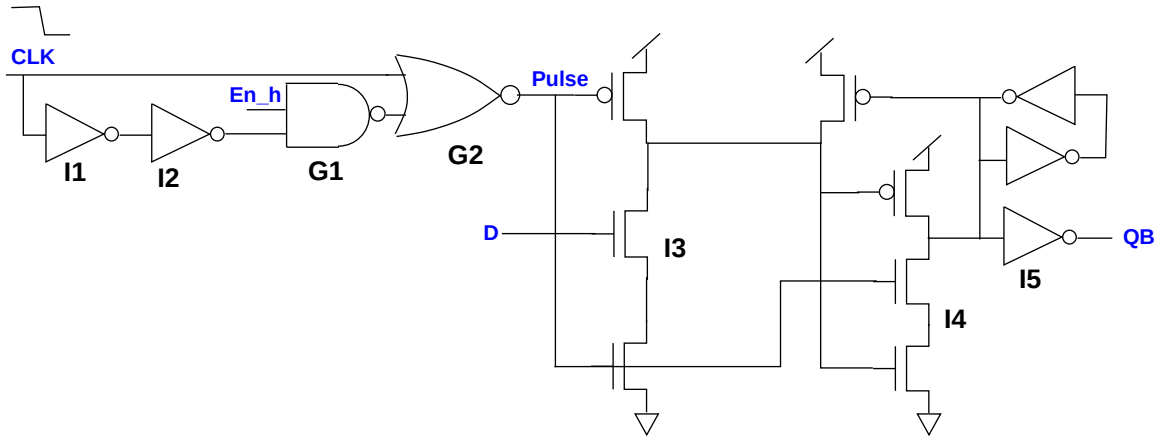
Stage ratio = 3
P:N = 2:1

Stay as close as possible to the above ratios.



4. (20 points)

The flip-flop in the figure below has the delays of the various components labeled (delay of the NAND gate is G1, etc.) Find the approximate setup time, hold time and clock-to-QB delay in terms of the delays of the basic gates and inverters (example, delay = G1 + I2). Use the single value of delay (I3 and I4) for the dynamic and clocked inverters shown at the transistor level.



Setup Time = ☐

Clock-to-QB delay = ☐

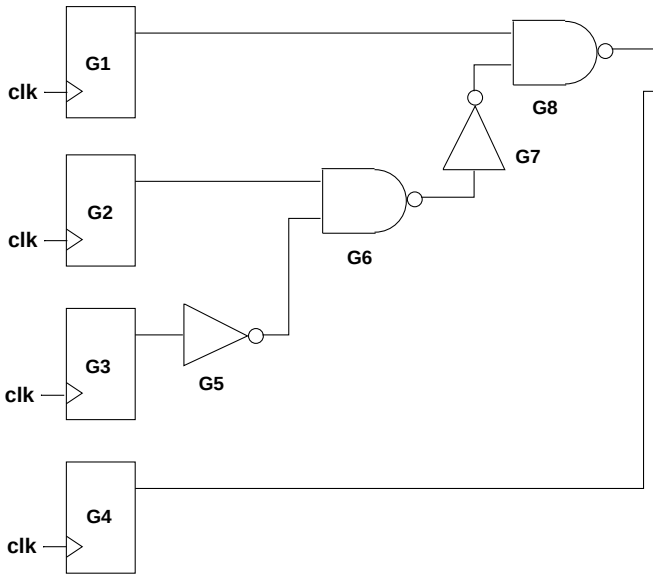
Hold Time = ☐

5. (25 points)

Identify if there are any hold time problems from the source flops (G1, G2, G3 and G4) to G11 in the following circuit. Sum the delays along the paths and show the amount of the violation under "Fail" (a negative number indicates that there is no hold-time violation.

Use the delays from the table below.

If there is any violation, show the fix on the circuit below (by using chains of inverters in the appropriate path). The additional inverters should impact as little of the circuit delay as possible.



	RISE	FALL
Flop Clk –> Q	300 ps	200 ps
Setup	150 ps	150 ps
Hold (after the clk/)	450 ps	450 ps
Nand2	100 ps	150 ps
Inv	50 ps	50 ps

Path	RISE at G11 input	Fail?	FALL at G11 input	Fail?
G1 → G11				
G2 → G11				
G3 → G11				
G4 → G11				

What is the maximum frequency of operation after fixing any hold-time violation? MHz

EE360R/EE382M **Introduction to VLSI Design** **J. A. Abraham, R. S. Tupuri**
Spring 2002 **Exam. II** **April 18, 2002**

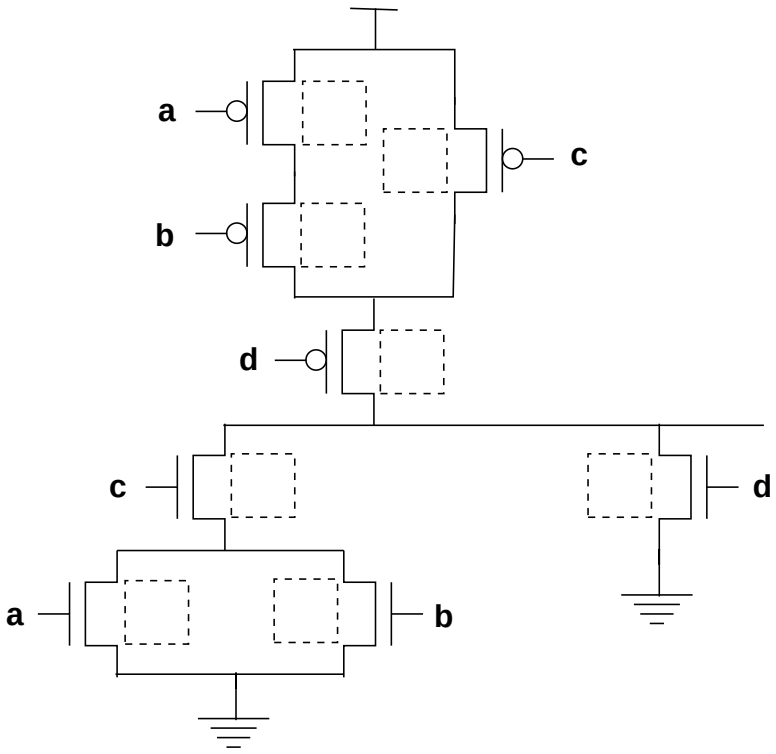
Name: _____

Open Book, Open Notes. Time Limit: 1 hour, 15 minutes (pace yourself). Check for 6 pages in exam.

Write your work and all your answers in the boxes provided for them. Use the back of the pages for scratch work if needed. State clearly any assumptions made.

1. (20 points)

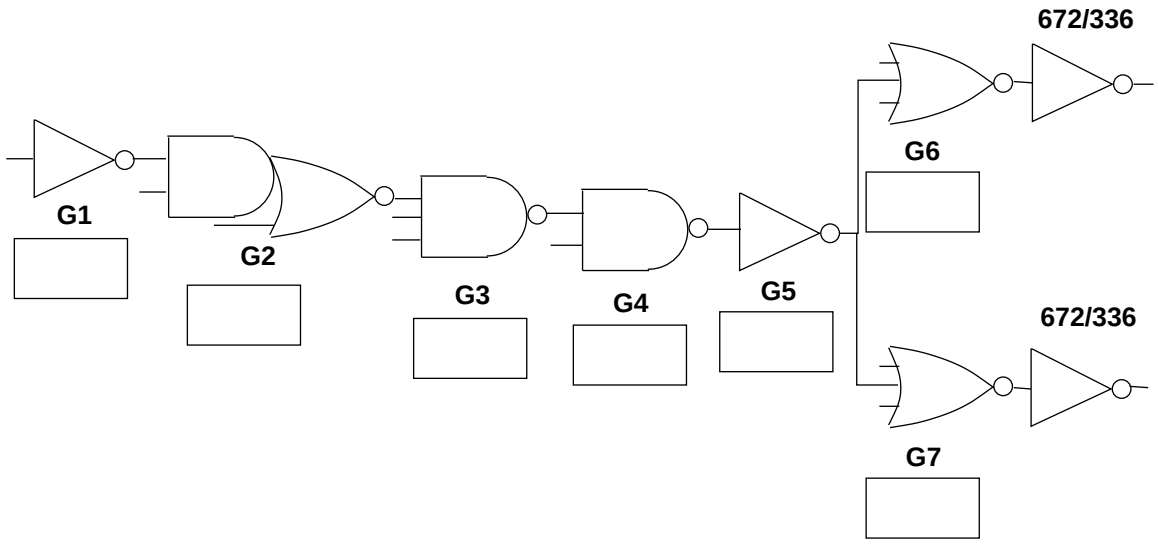
(a) Size the following complex gate so that it has the drive strength of an equivalent inverter with PW = 3 and NW = 2.



(b) Size the following paths using:

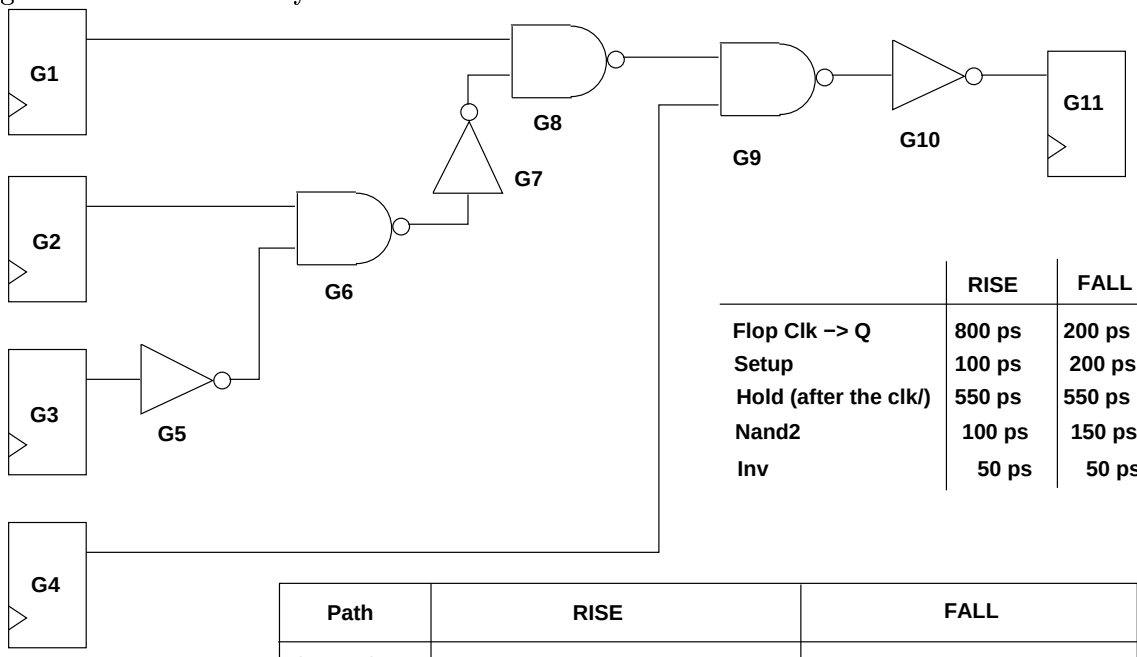
Stage ratio = 4 P:N = 2:1

Stay as close as possible to the above ratios.



2. (20 points)

(a) Identify if there are any hold time problems from the source flops (G1, G2, G3 and G4) to G11 in the following circuit. If there are any, indicate by how much the hold time is violated and suggest a fix. Use the delays from the table below.

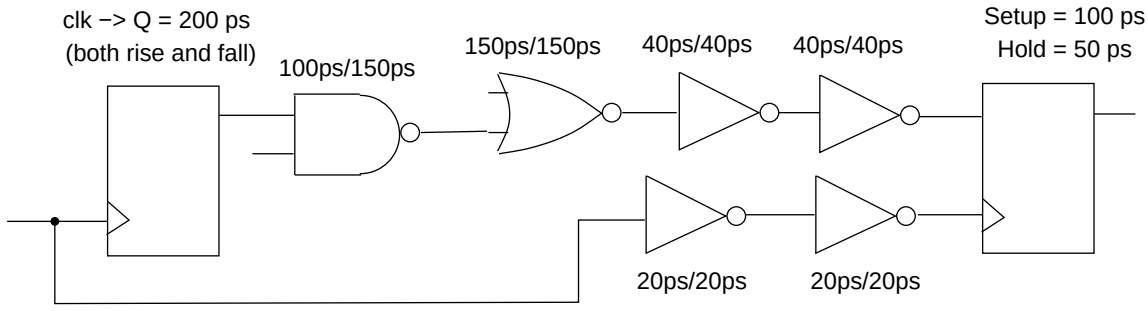


	RISE	FALL
Flop Clk –> Q	800 ps	200 ps
Setup	100 ps	200 ps
Hold (after the clk/)	550 ps	550 ps
Nand2	100 ps	150 ps
Inv	50 ps	50 ps

Path	RISE	FALL
G1 → G11		
G2 → G11		
G3 → G11		
G4 → G11		

What is the maximum frequency of operation after fixing any hold-time violation? MHz

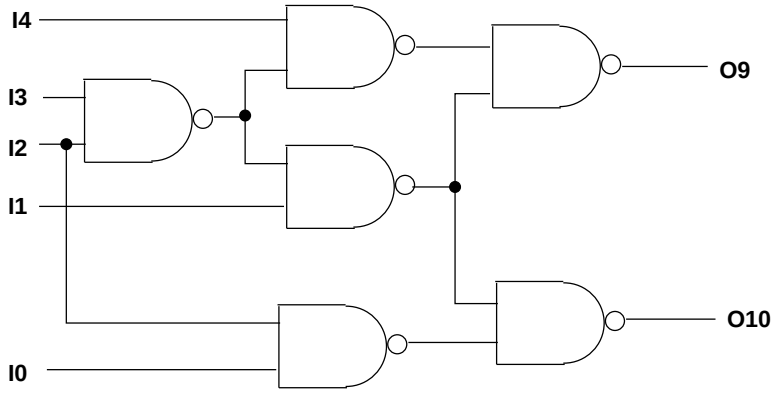
(b) What is the maximum frequency at which the following design can operate?

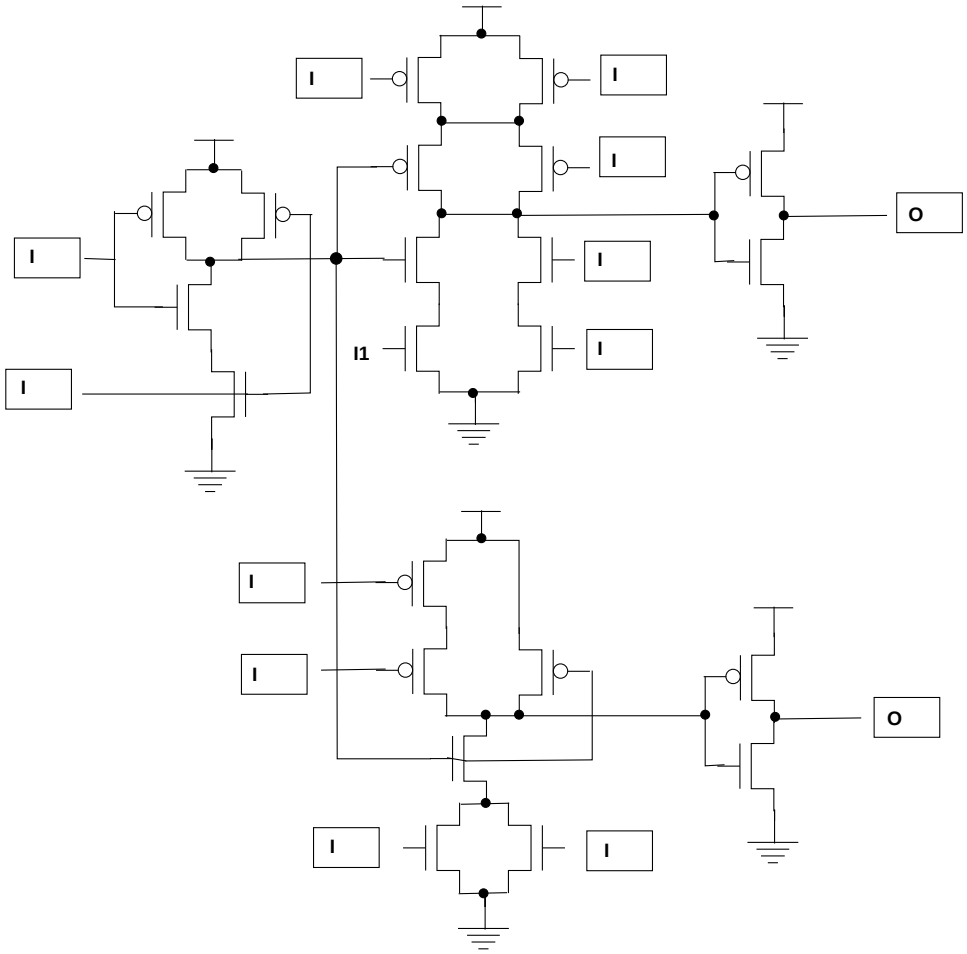


Frequency = MHz

3. (20 points)

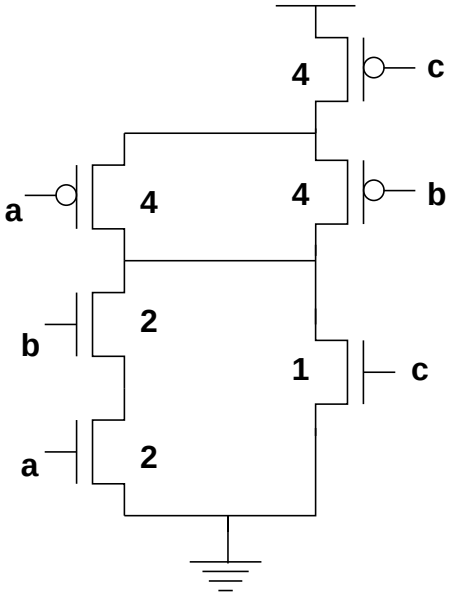
The gate level circuit below has been partially implemented with the transistor netlist at the bottom. Label the transistor gate inputs and the circuit outputs so that the gate level circuit is correctly implemented.





4. (20 points)

(a) Calculate the logical effort of the a, b and c inputs of the following AND-OR-INVERT (AOI) gate.

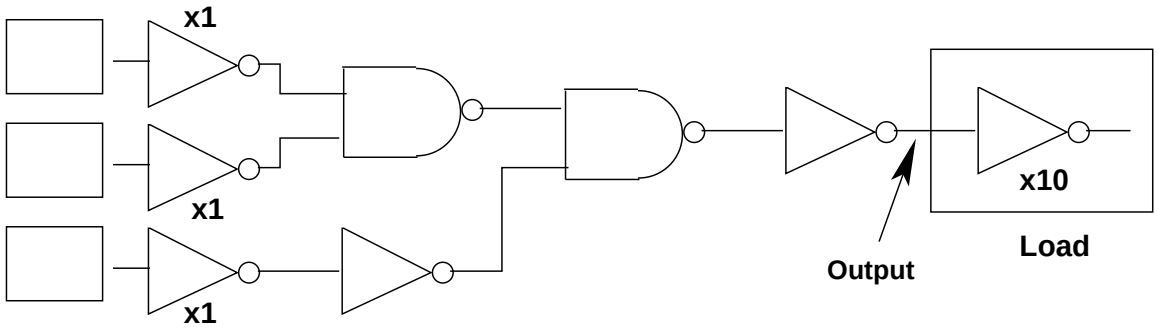


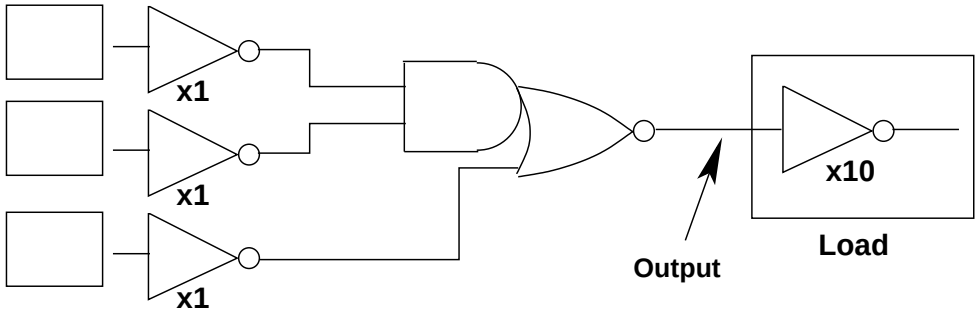
a =

b =

c =

(b) Compute the delays of the following paths (from each input to output (before the load)) using logical effort. The load inverter is ten times bigger than the input inverters. The parasitic delay of the AOI gate is 3, that of a NAND gate is 2 and that of an inverter is 1.

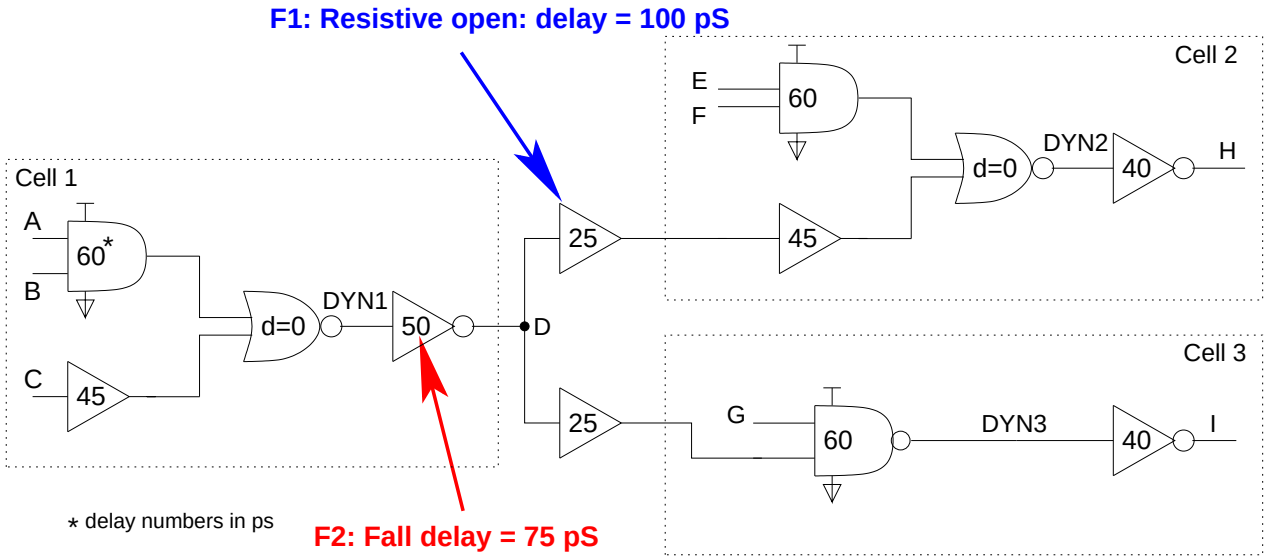




5. (20 points)

The following circuit is a logic model, extracted from three interconnected domino-logic cells at the transistor level, of a block between latches in a design which is supposed to have a cycle time of 250 picoseconds (excluding flop setup and clock-to-Q delays). The numbers on the logic symbols indicate the delays in picoseconds (the buffers model the wire delays).

There are two potential defects, F1 and F2, which cause delay faults (the rise/fall delay of a gate or the delay of the interconnect is increased to the number shown). Find tests for the two faults indicated (consider only one fault at a time), with values 0, 1 or X (don't care) for the variables.



Test for fault F1:

A	B	C	D	E	F	G	H	I

Test for fault F2:

A	B	C	D	E	F	G	H	I

EE360R/EE382M **Introduction to VLSI Design** **J. A. Abraham**
Spring 2005 **Exam. II** **April 27, 2005**

Name: _____

Class (382M/360R): _____

Open Book, Open Notes. Time Limit: 1 hour, 15 minutes (pace yourself). Check for 5 pages in exam.

Write your work and all your answers in the boxes provided for them. Use the back of the pages for scratch work if needed. State clearly any assumptions made.

1. (20 points)

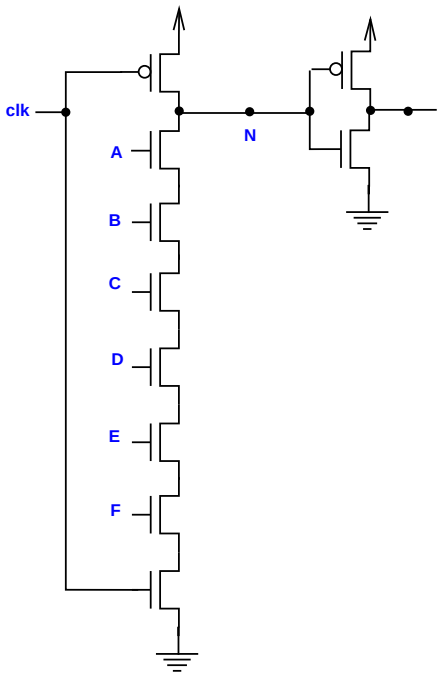
(a) Determine the worst-case charge sharing noise on the output of the N of the dynamic gate below as a function of V_{DD}, when the input is ABCDEF = 111101.

Assume that the diffusion capacitance on uncontacted nodes is half the gate capacitance and that on contacted nodes is equal to the gate capacitance. Also assume that all the nMOS transistors are minimum sized and the pMOS transistors are twice the width of the nMOS transistors.

V_{DD}

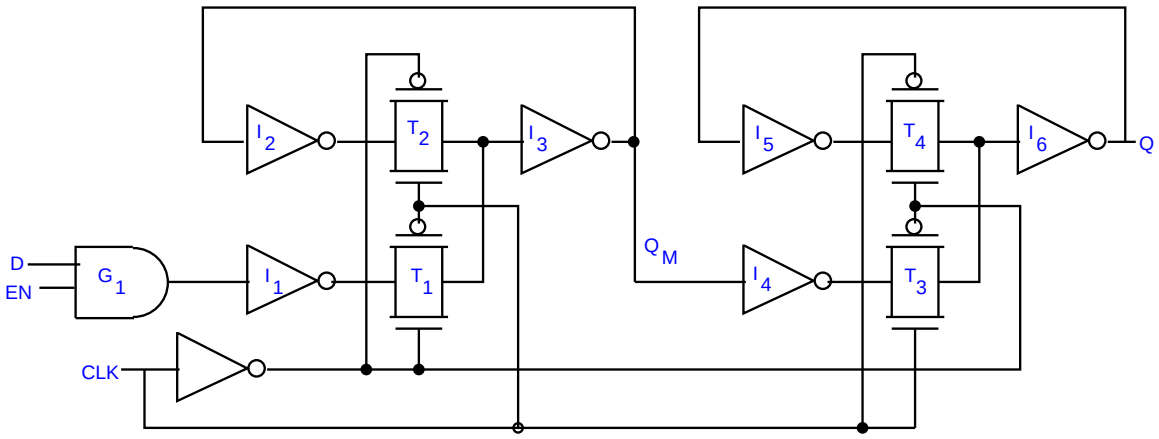
(b) What is the worst-case noise over all possible inputs?

V_{DD}



2. (20 points)

Write down the approximate setup time, hold time and clock-to-Q delay in the flip-flop below, in terms of the delays of the basic gates and inverters (example, I2 + T2 + I3).



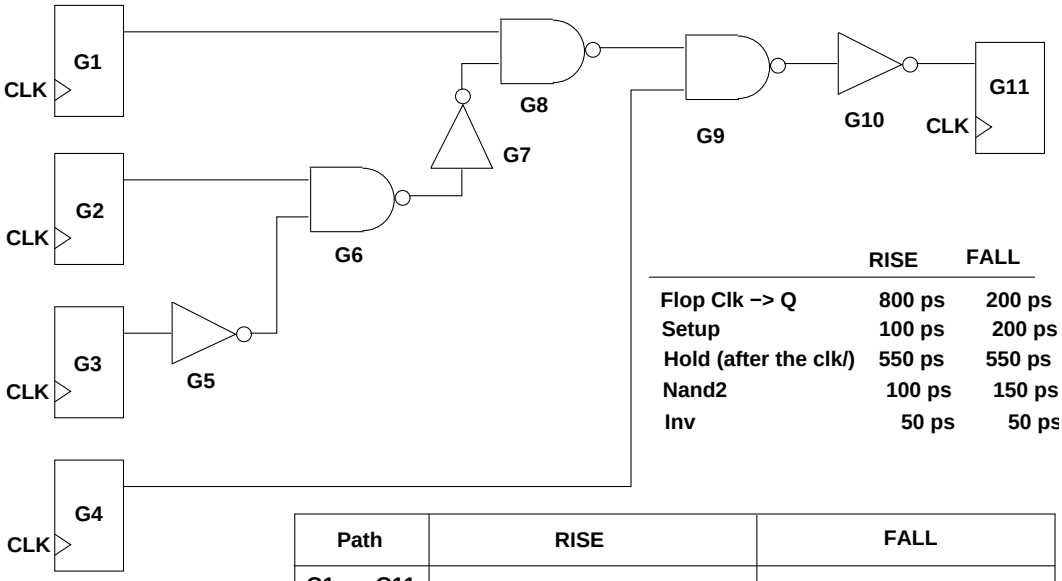
Setup Time =

Clock-to-QB delay =

Hold Time =

3. (25 points)

(a) Identify if there are any hold time problems from the source flops (G1, G2, G3 and G4) to G11 in the following circuit. If there are any, indicate by how much the hold time is violated and suggest a fix which minimizes the impact on the delay of the circuit. Use the delays from the table below.



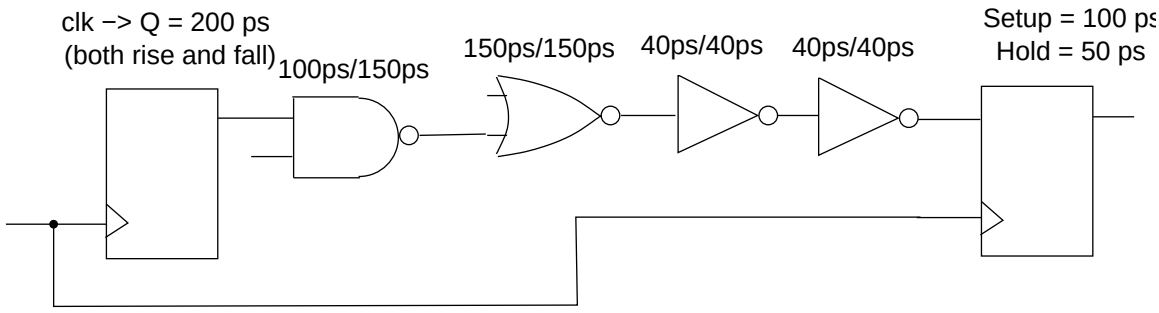
	RISE	FALL
Flop Clk –> Q	800 ps	200 ps
Setup	100 ps	200 ps
Hold (after the clk/)	550 ps	550 ps
Nand2	100 ps	150 ps
Inv	50 ps	50 ps

Path	RISE	FALL
G1→ G11		
G2→ G11		
G3→ G11		
G4→ G11		

What is the maximum frequency of operation after fixing any hold-time violation? MHz

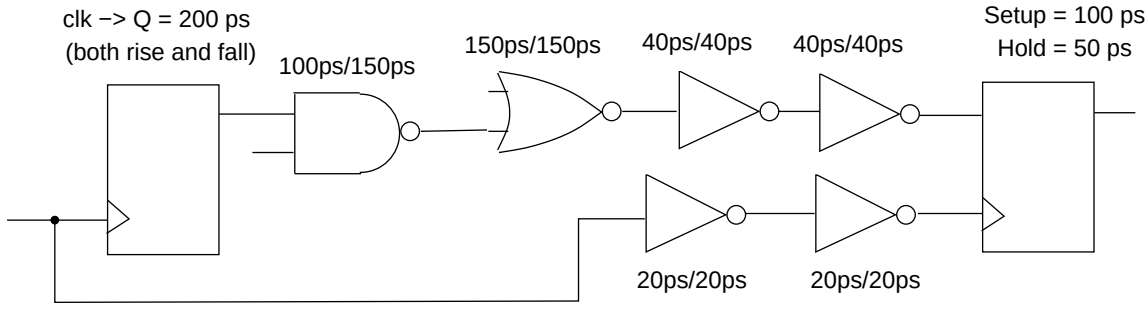
4. (20 points)

(a) What is the maximum frequency at which the following design can operate?



Frequency = MHz

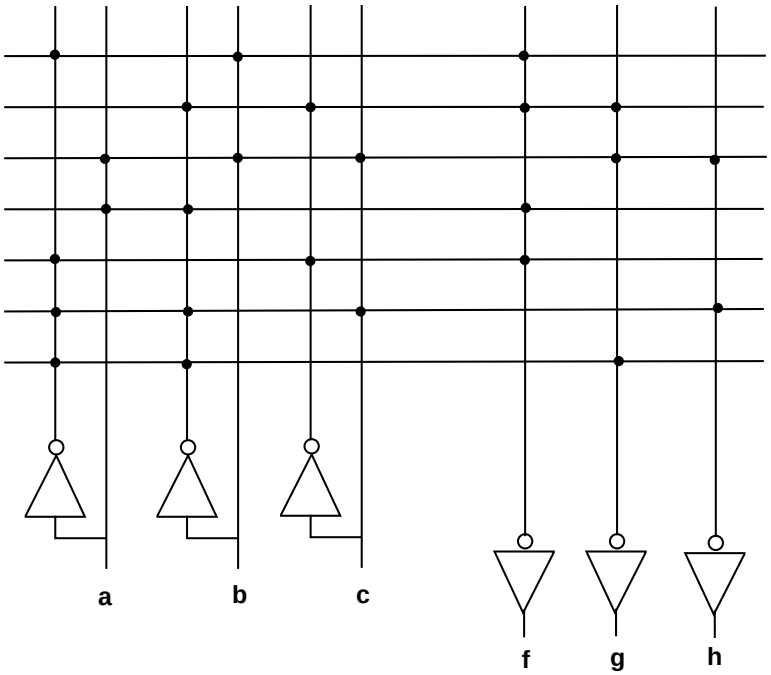
(b) What is the maximum frequency at which the following design can operate?



Frequency = MHz

5. (15 points)

Identify the functions, f, g and h implemented by the PLA below, drawn in dot notation.



☐ $f = \overline{a}\ \overline{b}\ \overline{c} + a\ b\ \overline{c}$

☐ $f = \overline{a}\ b + \overline{b}\ \overline{c} + a\ \overline{b} + \overline{a}\ \overline{c}$

☐ $f = a\ \overline{b} + b\ c + \overline{a}\ b + a\ c$

☐ $f = \overline{a}\ \overline{b}\ \overline{c} + b\ c + a\ b$

☐ $g = \overline{a}\ \overline{b}\ \overline{c} + b\ c + a\ b$

☐ $g = a\ b\ c + \overline{b}\ \overline{c} + \overline{a}\ \overline{b}$

☐ $g = \overline{a}\ b + \overline{b}\ \overline{c} + a\ \overline{b} + \overline{a}\ \overline{c}$

☐ $g = a\ b\ c + \overline{a}\ \overline{b}\ c$

☐ $h = a\ \overline{b} + b\ c + \overline{a}\ b + a\ c$

☐ $h = a\ b\ c + \overline{a}\ \overline{b}\ c$

☐ $h = a\ b\ c + \overline{b}\ \overline{c} + \overline{a}\ \overline{b}$

☐ $h = \overline{a}\ \overline{b}\ \overline{c} + a\ b\ \overline{c}$

	VLSI Design	**J. Abraham**
Spring 2006	**EXAM. II**	**April 12, 2006**

Name: Exam, No. 1

Open Book, Open Notes. Time Limit: 75 minutes (pace yourself). Check for 5 pages in exam.

Write all your answers in the spaces/boxes provided.

Show any calculations in these pages using the back of the pages if needed. State clearly any assumptions made.

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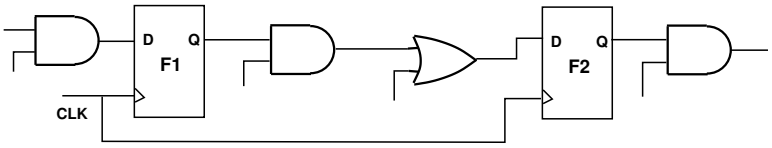
1. (20 points)

The circuit below has the following parameters for the components:
Clock period = 90 nS with a 50% duty cycle
t_{clk-q} **= 40 nS**
t_{setup} **= 20 nS**
t_{hold} **= 45 nS**
AND gate delay = 15 nS
OR gate delay = 20 nS
Inverter delay = 5 nS

Assume that the logic before F1 and after F2 has arbitrary slack and is impervious to timing issues.



(a) Will this circuit work correctly? Explain, and find the magnitude of the violation, if any.

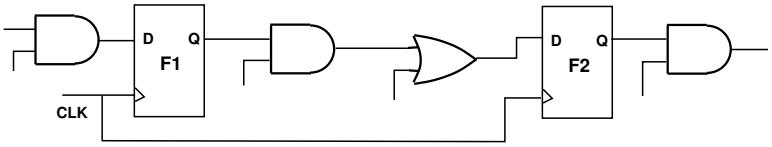
(b) If you cannot move any cells, but can add inverters anywhere in the design, show the new design which fixes the violation but does not change the functionality. Show the modification in the diagram above.

(c) If the design above has already been implemented in Silicon, you cannot change the design or add circuitry. Is there still a way to make the circuit work? Explain.

2. (25 points)

The circuit below has the following parameters for the components:
Clock period = 90 nS with a 50% duty cycle.
t_{clk-q} **= 5 nS**
t_{setup} **= 20 nS**
t_{hold} **= 45 nS**
AND gate delay = 15 nS
OR gate delay = 20 nS
Inverter delay = 5 nS

Assume that the logic before F1 and after F2 has arbitrary slack and is impervious to timing issues.



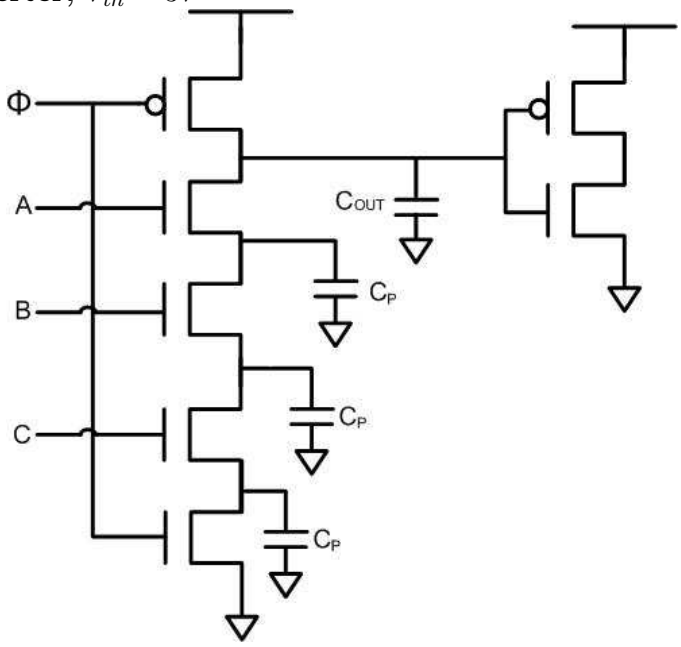
(a) Will this circuit work correctly? Explain, and find the magnitude of the violation, if any.

(b) If you cannot move any cells, but can add inverters anywhere in the design, show the new design which fixes the violation but does not change the functionality. Draw the inverters in the diagram above.

(c) If the design above has already been implemented in Silicon, you cannot change the design or add circuitry. Is there still a way to make the circuit work? Explain.

3. (20 points)

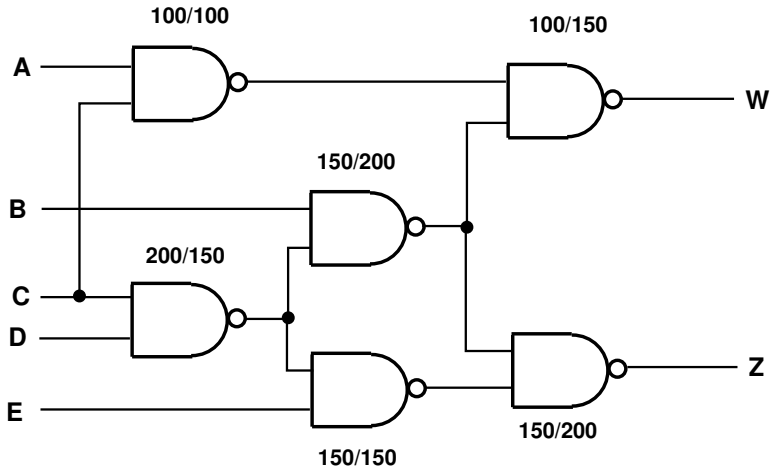
Find the minimum output capacitance, C_{OUT}, so that the domino circuit will work correctly for all input combinations. Assume the following:
All intermediate node capacitances, $C_p = 0.4pF$
$V_{DD} = 5V$
For the static inverter, $V_{th} = 3V$



Minimum value of C_{OUT} = ____

4. (20 points)

The following is a combinational circuit between two sets of flip-flops. The rise/fall delays (in pS) of each of the gates is shown. You are to analyze the circuit for information relating to the clocking of the system, and to find tests which will exercise the system for different conditions. When generating the tests, assign logic values to the smallest possible set of variables, leaving as many variables with X as possible.



(a) Find the delay through the circuit which will have the maximum impact on the clock frequency, and a test sequence for this delay.

Delay which has maximum impact on clock frequency = ☐

Test which produces this delay in the circuit:

A	B	C	D	E	W	Z

(b) Find the delay through the circuit which will have the largest impact on the hold time requirements, and a test sequence for this delay.

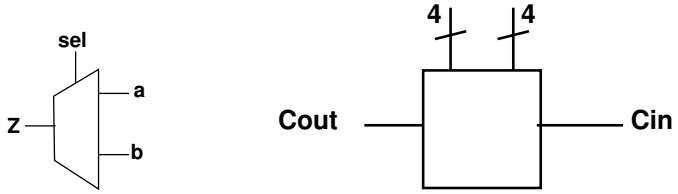
Delay which has largest impact on hold time = ☐

Test which produces this delay in the circuit:

A	B	C	D	E	W	Z

5. (15 points)

An application requires the carry out result of the addition of two 12-bit numbers, with the result to be produced in 1 nS. Design a circuit to achieve this, using ONLY two types of cells, a 4-bit adder with a delay of 400 pS and a 2-1 1-bit multiplexer with a delay of 100 pS.



Draw a neat block diagram of your circuit below.

	VLSI Design	**J. Abraham**
Spring 2006	**FINAL EXAM.**	**May 10, 2006**

Name: Student, Undergraduate

Open Book, Open Notes. Time Limit: 3 hours (pace yourself). Check for 7 pages in exam.

Write all your answers in the spaces/boxes provided.

Show any calculations in these pages using the back of the pages if needed. State clearly any assumptions made.

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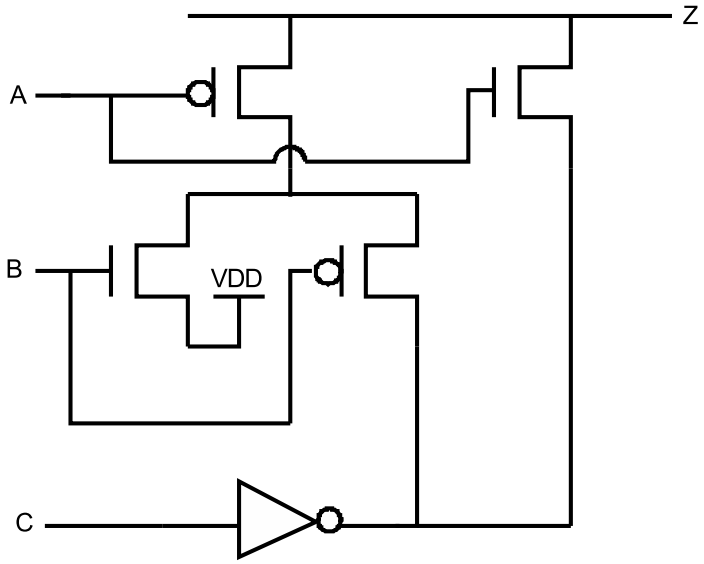
1. (10 points)

What is the logic function implemented by the circuit below (assuming that any V_t drops would be within margins)?



Z = ____

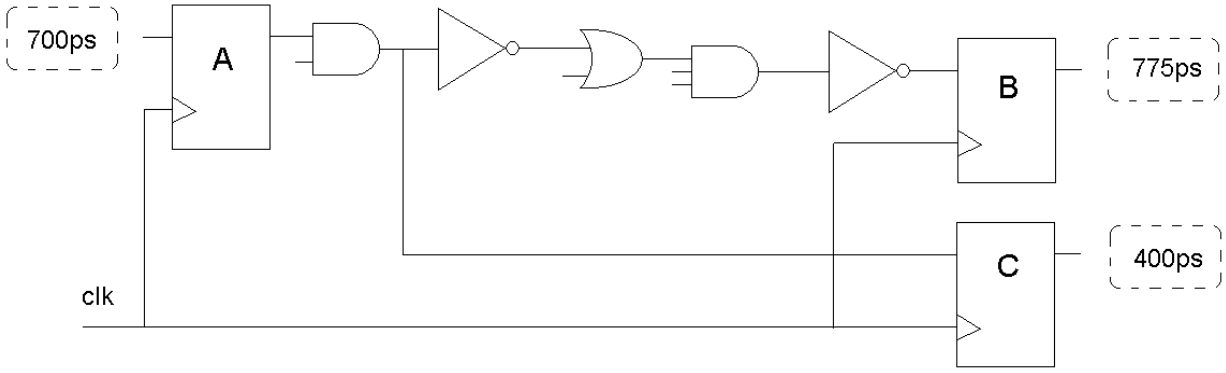
2. (15 points)

You are designing a specific stage in a pipelined circuit. The delay of the previous stage is 700 ps and your stage is to have a delay of at most 775 ps, and your design has to work with the other stages being designed by other people. The path from flop A to flop B is the ONLY critical path in this stage, and the other paths have plenty of slack.

The cells used in the design and their parameters are as follows.

	Setup	Hold	CLK to Q
DFF1	**250**	**275**	**400**
DFF1	**150**	**350**	**250**
DFF1	**200**	**325**	**200**

Cell	Delay
AND2	**100**
AND3	**200**
INV	**75**
OR2	**125**



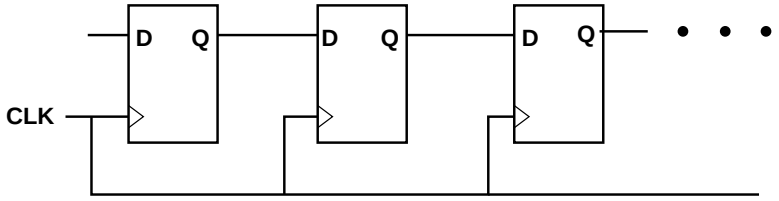
(a) Based on the data sheets of the cell library, which flip-flop would you use for A, B, and C respectively?

Flop A:
Flop B:
Flop C:

(b) One day, designers of the previous stage realized that they underestimated the delay of their stage by 75 ps, and they would like to borrow this from your stage by delaying the clock to your stage. Unfortunately, you cannot borrow time from the following stage. What would you do to reduce the delay of your critical path by at least 75 ps (using only the cells in the library)?

3. (10 points)

The flops used in the shift register below have a setup time of 100 ps a maximum clock-Q delay of 150 ps and a minimum clock-Q delay of 100 ps.



(a) How fast can this circuit be clocked?

Clock frequency = ☐ **MHz**

(b) What is the limit on the hold time of the flops at this frequency?

Hold time < ☐ **ps**

(c) What is the limit on the hold time of the flops at a frequency of 1 GHz?

Hold time < ☐ **ps**

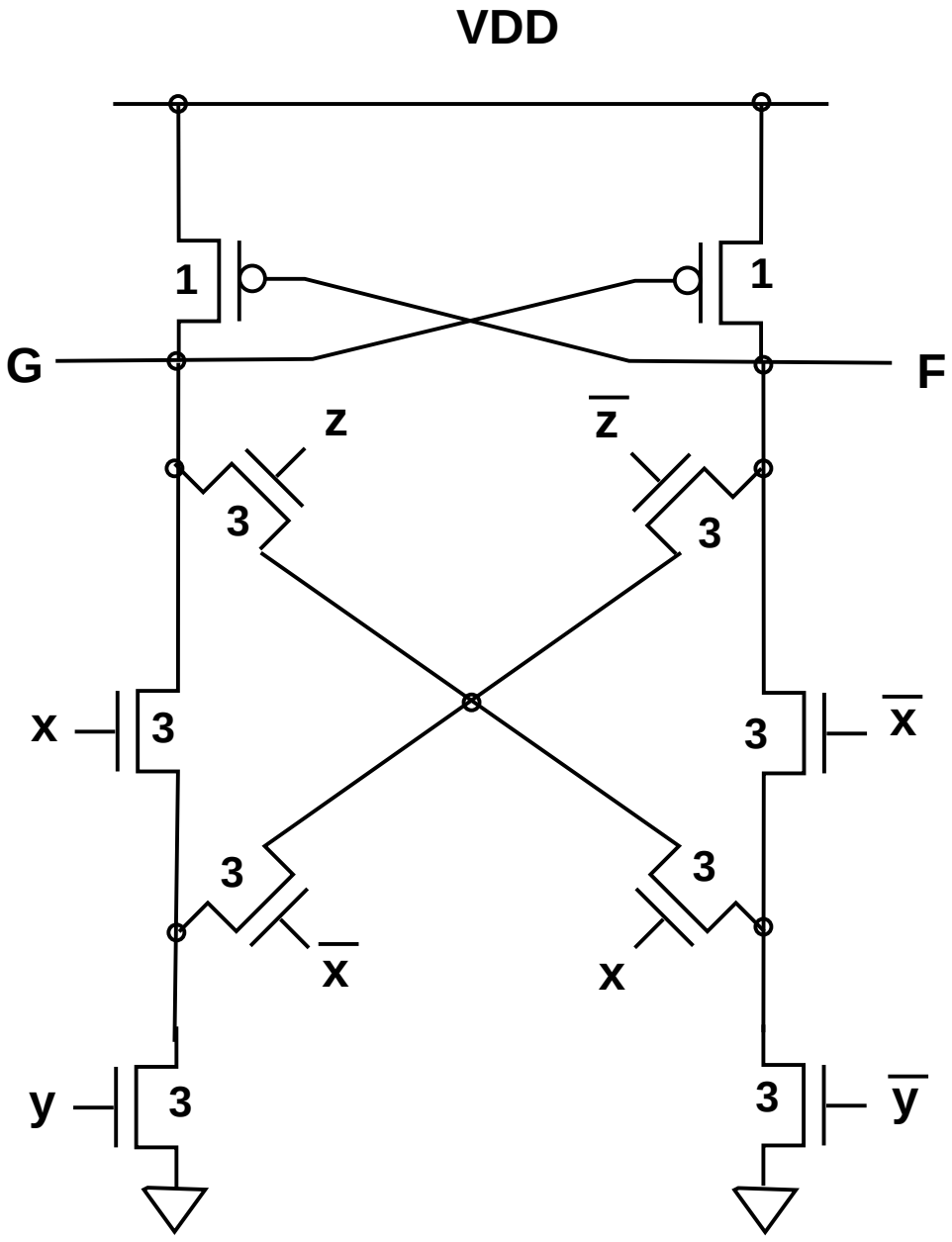
4. (10 points)

A synthesized design in 180 nm technology using standard cell libraries has an average switching capacitance of 150 pF/mm^2, and the area of the synthesized random logic is 50 mm^2. If the activity factor is 0.15, V_{DD} is 0.9 V and the clock speed is 500 MHz, what is the power consumption?

Power = ☐ **Watts**

5. (10 points)

Find the logical effort values for x, y, z in the circuit below. Assume that inverted inputs, such as $\overline{x}$, are generated independently



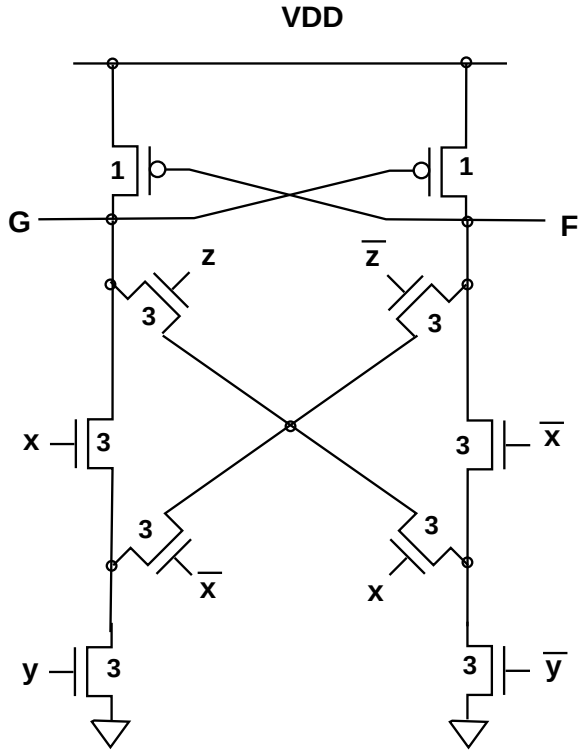
Logical Effort for input x = ____

Logical Effort for input y = ____

Logical Effort for input z = ____

6. (15 points)

This problem is to find the *smallest* and *largest* fall delays for the output F in the circuit below. The gate sizes of the transistors are shown in the figure. Use the assumption that the diffusion capacitance is equal to the gate capacitance and that a minimum sized transistor has gate and diffusion capacitance equal to C. The resistance of a nMOS transistor with unit width is R. Also assume NO sharing of diffusion regions.



(a) Write down an input sequence of two input patterns which results in charging up the intermediate nodes, causing the largest fall delay. Explain why this would be the largest delay.

(b) Write down an input sequence of two input patterns which results in charging up the intermediate nodes, causing the smallest fall delay. Explain why this would be the smallest delay.

7. (15 points)

Consider a design using latches and flops with the following parameters.

	Setup Time	clk-Q delay	D-Q delay	Contamination Delay	Hold Time
Flops	**65 ps**	**50 ps**	–	**35 ps**	**30 ps**
Latches	**25 ps**	**50 ps**	**40 ps**	**35 ps**	**30 ps**

(a) What is the maximum logic propagation delay available in a cycle for a traditional domino pipeline using a 500 ps clock cycle, with zero clock skew?

Delay = ☐ **ps**

(b) What is the maximum logic propagation delay available in a cycle for a traditional domino pipeline using a 500 ps clock cycle, with a clock skew of 50 ps?

Delay = ☐ **ps**

(c) Consider a four-phase skew-tolerant domino pipeline with a 500 ps clock cycle. How much time can one phase borrow into the next if the clock skew can be up to 50 ps and the clocks each have a 50% duty cycle?

Borrow time = ☐ **ps**

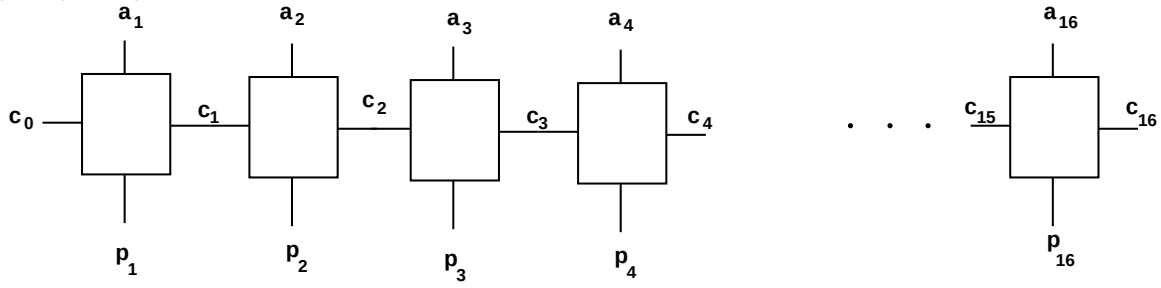
8. (15 points)

A priority circuit is implemnted as an iterative logic array below. In this circuit, the output p_i is 1 if inputs $a_1, a_2, ...a_{i-1}$ are all 0 and $a_i = 1$. The signal $c_0 = 0$, and $c_i = 1$ indicates that some previous input has priority.

The functions c_i and p_i are given by:

$c_i = a_i + c_{i-1}$

$p_i = \overline{c_{i-1}} \cdot a_i$



(a) If the functions c_i are implemented with a 2-input NOR gate followed by an inverter, with the sizes of each being equivalent to a 2:1 inverter, find the delay of the output c_{16} using logical effort.

(b) Show how the above delay can be reduced by using a "lookahead" circuit implemented using 4-input OR functions. Sketch the speedup circuit on the figure above (and label the 4-input ORs with the appropriate signals)

(c) If the 4-input OR function is implemented using 4-input NOR gates (sized to be equivalent to a 2:1 inverter) followed by a 2:1 inverter, what is the delay of the output c_{16} (using logical effort) using the approach in (b)?

EE360R	**Computer-Aided IC Design**	**J. A. Abraham**
Spring 2005	**Final Exam.**	**May 13, 2005**

Name: _____

Open Book, Open Notes. Time Limit: 3 hours (pace yourself). Check for 7 pages in exam.

Write your work and all your answers in the boxes provided for them. Use the back of the pages for scratch work if needed. State clearly any assumptions made.

1. (15 points)

The transistors in the dynamic circuit below have unit lengths and their widths are provided. Assume that the gate capacitance of a unit transistor (length=width=1) is C, and that the source and drain capacitances are *each* equal to the gate capacitance, for both uncontacted and contacted nodes (for example, for a gate width of 5, the capacitances for gate = source = drain = 5C).

(a) Initially, clk=0 and all other inputs are 1. Determine the worst-case charge sharing *noise* on the output, OUT, of the dynamic gate below as a function of V_{DD}, when the input is changed to clk = 1, A = 1 and BCDE = 0000.

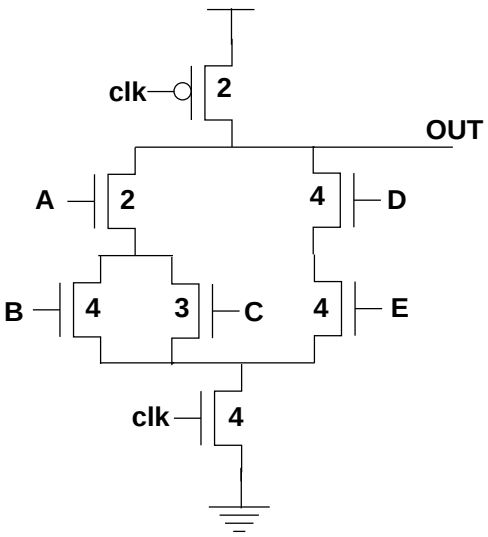
V_{DD}

(b) Again, initially, clk=0 and all other inputs are 1. Determine the worst-case charge sharing noise when clk becomes 1 and the other inputs are unchanged.

V_{DD}

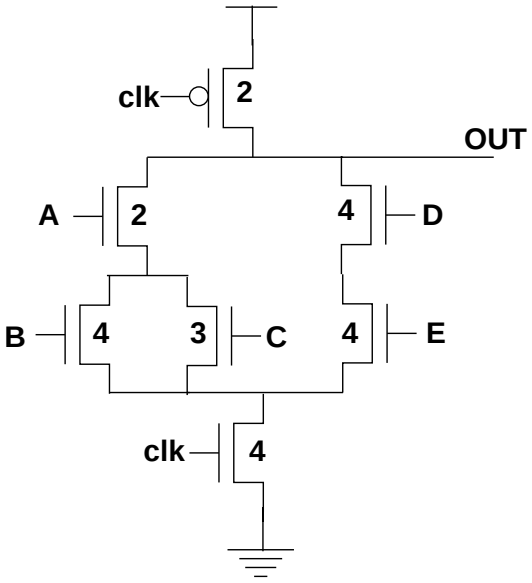
(c) Again, initially, clk=0 and all other inputs are 1. Determine the inputs which cause the worst-case charge sharing noise when clk becomes 1 and the amount of the noise.

V_{DD}



2. (20 points)

The transistors in the dynamic circuit below have unit lengths and their widths are provided. Assume that the on-resistance of a transistor of unit size (length=width=1) is R, and the gate capacitance of a unit transistor is C, and that the source and drain capacitances are *each* equal to the gate capacitance, for both uncontacted and contacted nodes (for example, for a gate width of 5, the capacitances for gate = source = drain = 5C).



(a) Using the Elmore delay approximation, find the *worst case* delay for an output transition from 1 to 0 (in terms of R and C)

Delay = [ ]

(b) What sequence of inputs would produce the conditions for the worst-case delay?

Sequence {ABCDE, ABCDE} = [{ , }]

(c) What would be the *best case* delay for an output going from 1 to 0? (Hint: use the equivalent resistance for a network.)

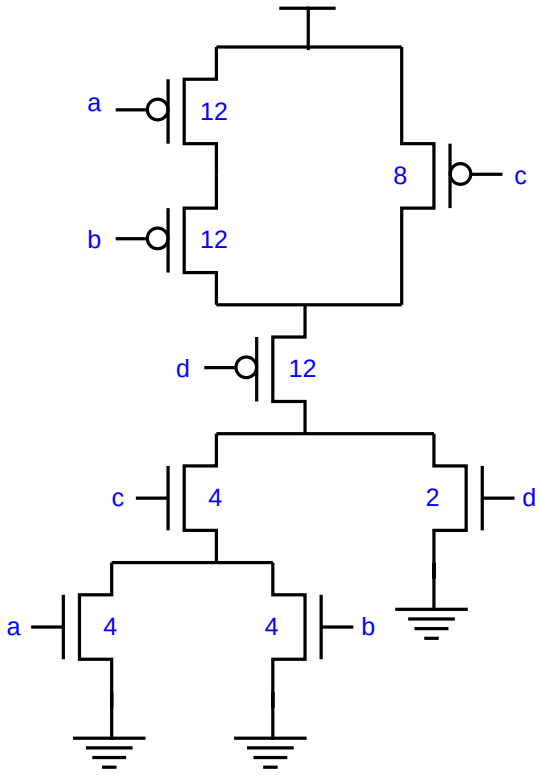
Delay = [ ]

(b) What sequence of inputs would produce the conditions for the best-case delay?

Sequence {ABCDE, ABCDE} = [{ , }]

3. (15 points)

(a) Calculate the logical efforts of the a, b, c and d inputs of the following gate.



a: ☐

b: ☐

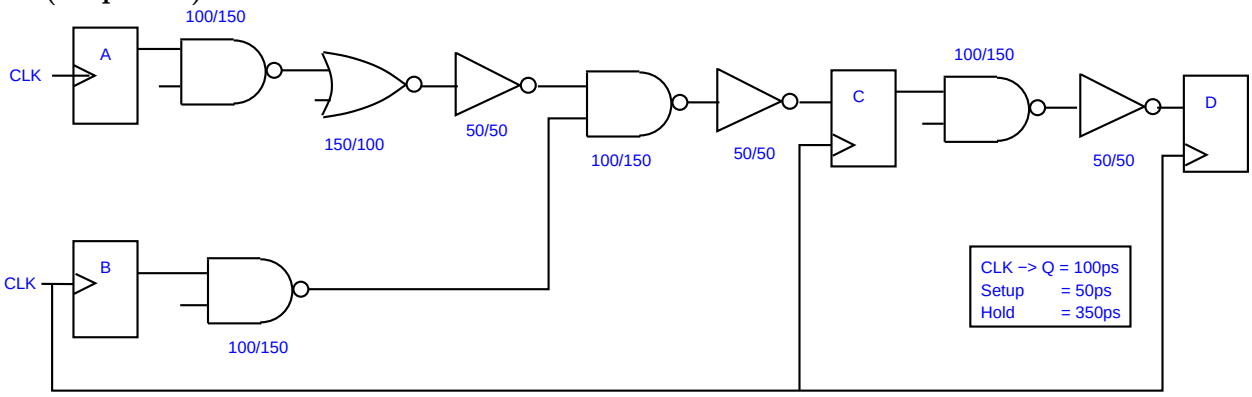
c: ☐

d: ☐

(b) What would be the logical effort of the c input if the pMOS transistor with input of c is sized to 12 for easier layout?

c: ☐

4. (25 points)



(a) Find the worst-case timing paths in the circuit above (the rise/fall times of the gates are give).

From A to C: _____ ps

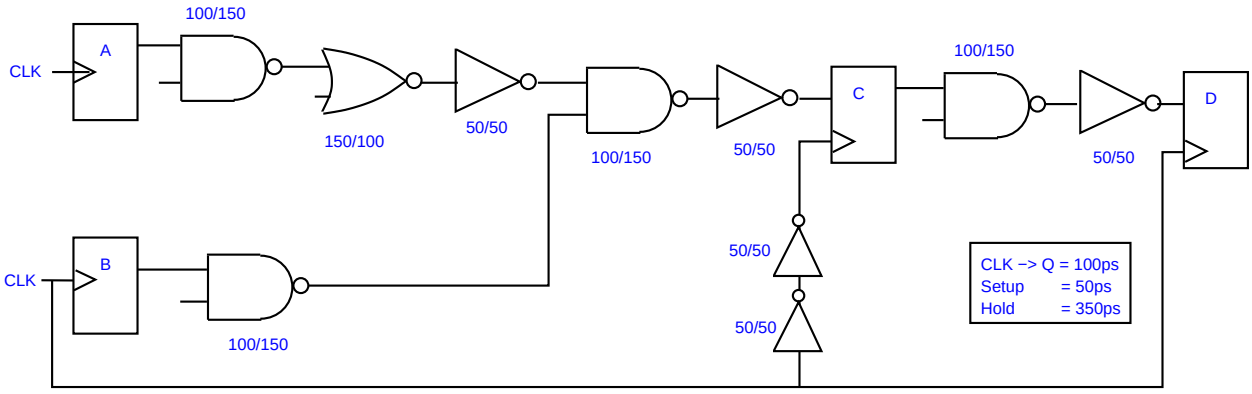
From C to D: _____ ps

(b) What is the maximum frequency at which the circuit can be clocked?

Frequency = _____ MHz

(c) Identify any Hold Time violations in the circuit

The clock is now stretched to balance the two stages.



(d) What is the worst-case timing path and the maximum frequency at which the circuit can now be clocked?

Timing path: _____ ps

Frequency = _____ MHz

(e) Identify any Hold Time violations in the circuit with clock stretching, **and suggest a fix with minimum impact on the operation**.

5. (15 points)

Systems with shared buses require buses with long wires. The portion of power consumed in wires relatively increases with the device scaling. Conventional systems use parallel bus structures which involves a lot of wires leading to decrease in the spacing between the adjacent wires thereby increasing coupling capacitance.

(a) Using the following values for the parameters, Calculate the power in case of a parallel bus.

```
a (switching factor) = 0.5
f (Bus Frequency)    = 400 Mhz
w (Bus width)        = 8
C (Bus Capacitance)  = 300 pF
V (Voltage Swing)    = 1.5 V
```

Power = [ ] milliwatts.

Bus serialization decreases the number of wires, and increases the pitch between the wires. The wider pitch decreases the coupling capacitance of wires ultimately decreasing the power consumption. The serialization degree is the extent to which the bus is serialized (for example, if you are transmitting a Bit pattern 11110000 over 4 wires, the serialization degree would be 2, the factor for increase in frequency for the same throughput).

(b) Now if the above parallel bus is serialized, using the following parameters, calculate the power of the serial bus assuming the same throughput as the parallel bus.

```
a (switching factor)    = 0.5
f (Bus Frequency)        = 400 Mhz
w (number of wires)      = 4
C (Bus Capacitance)      = 250 pF
V (Voltage Swing)        = 1.5 V
```

Power = [ ] milliwatts.

Consider a case where one bit pattern is '11000010' and the next bit pattern is '11000011'.

(c) What is the energy consumed during the the second pattern (the second clock) for the parallel bus, assuming that if a bit does not change, there is no energy consumed.

Energy = [ ] millijoules.

(d) For a serial bus with serialization degree of 2, what is the energy consumed for the second pattern (note that this would be for the third and fourth clocks).

Energy = [ ] millijoules.

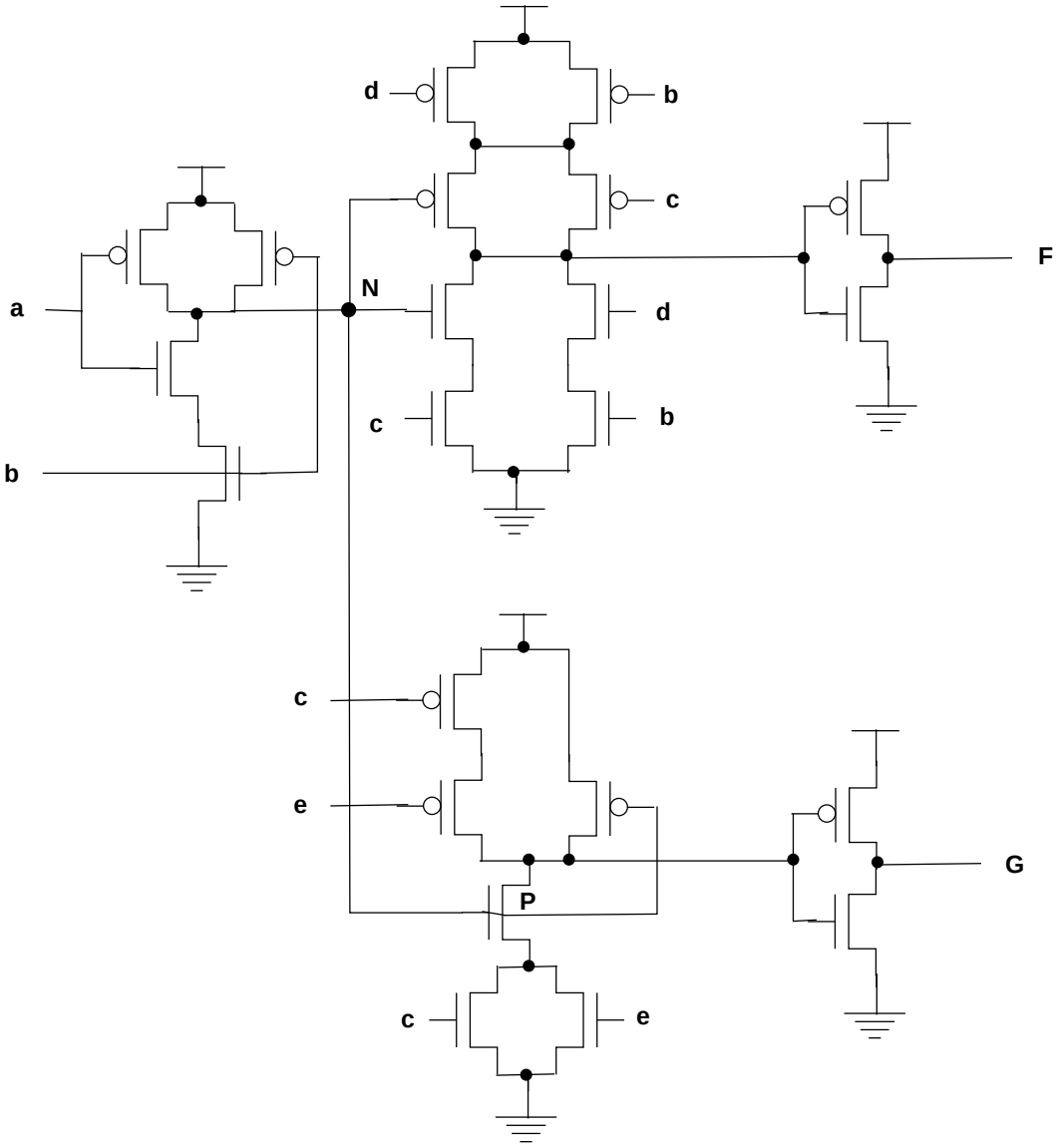
6. (10 points)

(a) Find a test for the node N stuck-at-0 in the circuit below.

Test: abcde = [ ]

(b) Find the sequence of two tests which would detect that the nMOS transistor, labeled P, is slow to turn on.

Test: {abcde, abcde} = [{ , }]



EE360R	**Computer-Aided IC Design**	**J. Abraham**
Spring 2002	**FINAL EXAM.**	**May 16, 2002**

Name: _____

Open Book, Open Notes. Time Limit: 3 hours (pace yourself). Check for 10 pages in exam.

Write all your answers in the spaces/boxes provided.

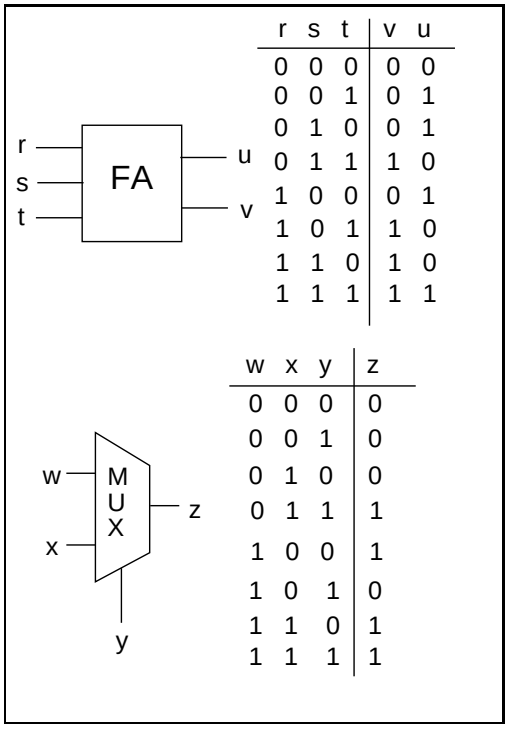
Show any calculations in these pages using the back of the pages if needed. State clearly any assumptions made.

PROBLEM	MAX	POINTS
1	15	
2	15	
3	20	
4	20	
5	15	
6	15	
TOTAL	100	

1. (a) (5 points) Design a transistor level circuit realization of the following function using **N-P Dynamic Logic**. Assume you have two non-overlapping clocks ϕ and $\overline{\phi}$ and the restriction that you cannot use more than **three** transistors in series (including clocking transistors) in any path from the output node to power or ground. You have only the **uncomplemented inputs** A, B, C, D, E, F, G available.

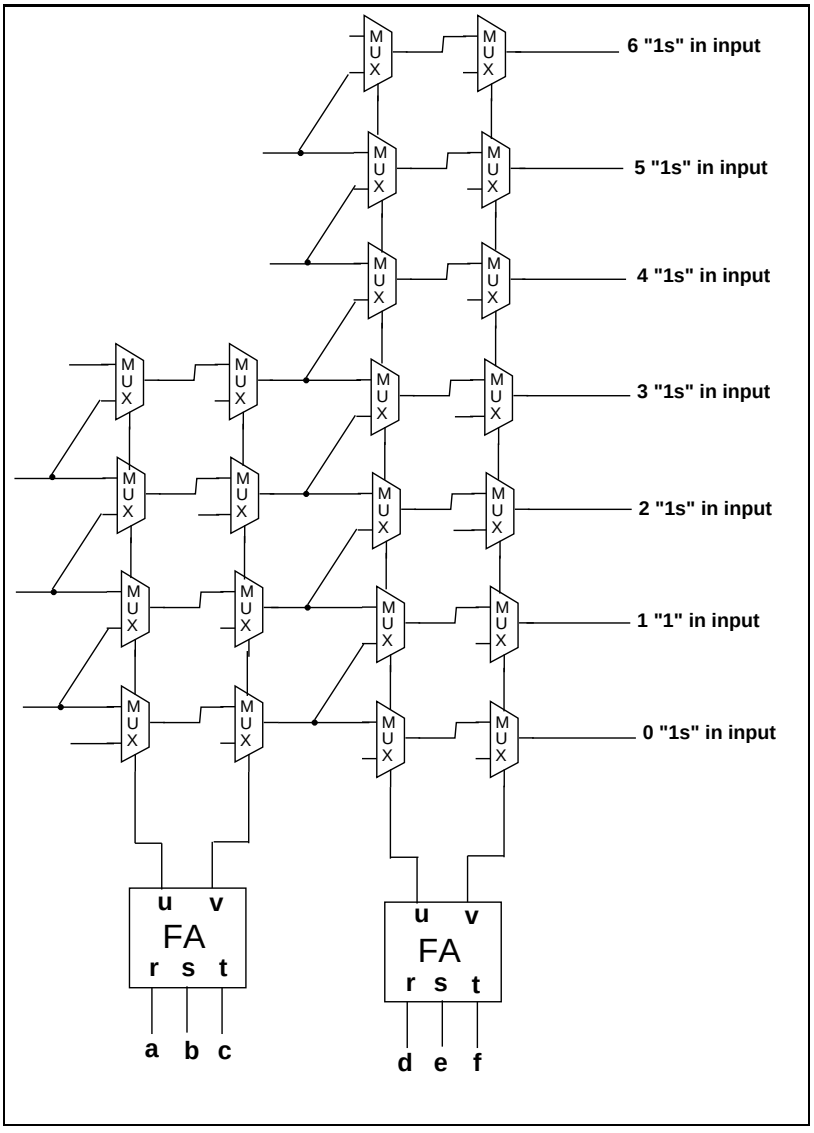
$(A \cdot B + C \cdot D) \cdot (E + G) \cdot (F + G)$

1. (b) (10 points) A circuit which counts the number of 1s in the input is implemented using two cells, a full adder (FA) and a multiplexer (MUX). The cells, their truth table and the partially designed are shown below.



r	s	t	v	u
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

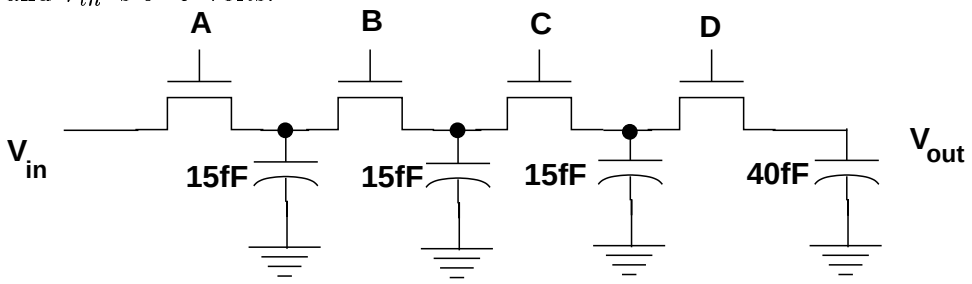
w	x	y	z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



Complete the interconnections in the figure on the right so that the outputs are high depending on the number of 1s in the input, (a b c d e f), as labeled in the figure. **Do not add any other cells or logic. You may tie the free inputs to the MUX to Vdd or Gnd.**

2. (a) (5 points)

Four n-channel transistors in a pass transistor chain are shown below. The input voltage, V_{in} is set to 3 Volts, and V_{tn} is 0.25 Volts.



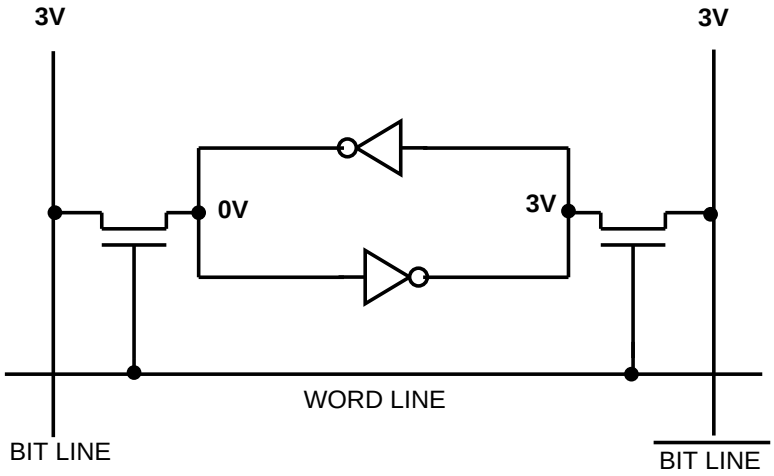
Initially, V_{out} is 0 Volts, and ABCD = 1110 (Logic 1 $\equiv$ 3 Volts, Logic 0 $\equiv$ 0 Volts).

Then, the inputs are switched to ABCD = 0111.

Find the final value of V_{out} = ☐

2. (b) (10 points)

The figure below is a one bit of a static RAM array. The gate capacitance of an n-channel transistor in the cell is 0.02pF and that of a p-channel transistor is 0.03pF. The source/drain capacitance of an n-channel transistor is 0.001pF and for a p-channel transistor is 0.002pF. The routing capacitance on the bit lines is equal to that of an n-channel transistor per cell.

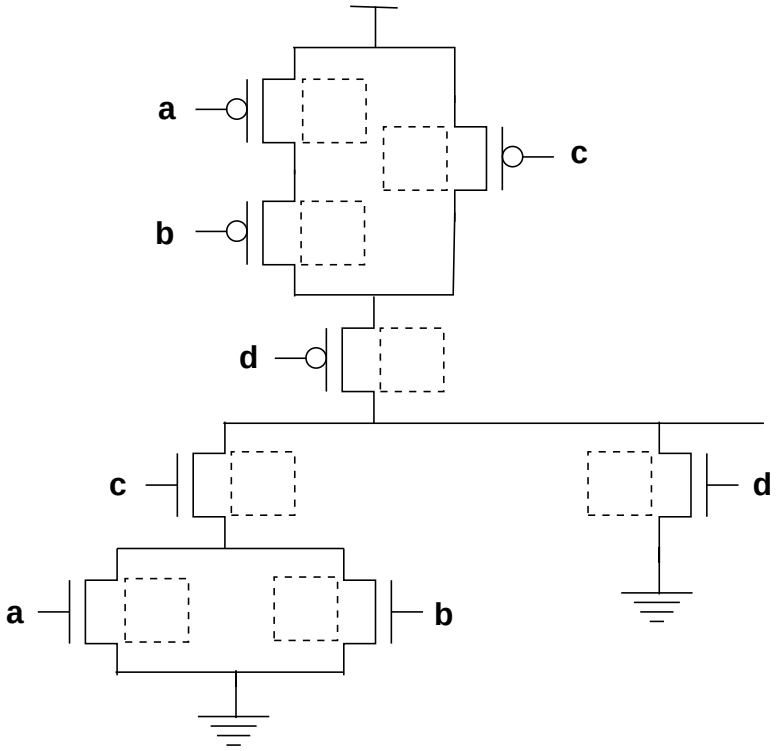


Consider an array with 32 words. Suppose the WORD line is initially 0, and the BIT and $\overline{BIT}$ lines are precharged to 3 Volts, as shown in the figure. When the WORD line is turned on (for a READ), what will be the voltage on the BIT line?

BIT LINE Voltage (just after WORD line on)= ☐

3. (a) (5 points)

Size the following complex gate so that it has the drive strength of an equivalent inverter with PW = 12 and NW = 5.

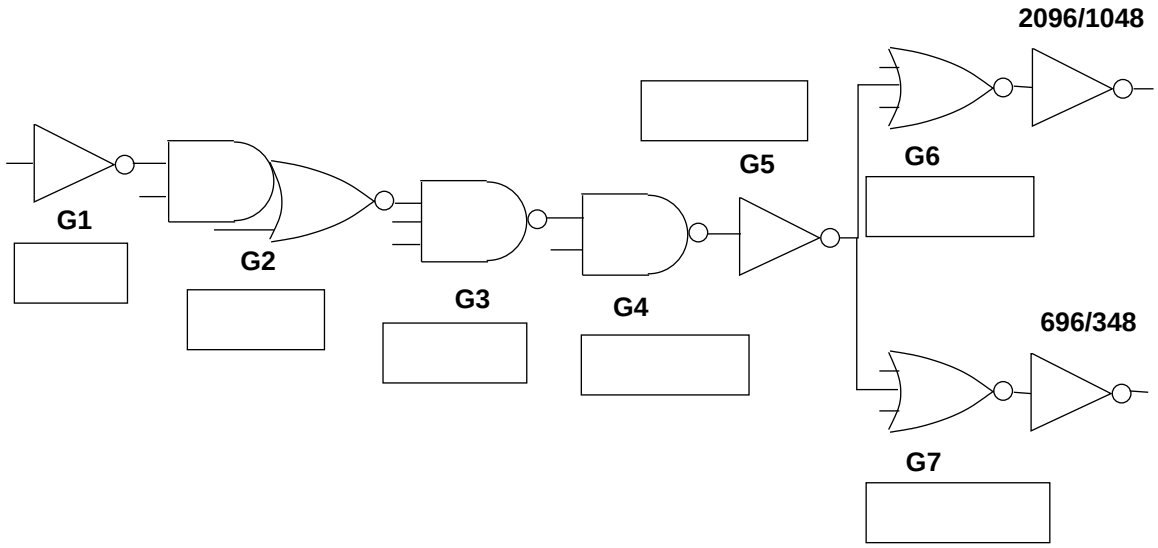


3. (b) (15 points)

Size the following paths using:

Stage ratio = 4
P:N = 2:1

Stay as close as possible to the above ratios.

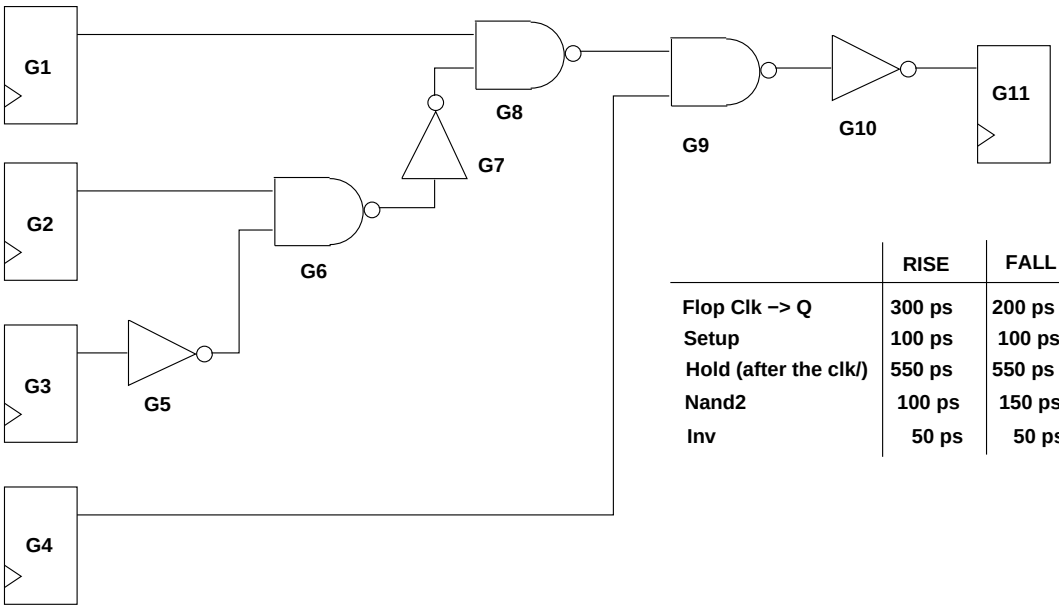


4. (a) (15 points)

Identify if there are any hold time problems from the source flops (G1, G2, G3 and G4) to G11 in the following circuit. Sum the delays along the paths and show the amount of the violation under "Fail" (a negative number indicates that there is no hold-time violation.

Use the delays from the table below.

If there is any violation, show the fix on the circuit below (by using chains of inverters in the appropriate path). The additional inverters should impact as little of the circuit delay as possible.



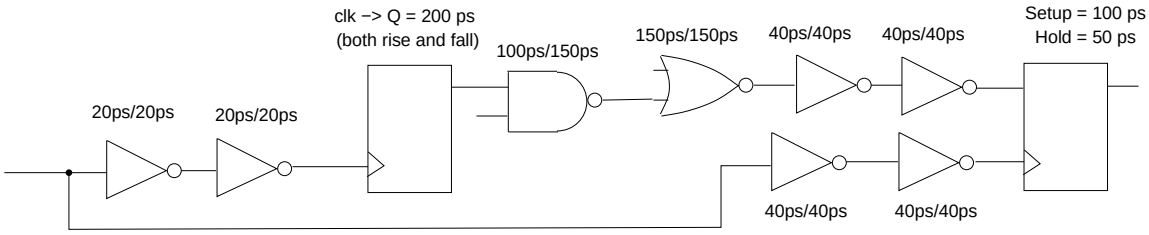
	RISE	FALL
Flop Clk –> Q	300 ps	200 ps
Setup	100 ps	100 ps
Hold (after the clk/)	550 ps	550 ps
Nand2	100 ps	150 ps
Inv	50 ps	50 ps

Path	RISE	Fail?	FALL	Fail?
G1 → G11				
G2 → G11				
G3 → G11				
G4 → G11				

What is the maximum frequency of operation after fixing any hold-time violation? MHz

4. (b) (5 points)

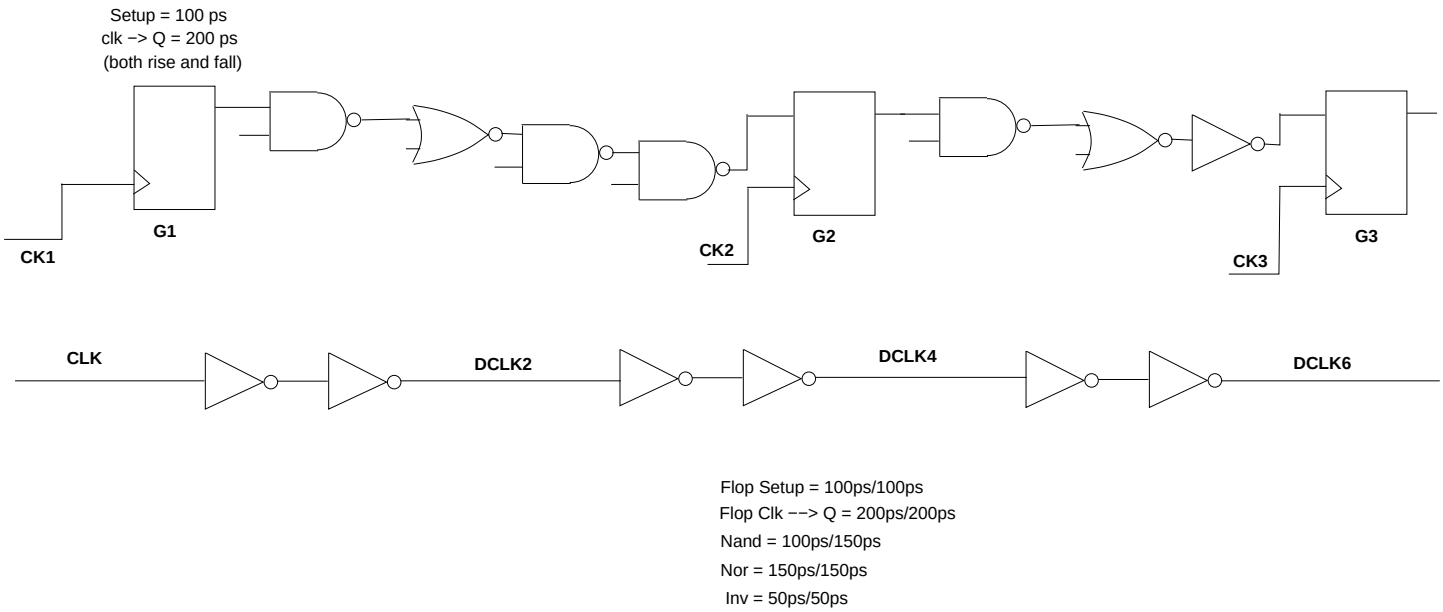
What is the maximum frequency at which the following design can operate (the rise and fall delays of the components as well as the flop parameters are shown in the figure)?



Frequency = MHz

5. (15 points)

A part of a pipelined circuit is shown below. The clock inputs to the three flops are CK1, CK2 and CK3, as shown in the figure.



What is the maximum frequency of operation for this circuit if CK1, CK2 and CK3 are all connected to the clock, CLK?

	MHz

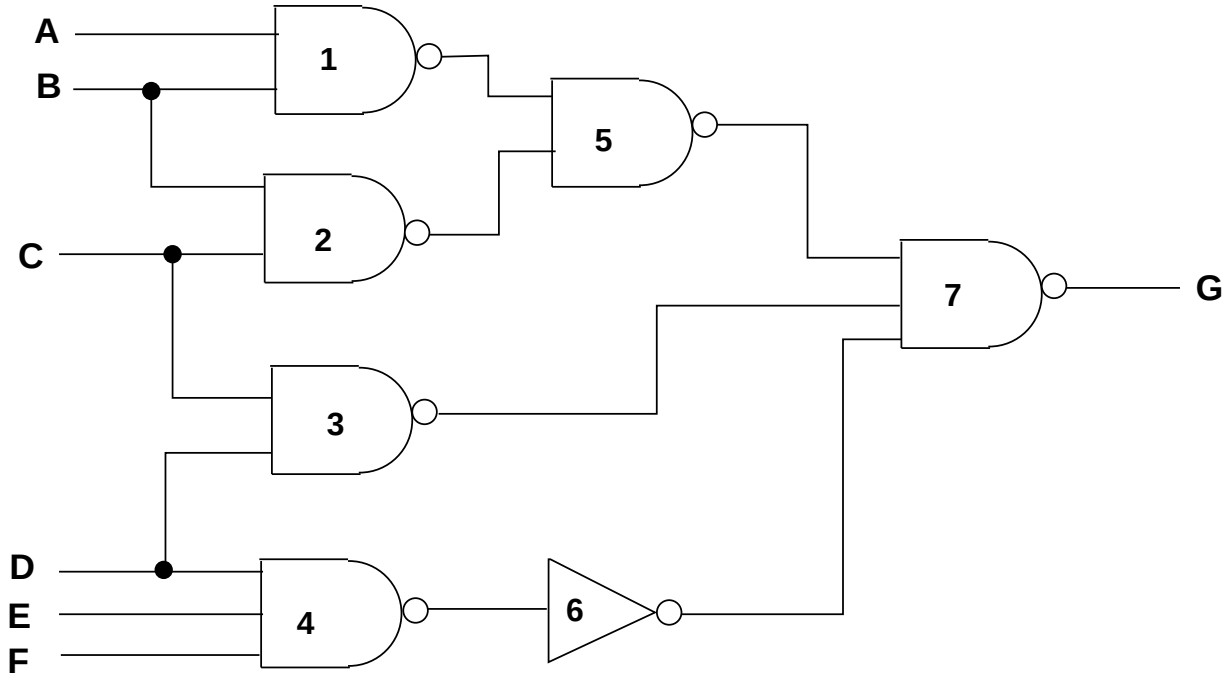
Speed up the operation of the circuit by appropriately clocking CK1, CK2 and CK3. Do this by connecting CK1, DCLK2 or DCLK4 to CK1, CK2 and CK3, so that the design will operate at the maximum frequency.

What is the maximum frequency of operation after rewiring the clock inputs to the flops?

	MHz

6.

This problem deals with finding tests for faults in the circuit below.



(a) (5 points)

Find a test for the line F "stuck at 1"

Test: A B C D E F = ____

(b) (5 points)

Find a test for a fault in the p-channel transistor connected to F which increases its channel resistance so that the output could become slow to rise.

Input 1: A B C D E F =	
Input 2: A B C D E F =	

(c) (5 points)

Find a test for a fault which causes the gate marked "3" to have an increased rise time.

Input 1: A B C D E F =	
Input 2: A B C D E F =	

EE360R | **Computer-Aided IC Design** | **J. Abraham**
Fall 2002 | **FINAL EXAM.** | **December 16, 2002**

Name: _____

Open Book, Open Notes. Time Limit: 3 hours (pace yourself). Check for 7 pages in exam.

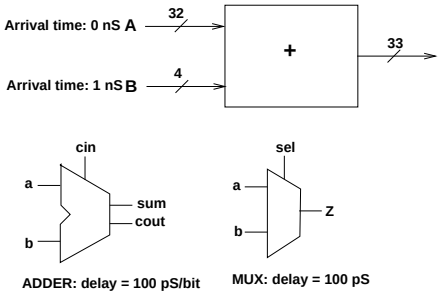
Write all your answers in the spaces/boxes provided.

Show any calculations in these pages using the back of the pages if needed. State clearly any assumptions made.

PROBLEM	MAX	POINTS
1	20	
2	15	
3	15	
4	15	
5	15	
6	20	
TOTAL	100	

1. (20 points)

This problem is to design a fast circuit (+) to add a 32-bit number with a 4-bit number (to produce a 33-bit number). The circuit should be designed with two macros (shown below): an adder macro (adds numbers of a specified bit-width) which produces an adder with a delay of 100 pS/bit, and a multiplexer (which selects from inputs of specified bit width) which has a delay of 100 pS (independent of the size). The arrival times of the input signals to the circuit are also shown below.



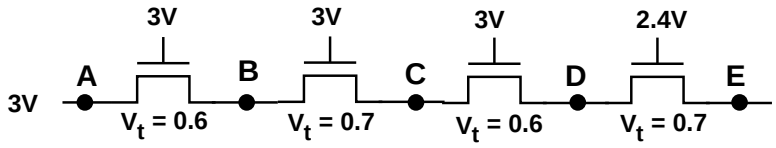
Design the circuits for the following specifications, and show the interconnection of the modules below to meet the specs. Make sure that the you show the appropriate bits for the inputs to the modules. (You may not need to use all the modules for a solution, or you may need to add additional modules. Do NOT add any other logic other than the two modules.)

(a) Design a circuit to complete the addition in $\leq$ 3 nS.

(a) Design a circuit to complete the addition in $\leq$ 2 nS.

2. (a) (5 points)

Write down the voltages at the nodes B, C, D and E in the circuit below, given the voltages at A and the gate inputs of the transistors. Each transistor is labeled with its V_t value.



Voltage at B = ☐

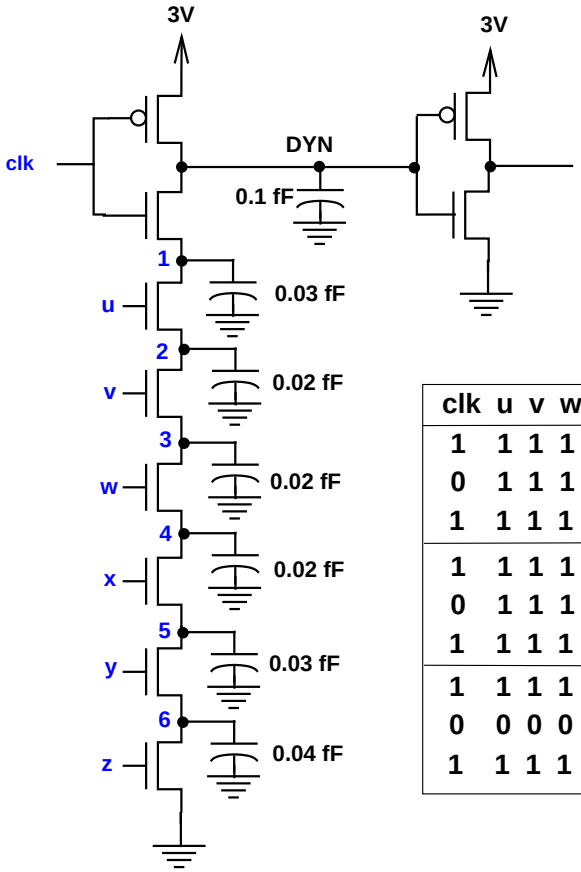
Voltage at C = ☐

Voltage at D = ☐

Voltage at E = ☐

2. (b) (15 points)

Calculate the voltages on the node **DYN** in the circuit below following the various initial conditions given.



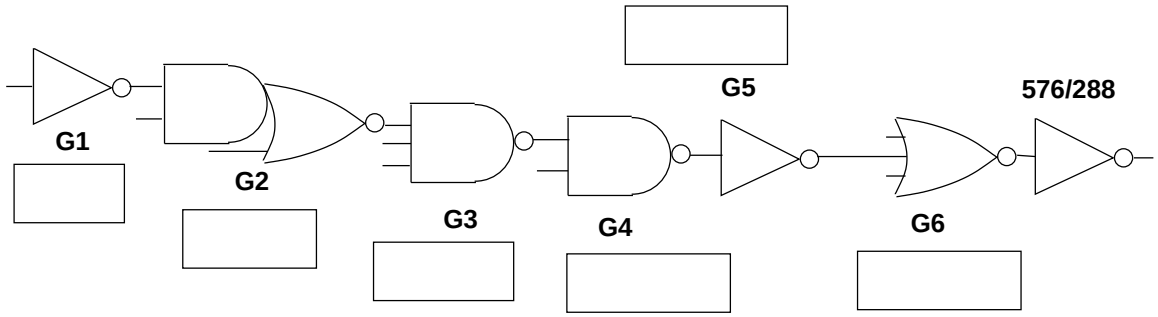
clk	u	v	w	x	y	z	DYN
1	1	1	1	1	1	1	0 Volts
0	1	1	1	1	1	1	
1	1	1	1	1	1	0	
1	1	1	1	1	1	0	3 Volts
0	1	1	1	1	1	0	
1	1	1	1	1	1	0	
1	1	1	1	1	1	1	0 Volts
0	0	0	0	1	1	1	
1	1	1	1	0	0	0	

3. (15 points)

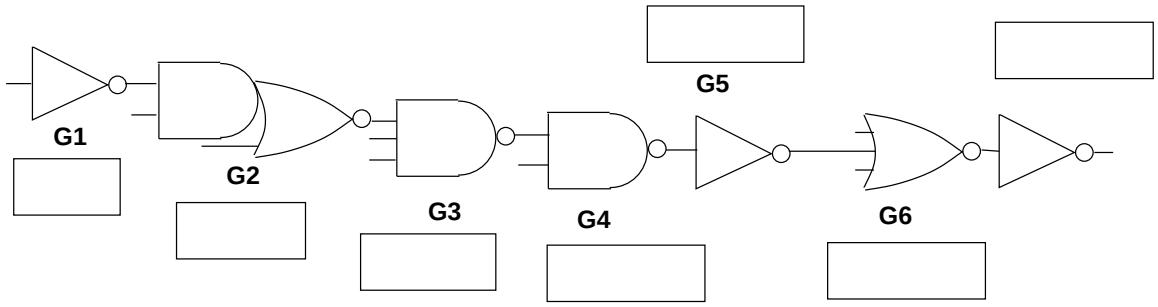
Size the following paths using:

Stage ratio = 3
P:N = 2:1

Stay as close as possible to the above ratios.



Using the sizing you found for G4, size its loads and drivers to a P:N ratio of 3:1.

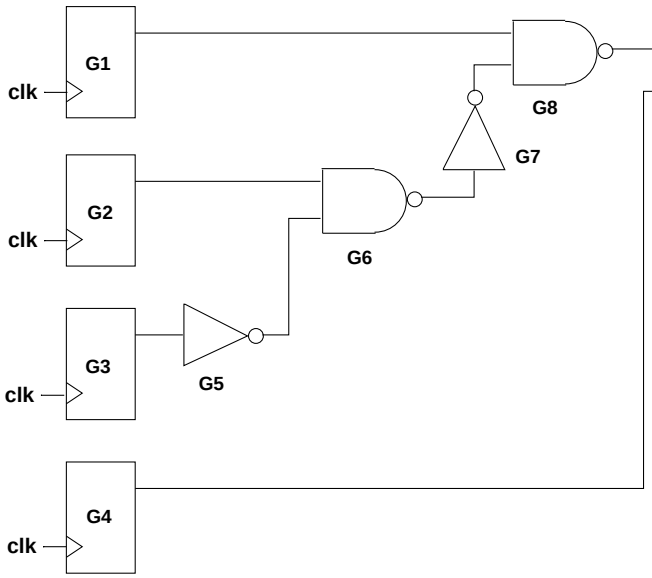


4. (15 points)

Identify if there are any hold time problems from the source flops (G1, G2, G3 and G4) to G11 in the following circuit. Sum the delays along the paths and show the amount of the violation under "Fail" (a negative number indicates that there is no hold-time violation.

Use the delays from the table below.

If there is any violation, show the fix on the circuit below (by using chains of inverters in the appropriate path). The additional inverters should impact as little of the circuit delay as possible.

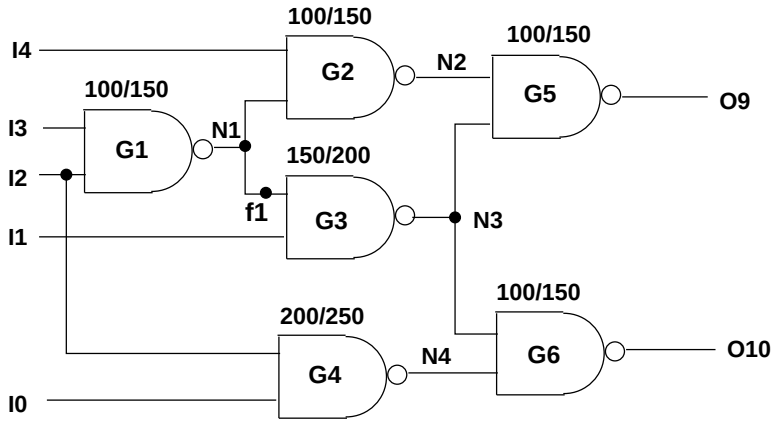


	RISE	FALL
Flop Clk –> Q	300 ps	200 ps
Setup	150 ps	150 ps
Hold (after the clk/)	450 ps	450 ps
Nand2	100 ps	150 ps
Inv	50 ps	50 ps

Path	RISE at G11 input	Fail?	FALL at G11 input	Fail?
G1 → G11				
G2 → G11				
G3 → G11				
G4 → G11				

What is the maximum frequency of operation after fixing any hold-time violation? MHz

5. (15 points)



(a) Find the three longest paths from some input to one of the outputs in the circuit above (gate rise/fall times are shown). Indicate, for each path,

Input, rising/falling, node1, node2, ... , output (Example: I2 (rising), N4, O10)

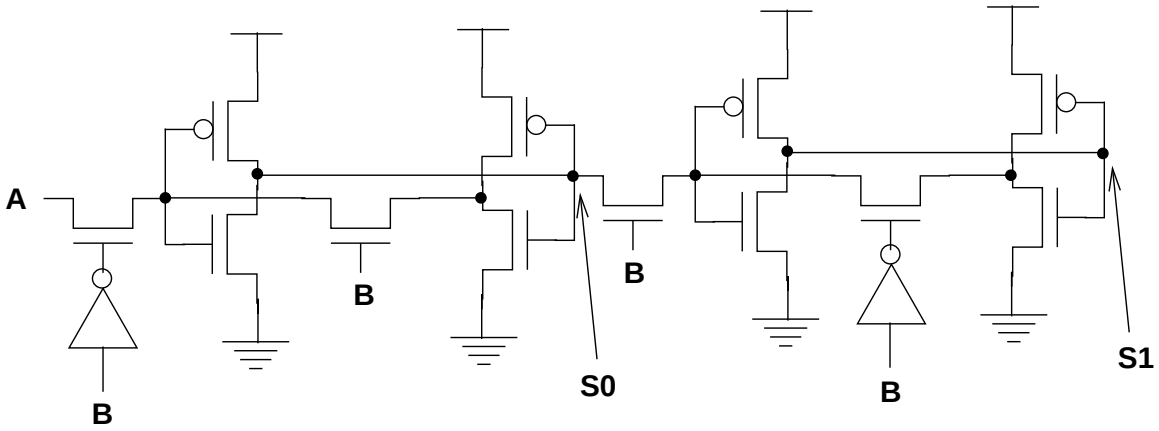
(b) Find a test for the node f1 stuck-at-1.

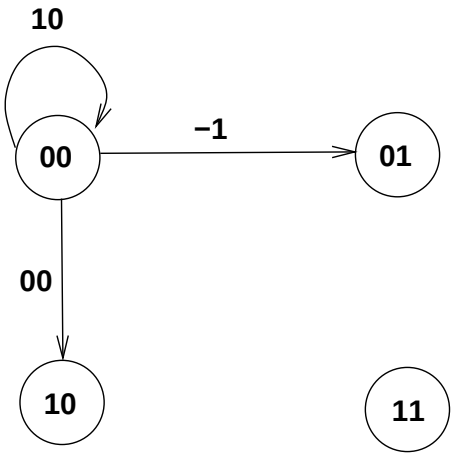
(c) Find a test for the node N4 stuck-at-1.

(d) Find a test for the n-channel transistor connected to the I2 input on gate G1 being slow to turn on.

6. (20 points)

Complete the state transition diagram for the circuit below ("-" represents a "don't-care").





State: S0 S1

Transition: AB

EE360R **Computer-Aided IC Design** **J. Abraham**
Fall 2003 **FINAL EXAM.** **December 10, 2003**

Name: Student, U. G.

Signature: _____

Open Book, Open Notes. Time Limit: 180 minutes (pace yourself). Check for 8 pages in exam.

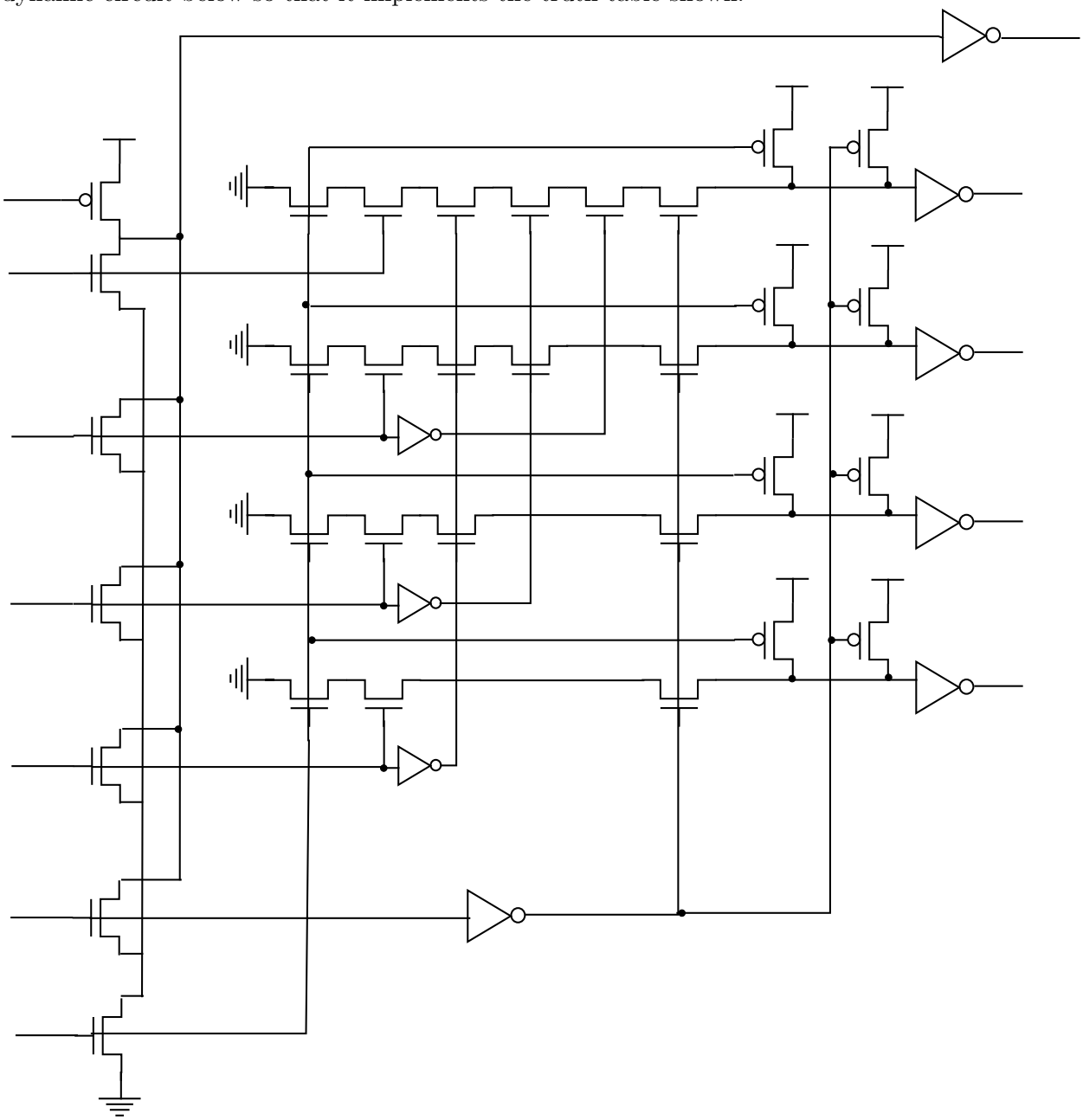
Write all your answers in the spaces/boxes provided.

Show any calculations in these pages using the back of the pages if needed. State clearly any assumptions made. You will not receive partial credit if you don't show your steps toward the solution.

PROBLEM	MAX	POINTS
1	15	
2	15	
3	10	
4	15	
5	10	
6	20	
7	15	
TOTAL	100	

1. (15 points)

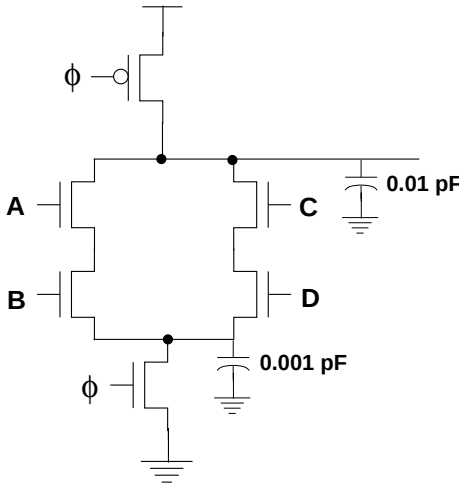
Label the clocks (ϕ or $\overline{\phi}$), inputs (Pin, D0, D1, D2, D3) and outputs (Pout, P0, P1, P2, P3) of the dynamic circuit below so that it implements the truth table shown.



Pin	D0	D1	D2	D3	P0	P1	P2	P3	Pout
1	X	X	X	X	0	0	0	0	1
0	1	X	X	X	1	0	0	0	1
0	0	1	X	X	0	1	0	0	1
0	0	0	1	X	0	0	1	0	1
0	0	0	0	1	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0

2. (15 points)

The following AND-OR-INVERT domino circuit is implemented in a technology with a V_{dd} of 2 Volts and a V_t of 0.5 Volts for the n-channel transistors. The n-channel transistors have on-resistances of 5 $K\Omega$. The source/drain capacitance of an n-channel transistor is 0.001 pF and that of a p-channel transistor is 0.002 pF. The routing capacitances for interconnections are lumped at the nodes as shown.



When the circuit goes through the precharge/evaluate cycle, the capacitors (at the output as well as the internal nodes) are charged and discharged depending on the values on A, B, C and D. Therefore, the delay depends on the input values which would charge up internal nodes.

(i) Find the input *sequences* which will result in the **worst-case** falling delay

Step	ϕ	A	B	C	D
1					
2					
3					

(i) Find the input *sequences* which will result in the **best-case** falling delay

Step	ϕ	A	B	C	D
1					
2					
3					

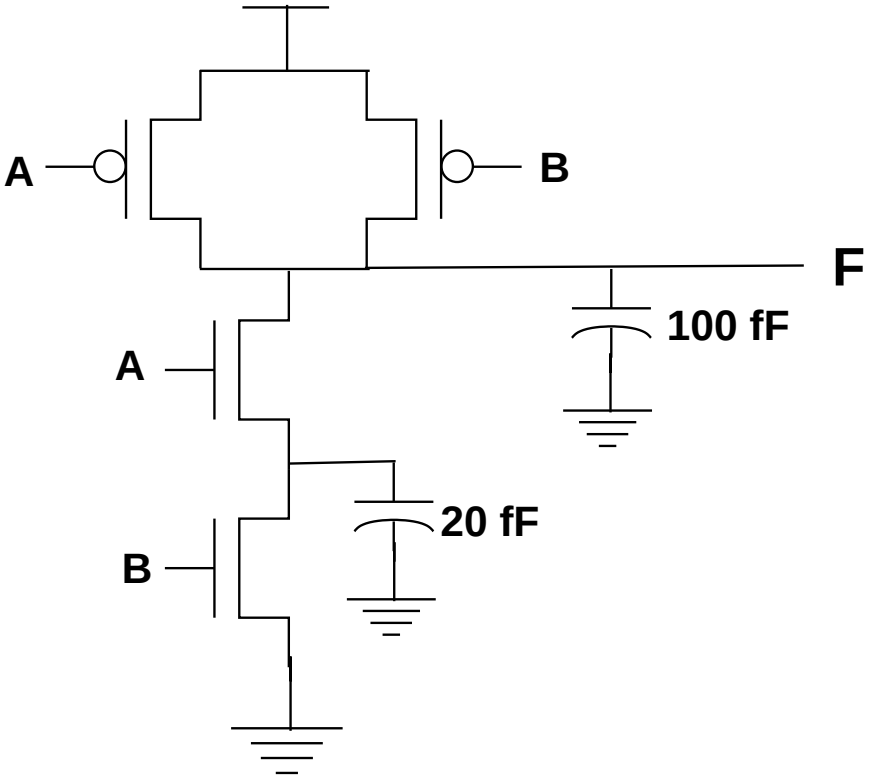
(iii) Using the Elmore delay approach, find the fall times for the following cases, when ϕ goes from 0 to 1; assume internal capacitances are all charged (for the worst case delay).

ABCD = 0011

ABCD = 0111

3. (10 points)

The NAND gate below is implemented in a 0.18 μ technology with a power supply of 2 Volts. The P-channel transistors have on-resistances of 100 Ω, V_t = -0.3 Volts, and the source and drain capacitances are each 50 fF. The N-channel transistors have on-resistances of 50 Ω, V_t = 0.3 Volts, and each source and drain capacitance is 25 fF. The load and parasitic capacitances are shown in the figure.



Initially, A = B = 1.

Now, the input is changed to A = 0, B = 0. What is the energy dissipated in this transition?

Energy = ☐

What is the energy dissipated if the *next* input is A = 1, B = 1.

Energy = ☐

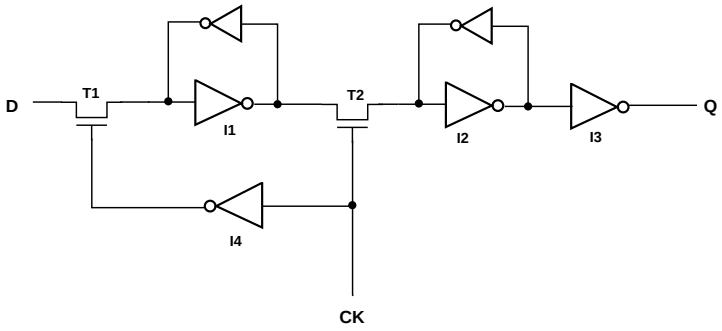
Finally, the input is changed to A = 1, B = 0 (as the *next* input).

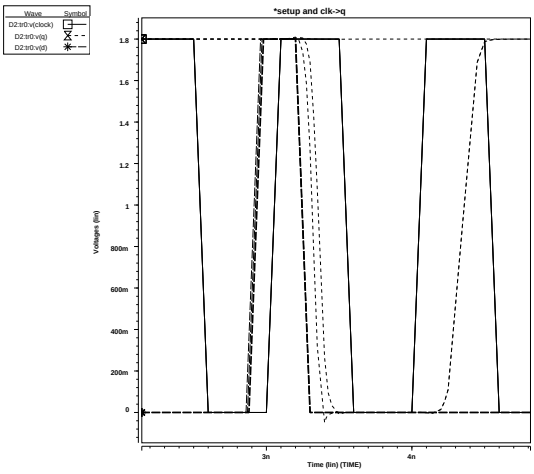
What is the energy dissipated for this transition?

Energy = ☐

4. (15 points)

The flop below has been characterized using a circuit simulator and the simulation outputs are also shown. First, find the approximate values for the flop characteristics in terms of the delays of the transistors and inverters (T2, I3, etc.). Then, from the simulation outputs, determine the values for the flop parameters.



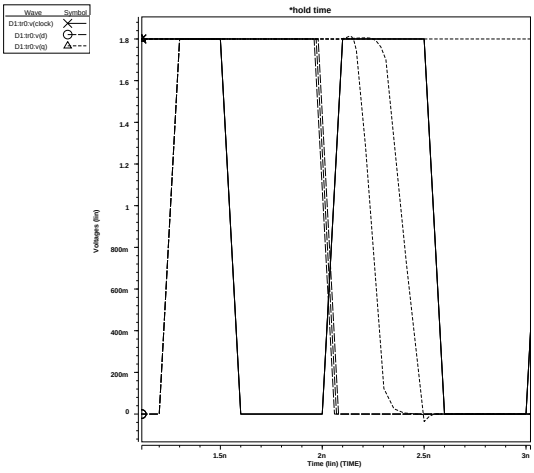


Approximate:

Setup Time = ____

Clock-to-Q delay = ____

Hold Time = ____



From simulation:

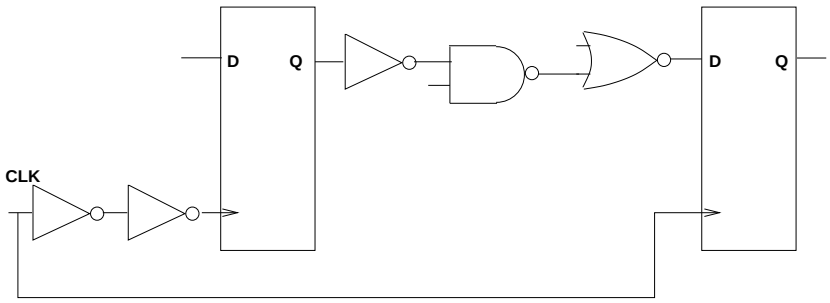
Setup Time = ____

Clock-to-Q delay = ____

Hold Time = ____

5. (10 points)

Find the maximum frequency at which the following design can operate.



Delay	Rise	Fall
CLK –> Q	300 ps	200 ps
Inv	200 ps	200 ps
Nand	250 ps	250 ps
Nor	300 ps	200 ps
Setup time at D	100 ps	50 ps

Calculate the delays (including Clock-to-Q and Setup times):

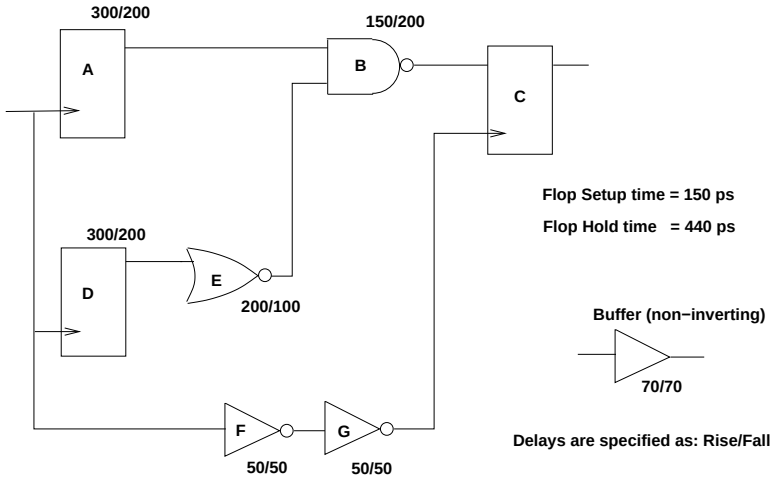
Rise Delay =

Fall Delay =

Cycle Time Needed =

Frequency =

6. (a) (5 points) Find the maximum cycle time at which the following circuit can operate.



A/ –> B\ –> C =

A\ –> B/ –> C =

D/ –> E\ –> B/ –> C =

D\ –> E/ –> B\ –>C =

Maximum cycle time =

6. (b) (10 points) Perform a hold time analysis and identify the failing paths.

A/ –> B\ –> C =

A\ –> B/ –> C =

D/ –> E\ –> B/ –> C =

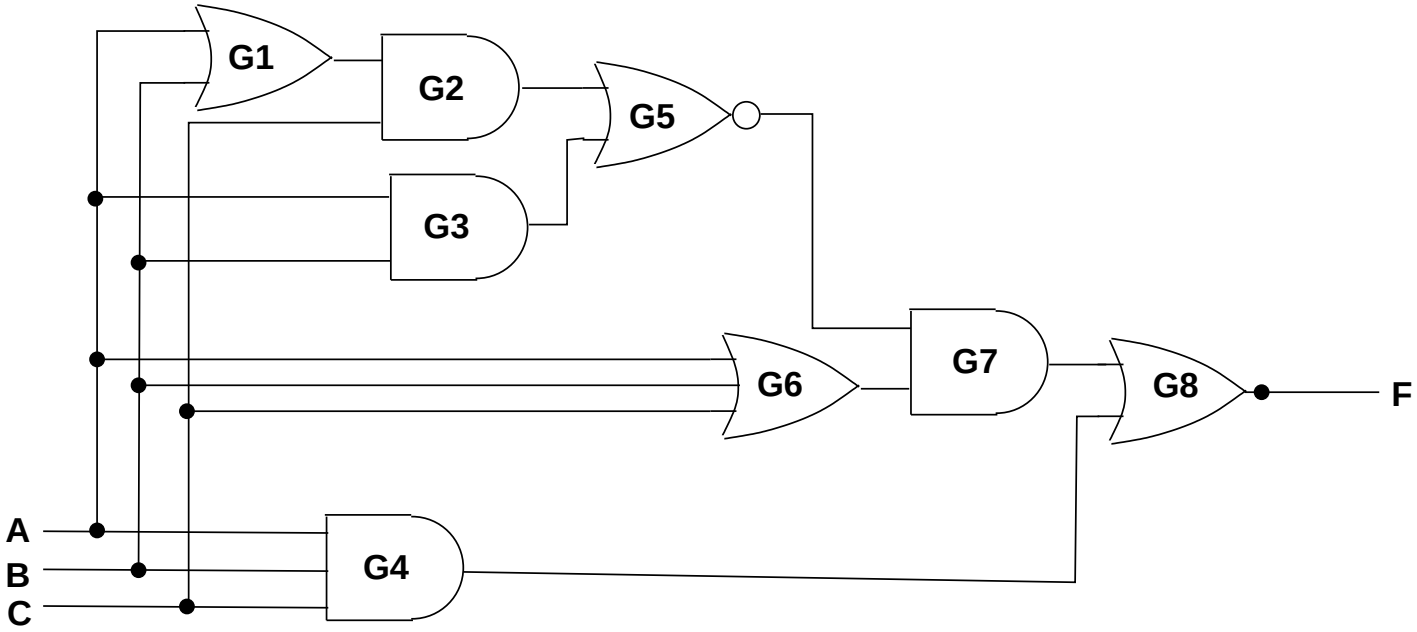
D\ –> E/ –> B\ –>C =

Fix the failures so that the maximum cycle time is either not affected or affected minimally. Use buffers to fix the hold time problems.

Fix is

6. (c) (5 points) New maximum cycle time after the fix =

7. (15 points)



Find a test for the output of gate G3 stuck at 0

Test: A B C =

Find a test for the longest path delay in the circuit (assume gate delays are all approximately equal) by launching a transition (0 - 1) on input A.

Test: A B C =

Find a test for the n-channel transistor of gate G6 connected to B having abnormal resistance (making it slower).

Test: A B C =