EE382M VLSI I — J. Abraham

Fall 2010 — Outline Solution for Exam. I — October 11, 2010

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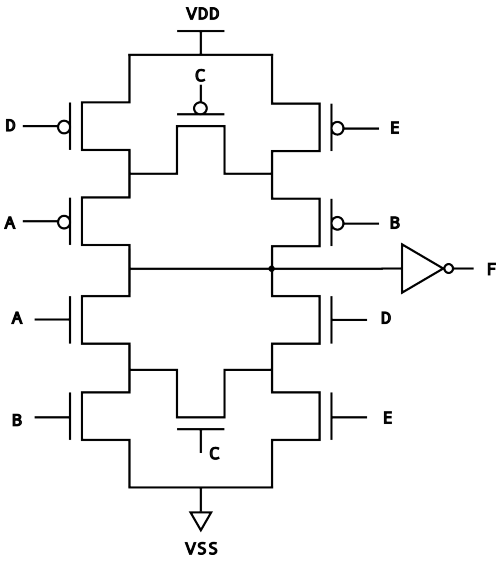
1. Function F implemented by the circuit.



[c] $F = A \cdot (B + C \cdot E) + D \cdot (E + B \cdot C)$

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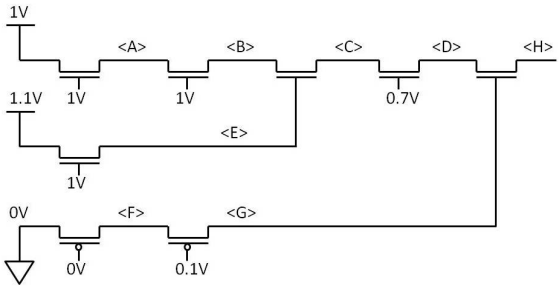
2. Find the voltage at node H. Assume V_{thn}=0.2V, $|V_{thp}|$=0.3V.



0.2 V

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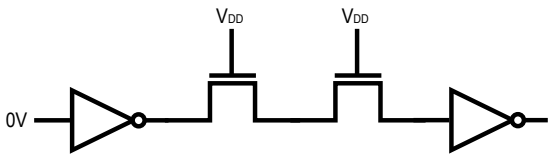
3. Consider the figure below where VDD is 1.3V. The minimum HIGH output voltage of inverters, V_{OH}, is 1V and threshold voltage of an nMOS transistor is 0.45V. What is the minimum noise margin to make it operate correctly? (Assume there is no noise.)



0.2V

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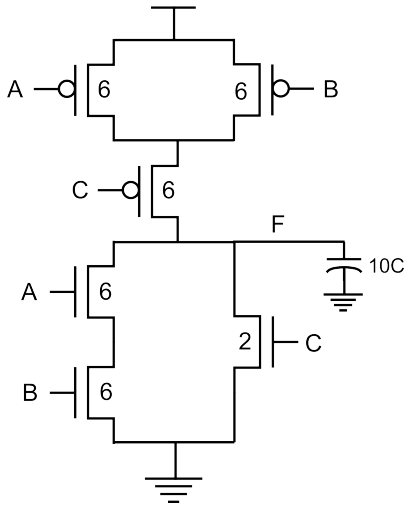
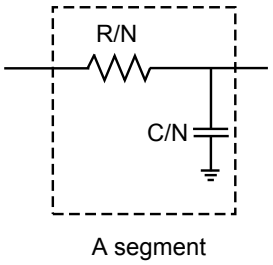
4. The rise and fall delays of the circuit in the figure on right for a given input would depend on whether the previous input had charged or discharged the intermediate nodes.

Elmore delay calculation taking into account the differences in delay with the charge on an internal node.
Worst-case fall delay for the circuit (for a single input changing): 18RC
Best-case fall delay for the circuit (for a single input changing, and only one path from power or ground to the output): 12RC
Sequence of inputs (ABC) which would cause the worst-case fall delay (for a single input changing): 100 → 101
Sequence of inputs (ABC) which would cause the best-case fall delay (for a single input changing, and only one path from power or ground to the output): 010 → 011
Sequence of inputs (ABC) which would cause the worst-case rise delay (for a single input changing): 110 → 100



5.

Wire with total length of L partitioned into N identical segments, each with a length of L/N.



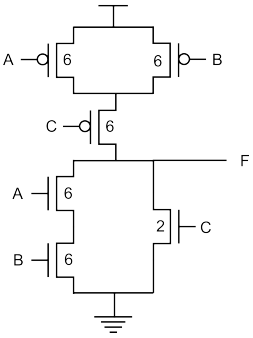
Elmore delay of the wire in terms of R, C and N:

$$\sum_{n=1}^{N}\left(\frac{nR}{N}\right)\frac{C}{N}=\frac{RC}{2}\left(1+\frac{1}{N}\right)$$

Asymptotic delay as the number of segments is increased:

$$\frac{RC}{2}$$

6.



Logical effort for input A: 24/9 Rising, 12/9 Falling

Logical effort for input B: 24/9 Rising, 12/9 Falling

Logical effort for input C: 16/9 Rising, 8/6 Falling

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7. The critical path in a module goes through four 3-input NAND gates. Internal fanouts result in a branching factor of 3. The gates are sized for a stage delay ($\hat{f}$) of 3.5.

If the input capacitance of the critical path is 3C, what is the output capacitance that is driven at the end of the path? 19.45C

What is the delay of the path? 26τ

What would be the input capacitance of the last NAND gate in the path? 9.26C

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8. A ring oscillator is made up of 15 inverters in a 65nm technology with a supply voltage of 1 V. Each inverter is minimum sized (2:1). The FO4 inverter delay for this technology is 30 ps. The gate capacitance is 2fF/μm.

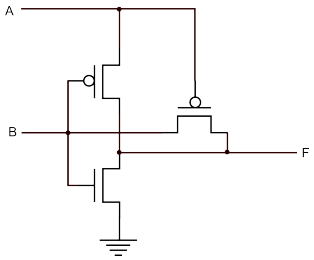
What is the frequency of oscillation? 2.778 GHz

EE360R, Computer-Aided IC Design — J. Abraham

Fall 2011 — Outline Solution to Exam. I — September 28, 2011

Name:

1. Identify the function F implemented by the CMOS circuit (with a reasonable assumption regarding logic levels depending on voltages).



$F = \overline{A \cdot B + \overline{A} \cdot \overline{B}}$

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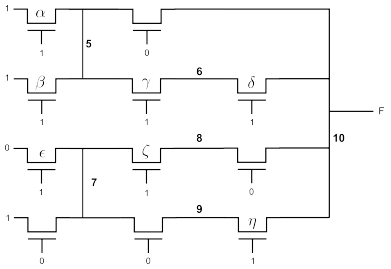
2. The circuit is implemented in a technology with $V_{DD} = 1$ V, and with transistors with different threshold voltages identified with Greek letters next to the respective transistor.
The inputs applied to the circuit are also shown; $1 \equiv 1V$ and $0 \equiv 0V$.
Assuming that all the nodes were at 0V initially, fill in the blanks below for consistent threshold and node voltages.



Node 5	0.9V	V_t α	0.1V
Node 6	0.85V	V_t β	0.15V
Node 7	0V	V_t γ	0.15V
Node 8	0V	V_t δ	0.1V
Node 9	0.85V	V_t ϵ	0.1V
Node 10	0.85V	V_t ζ	0.15V
		V_t η	0.15V

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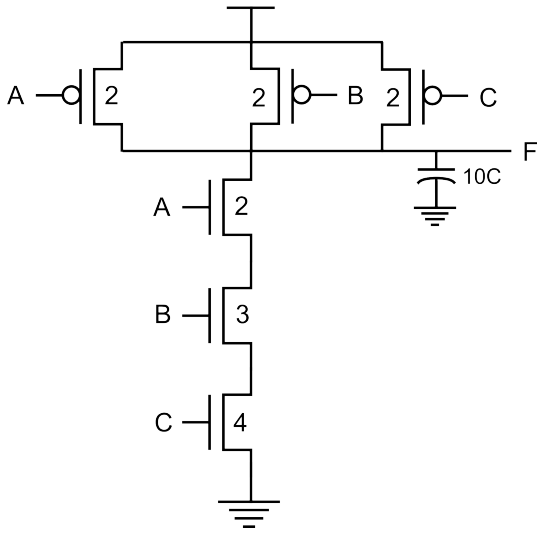
3. The circuit below is an example of a "tapered" gate, where the widths of the transistors are modified in an attempt to improve the delay. Assume that there is no sharing of diffusion (i.e., the diffusion capacitance on a node is the sum of the diffusion capacitances of the transistors connected to the node).



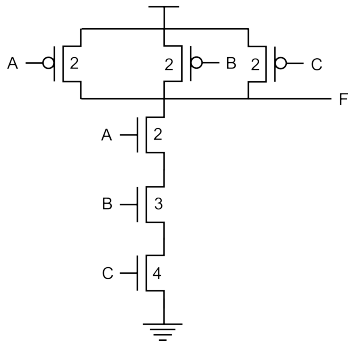
(a) Using the Elmore delay formulation, find the worst case falling delay for this gate.
Delay = 24.2 RC

(b) What is the worst-case falling delay for a "standard" 3-input NAND gate which is sized to have the same currents as a minimum (2:1) inverter?
Delay = 25 RC

(c) If the tapered gate is inserted in a circuit so that the A input has the latest arriving signal, what would be the falling delay?
Delay = 19.5 RC

(d) If the "standard" 3-input NAND gate has the latest arriving signal connected to the inner nMOS transistor (closest to the output), what would be its falling delay?
Delay = 19 RC

4. Find the logical efforts for the inputs A, B, C of the circuit in the figure.



(a) Logical effort of input A = 4/3 (rising output), 13/9 (falling output)

(b) Logical effort of input B = 5/3 (rising output), 65/36 (falling output)

(c) Logical effort of input C = 6/3 (rising output), 13/6 (falling output)

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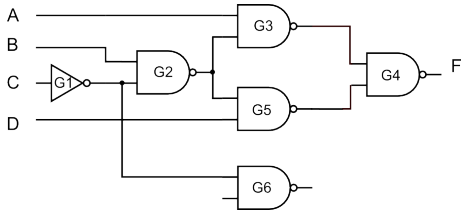
5. The circuit below needs to have a delay of 4.1 FO4 units for the longest path from C to F (through G1-G2-G3-G4). The input to inverter G1 has an input capacitance of 3 units. You may assume that the off-path capacitance is the same as the on-path capacitance for each branch.



Gate	Input Cap.	P	N
Gate G4	16	8	8
Gate G3	6	3	3
Gate G2	5	2	3
Gate G1	3	2	1

(a) If the gates on the path are sized to have the same effort for each state, what would be the stage effort $\hat{f}$ to achieve the above delay for the path?
$\hat{f} = 3.38$ units

(b) What is the maximum capacitance the gate G4 can drive and still keep within the above delay?
$C_L = 41.05$ units

(c) Using the output capacitance value in (b), find the input capacitances for each gate on the path and size the P and N transistors so that the worst-case rise and fall times of the transistors are approximately equal.

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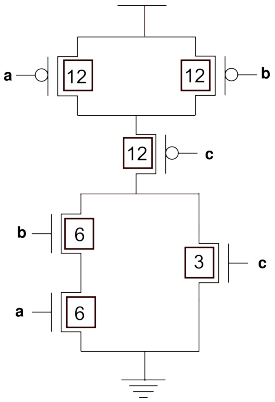
6. The AOI macro is part of a path being analyzed using logical effort. The input capacitances for a, b and c were determined to be 18, 18 and 15, respectively. Find the sizes for each of the transistors to achieve the input capacitances, as well as for the circuit to have the same currents as a 2:1 inverter, and write them in the boxes adjacent to each transistor.



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7. A ring oscillator consisting of 15 minimum-sized (2:1) inverters in a loop, placed on a 45 nm chip, has a measured frequency of 6.41 GHz.

(a) What is the delay of one stage of the ring oscillator? Delay = 5.2 ps

(b) If the ring oscillator performance is assumed to be representative of the performance of the transistors on the chip, what would be the FO4 delay for the inverters on this particular chip? FO4 Delay = 13 ps

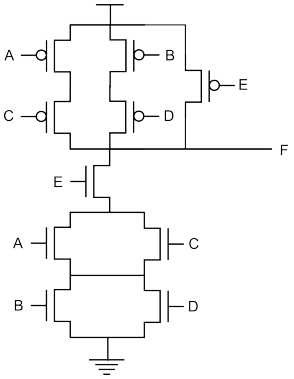
VLSI Design — J. Abraham

Fall 2015 — Outline Solution for Exam. I — October 7, 2015

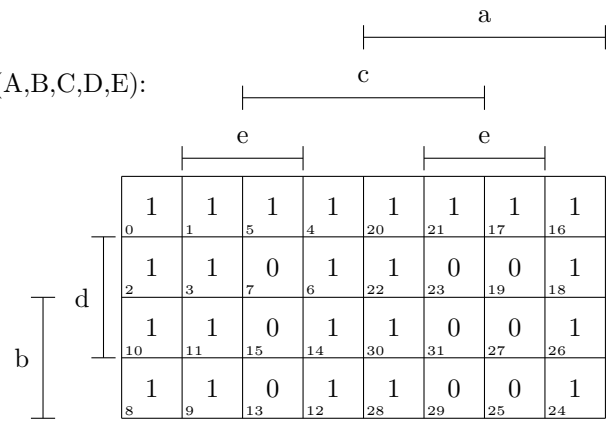
Exam, 1.

1.

Fill in the Karnaugh map to represent the Boolean function implemented by the pass-transistor circuit below.

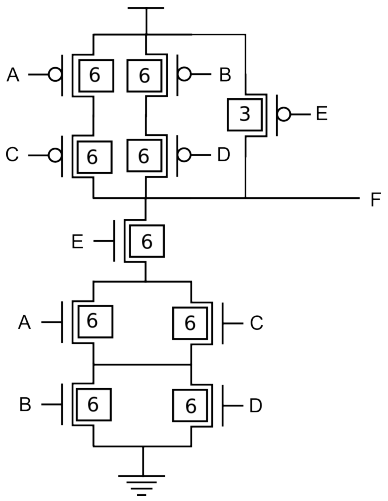


F(A,B,C,D,E):



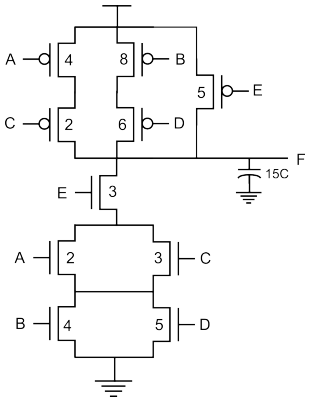
2.

Size the transistors in the circuit on the right so that the current through any single path in the P and N network is the same as that of an inverter with widths of P=3, N=2.



3.

Use the Elmore Delay formulation to calculate the (worst-case) delay for the output transitions in the circuit below, for the following inputs.



(a) ABCDE = 10001

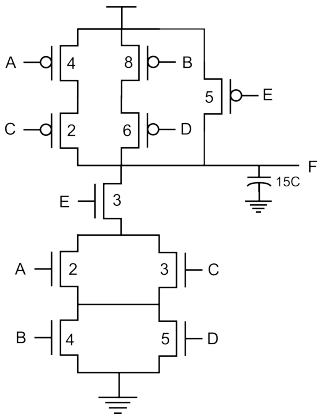
Delay = 37.91 RC

(b) ABCDE = 11001

Delay = 66.75 RC

4.

Find the logical efforts of the following inputs in the CMOS circuit below.



(a) Logical Effort of Input A: Rising: 3

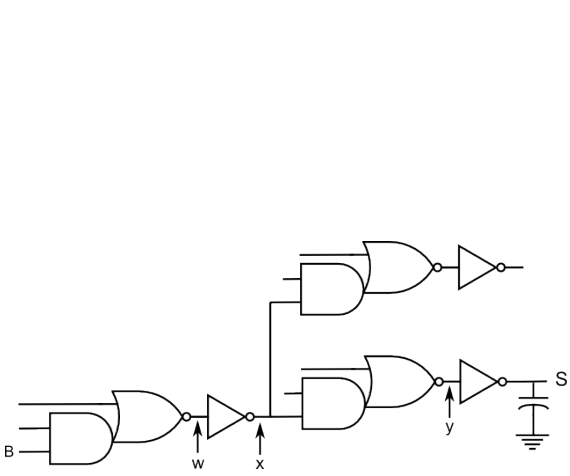
Falling: 13/6

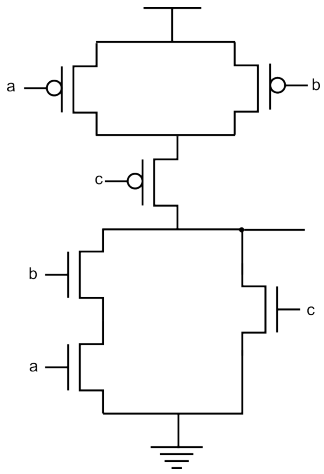
(b) Logical Effort of Input B: Rising: 7/3

Falling: 13/3

5.

Calculate the delay of the segment from B to S of the adder shown below, given that the output capacitance is 25 units (normalized), and the input capacitance of the first AOI121 gate is 6 units.





Delay = 16.28 units.

Now calculate the capacitances of the nodes y, x and w.

Capacitance of node y = 10.40 units.

Capacitance of node x = 8.66 units

Capacitance of node w = 7.21 units

6.

A particular technology node has a FO4 delay of 9 ps. How many minimum size inverters (2:1) need to be included in a ring oscillator so that the oscillating frequency is close to 7.3 GHz?

Number of inverters = 19

VLSI Design — J. Abraham

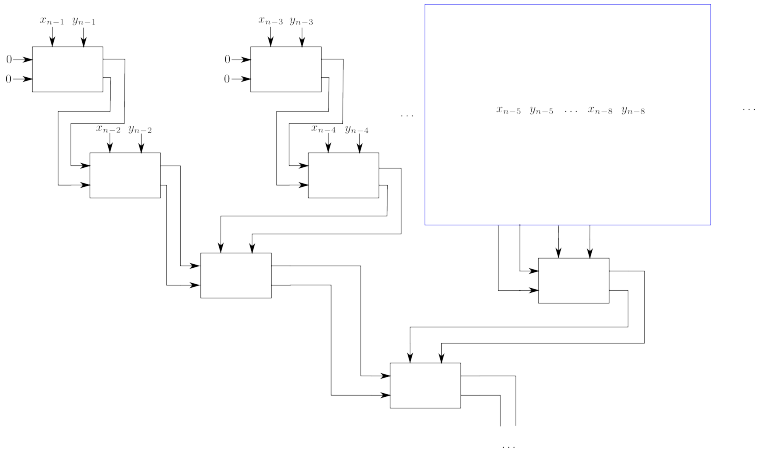
Fall 2016 — Outline Solution for Exam. I — October 3, 2016

1. (15 points)

Fill in the truth table entries for a cell in an iterative comparator. The signals c_i and d_i cannot be 1 at the same time (so this input will never occur).

c_{i+1}	d_{i+1}	x_i	y_i	c_i	d_i
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	0	0
0	1	X	X	0	1
1	0	X	X	1	0
1	1	-	-	-	-

Sketch the design of a comparator with delay $O(log_2 n)$, using **only** copies of the above cell.



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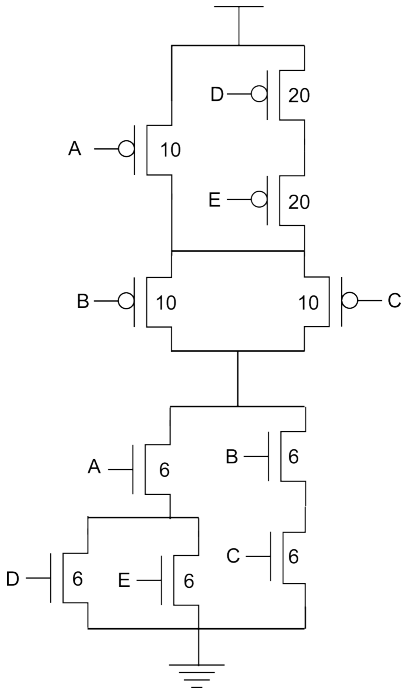
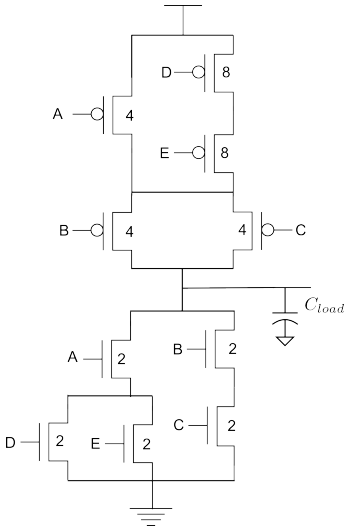
2. (10 points)
Size the transistors in the compound gate on the right with P:N = 5:3.



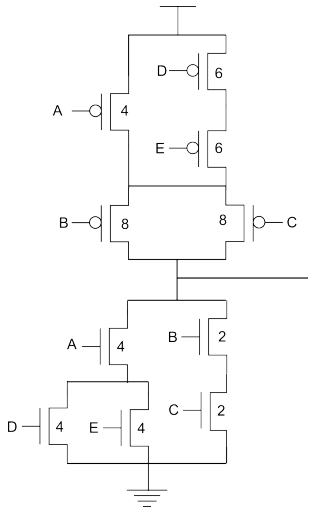
3. (15 points)
Using the Elmore delay formulation, find the *worst-case* rise and fall delays in the following circuit, when $C_{load} = 10C$.



Worst-case rise delay: 46RC
Input combination which results in worst-case rise delay: 11000
Worst-case fall delay: 65RC
Input combination which results in worst-case fall delay: 11010

4. (20 points)

Find the logical efforts of the following inputs in the CMOS circuit below.



(a) Logical Effort of Input A: Rising: 2, Falling: 4/3

(b) Logical Effort of Input E: Rising: 55/18, Falling: 5/3

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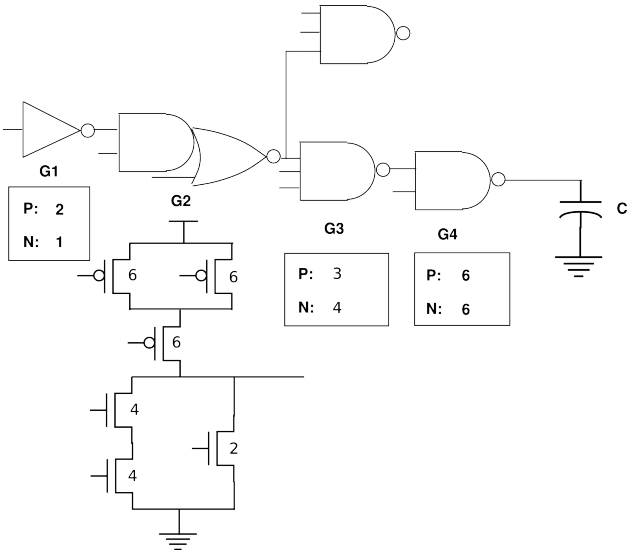
5. (25 points)

Find the smallest delay of the path from the input of G1 to the output of G4, when the load capacitance is 27 units. Label the sizes for the transistors in the gates. Use integer values for the sizes which most closely match the input capacitance and a P:N ratio of 2:1.

Delay = 20.3 units.



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6. (15 points)

The maximum number of 3-input NAND gates that can comprise the longest path, if the delay of the stage cannot exceed 6 FO4 delays?

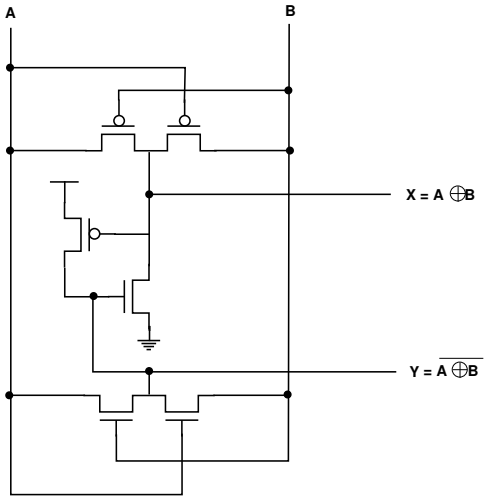
Maximum number of NAND gates in the longest path ≤ 4.

Spring 2007 | VLSI Design – ECD
OUTLINE SOLUTIONS to EXAM I | J. Abraham
March 10, 2007

Name: Student, 1

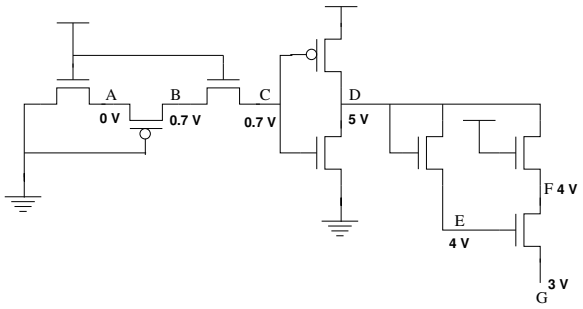
1.

Find the functions X and Y implemented by the following circuit.



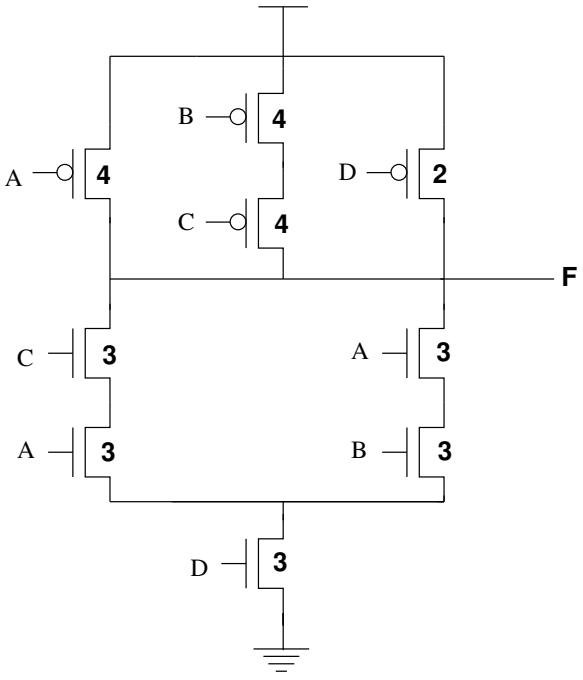
2.

Write down the voltages at A, B, C, D, E, F, G in the following circuits, assuming that the initial voltage on each node is 2.5 volts. The relevant transistor parameters are, $V_{dd} = 5V$, $V_{tn} = 1V$ and $|V_{tp}| = 0.7V$.



3.

Use the Elmore delay approximation to find the *worst-case* rise and fall delays at output F for the following circuit. The gate sizes of the transistors are shown in the figure. Use the assumption that the diffusion capacitance is equal to the gate capacitance and that a minimum sized transistor has gate and diffusion capacitance equal to C. The resistance of a nMOS transistor with unit width is R and the resistance of a pMOS transistor with width of 2 is also R. Also assume NO sharing of diffusion regions.



Input for worst-case rise delay (ABCD) = **1100**

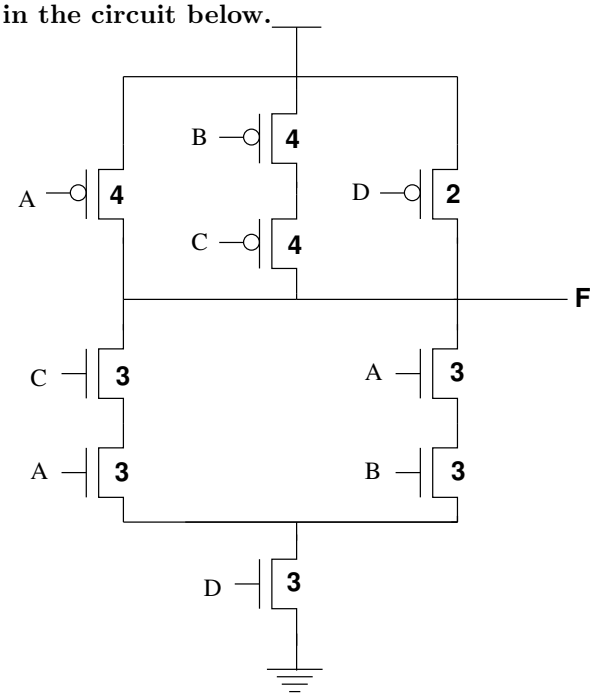
Worst-case rise delay = **39RC**

Input for worst-case fall delay (ABCD) = **1101**

Worst-case fall delay = **33RC**

4.

Find the logical efforts for the inputs, A, B, C, and D in the circuit below.



Logical effort of A =

Output Falling: 10/3, Output Rising: 10/6

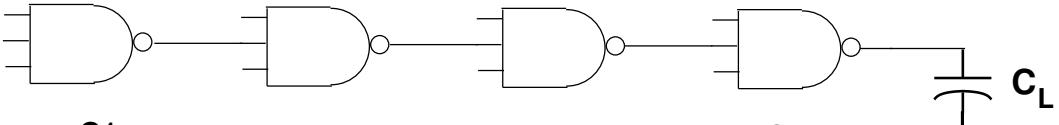
Logical effort of B = **7/3**

Logical effort of C = **7/3**

Logical effort of D = **5/3**

5.

(a) Find the sizes of the P and N transistors in the gates below, to achieve the minimum delay, if the output capacitance C_L is 524 units.



G1	G2	G3	G4
P: 2	P: 6	P: 20	P: 66
N: 3	N: 10	N: 31	N: 98

(b) If a chain of n inverters, starting with a 2:1 inverter, is driving a load of $3C_L$, what is the input capacitance at each stage for the least delay?
If the stages are labeled $0..(n-1)$, the input capacitance at stage i is $3C_L^{(i/n)}$

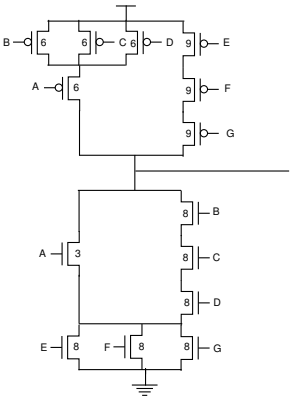
(c) Would the input capacitance in (b) depend on the type of gate being used in each stage? Explain.
For a chain of gates with logical effort g, $F = g^n.H$, and $f = gH^{(1/n)}$.
Input capacitance at any stage = $\frac{C_{out}\ g}{gH^{(1/n)}} = C_{out}/H^{(1.n)}$ which is not a function of g.

Spring 2009 | **EE 360R – Computer-Aided IC Design** **OUTLINE SOLUTIONS to EXAM I** | **J. Abraham** **March 4, 2009**

Name: Student,

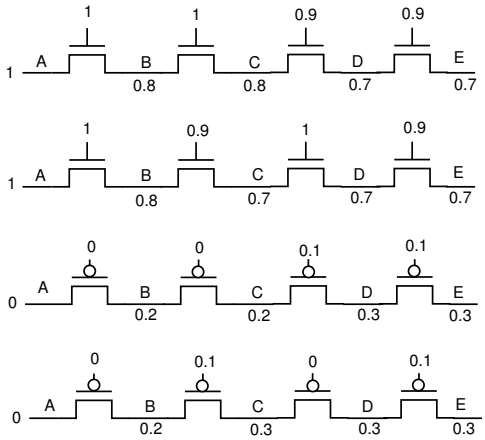
1.

Size the transistors to match the current of an inverter with p-width of 3 and n-width of 2.



2.

Write down the voltages at the nodes in the following circuits, assuming that an initial voltage on each node is 0.5 volts. Relevant transistor parameters are, $V_{dd} = 1V$, $V_{tn} = 0.2V$ and $|V_{tp}| = 0.2V$.



3.

Use the Elmore delay approximation to find the *worst-case* rise and fall delays at output F. Assume NO sharing of diffusion regions. (Hint: off-path capacitances can contribute to delay.)

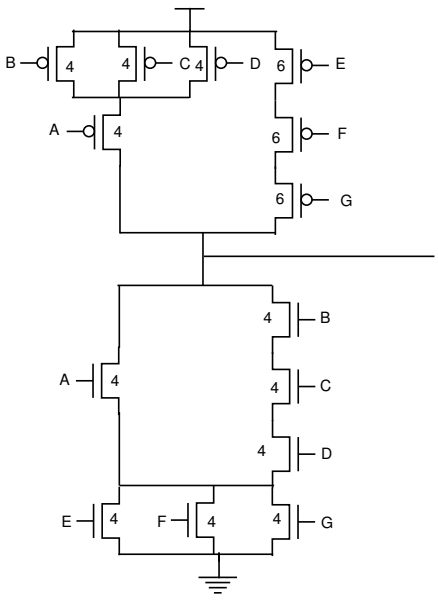
Input for worst-case rise delay (ABCDEFG) = **0111000**

Worst-case rise delay = **82RC**

Input for worst-case fall delay (ABCDEFG) =

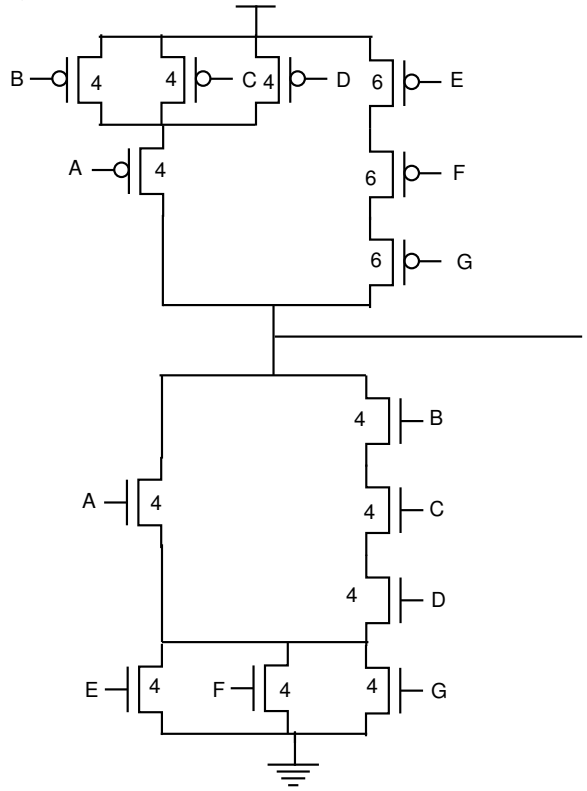
0111100

Worst-case fall delay = **73RC**



4.

Find the logical efforts for the inputs, A, B, C, D, E, F, and G in the circuit below.



Logical effort of A =

Output Rising: 8/3, Output Falling: 8/6

Logical effort of B = 8/3

Logical effort of C = 8/3

Logical effort of D = 8/3

Logical effort of E = 10/3 (worst-case)

Logical effort of F = 10/3 (worst-case)

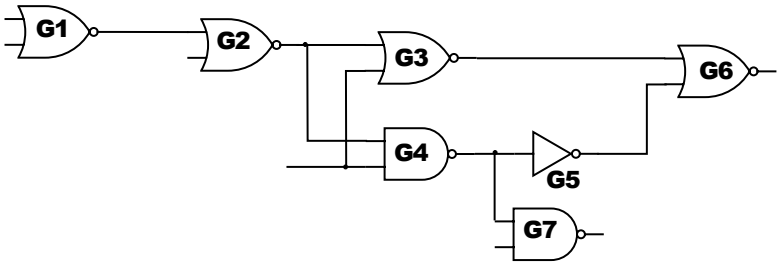
Logical effort of G = 10/3 (worst-case)

5.

Calculate the delays of the paths G1-G2-G3-G6 and G1-G2-G4-G5-G6 in the circuit below using logical effort. Also give the sizes of the P and N transistors to achieve this delay. You may assume that the off-path capacitance is the same as the on-path capacitance for each branch.

Input capacitance of NOR Gate G1 = 5 units.

Load capacitance driven by Gate G6 = 106 units.



Delay of Path G1 - G2 - G3 - G6: 25

G1	G2	G3	G6
P: 4 N: 1	P: 10 N: 3	P: 13 N: 3	P: 33 N: 9

Delay of Path G1 - G2 - G4 - G5 - G6: 26.5

G1	G2	G4	G5	G6
P: 4 N: 1	P: 8 N: 2	P: 6 N: 5	P: 10 N: 5	P: 40 N: 10