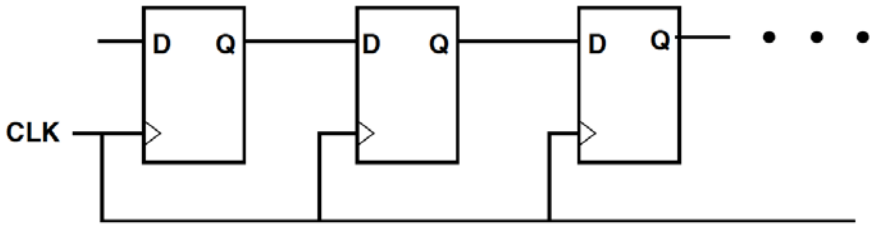
Sample Exam #2 Questions

The flops used in the shift register below have a setup time of 100 ps, a maximum clock-Q delay of 150 ps, and a minimum clock-Q delay of 100 ps.



(a) How fast can this circuit be clocked?

Clock frequency = [ ] MHz

(b) What is the limit on the hold time of the flops at this frequency?

Hold time < [ ] ps

(c) What is the limit on the hold time of the flops at a frequency of 1 GHz?

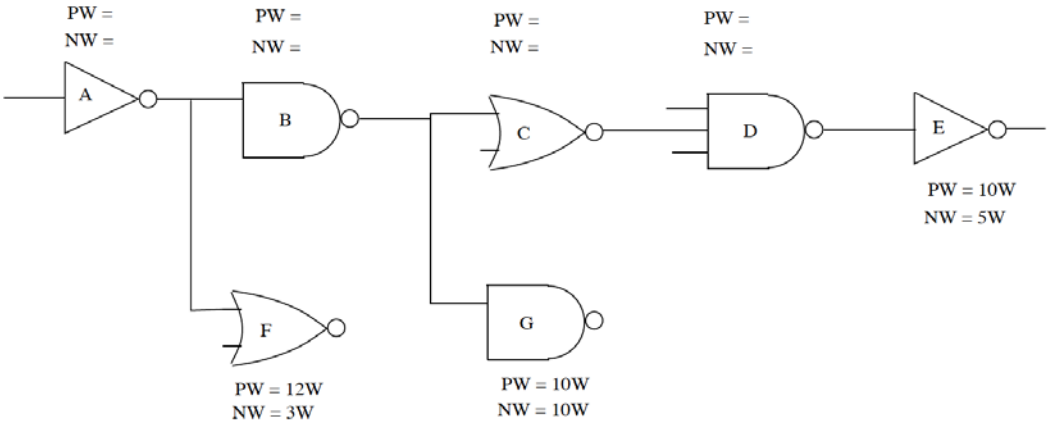
Hold time < [ ] ps

(d) What is the limit on the hold time of the flops if the circuit is clocked at a frequency of 100 MHz?

Hold time < [ ] ps

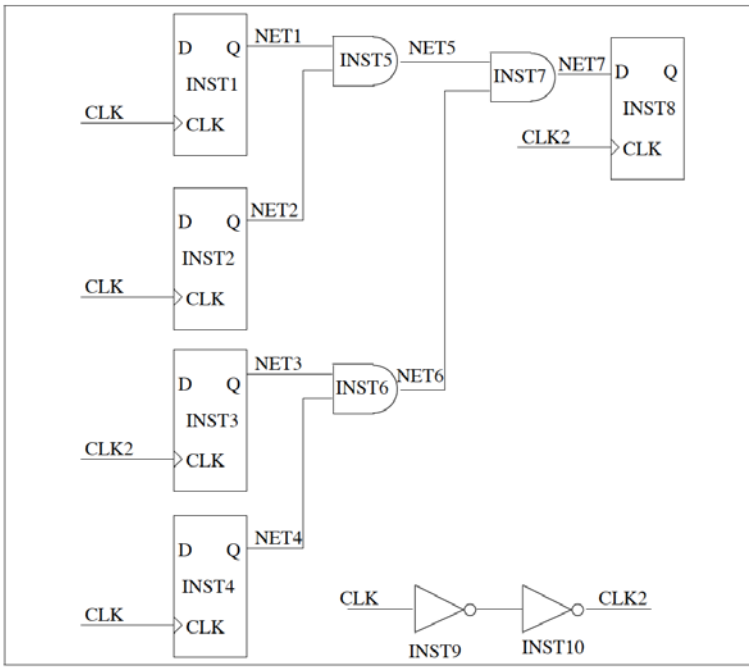
Sample Exam #2 Questions

1. (25 points) Size the following path (A, B, C, D) using a 2:1 P:N ratio and a *stage ratio* of 3. Indicate the size of P and N transistors in the gates A, B, C and D.



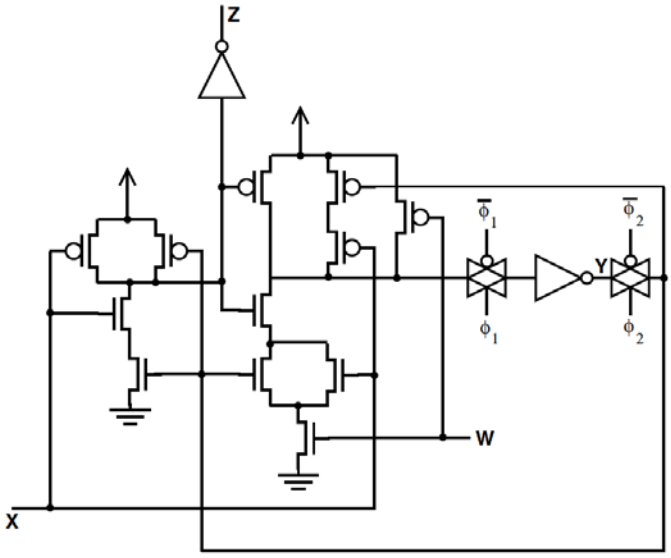
Identify if there are any hold time problems from the source flops (INST1, INST2, INST3 and INST4) to INST8 in the following circuit. If there are any, indicate by how much the hold time is violated and suggest a fix. Use the delays from the table below. Do not insert additional delays for the paths that have no hold violations.

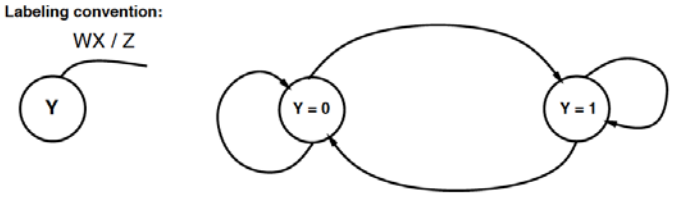
	Rise	Fall
CLK ⇒ Q	370ps	370ps
Flop Hold Time	800ps	800ps
And Gate	300ps	200ps
Inverter Gate	50ps	20ps



Sample Exam #2 Questions

(a) The circuit below has two inputs, W and X, and one output Z. It has two states, implemented by the state variable Y. Complete the State Diagram for the circuit, labeling the arcs as indicated with the appropriate binary values of W, X and Z.

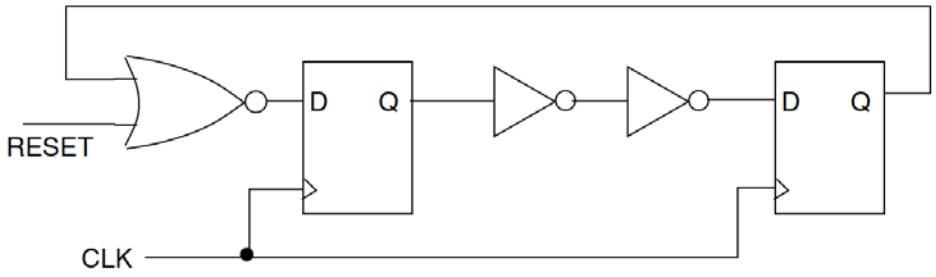




(b) What does the circuit do?

Sample Exam #2 Questions

(a) What is the highest frequency at which the following circuit can be operated correctly? The parameters of the components are as follows.
Inverter: $t_{pd} = 200ps$, $t_{cd} = 100ps$
2-input NOR: $t_{pd} = 200ps$, $t_{cd} = 150ps$
D-flop: $t_{pd} = 200ps$ $t_{cd} = 0ps$, **Setup time = 300 ps, Hold time = 100 ps.**



Maximum Clock frequency = ☐ **MHz**

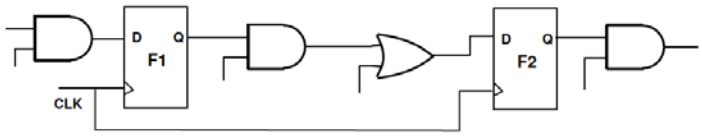
(b) If the two inverters are removed (the Q of the first flop is connected to the D of the second), what will be the highest frequency at which the circuit can be operated. Explain your answer.

Maximum Clock frequency = ☐ **MHz**

Sample Exam #2 Questions

The circuit below has the following parameters for the components:
Clock period = 90 nS with a 50% duty cycle
t_{clk-q} = 40 nS
t_{setup} = 20 nS
t_{hold} = 45 nS
AND gate delay = 15 nS
OR gate delay = 20 nS
Inverter delay = 5 nS

Assume that the logic before F1 and after F2 has arbitrary slack and is impervious to timing issues.

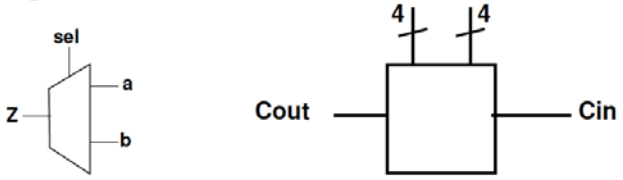


(a) Will this circuit work correctly? Explain, and find the magnitude of the violation, if any.

(b) If you cannot move any cells, but can add inverters anywhere in the design, show the new design which fixes the violation but does not change the functionality. Show the modification in the diagram above.

(c) If the design above has already been implemented in Silicon, you cannot change the design or add circuitry. Is there still a way to make the circuit work? Explain.

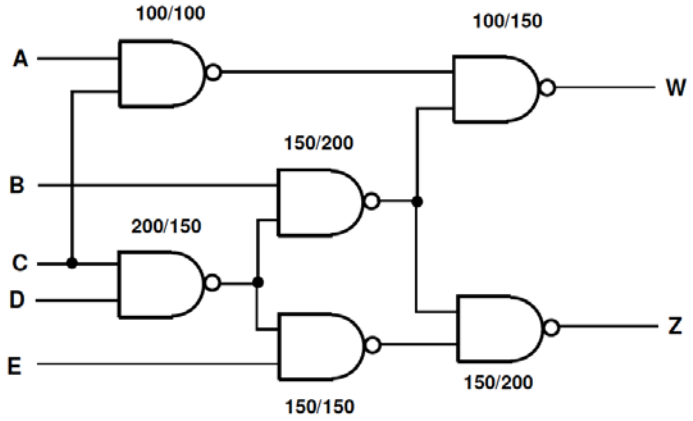
An application requires the carry out result of the addition of two 12-bit numbers, with the result to be produced in 1 nS. Design a circuit to achieve this, using ONLY two types of cells, a 4-bit adder with a delay of 400 pS and a 2-1 1-bit multiplexer with a delay of 100 pS.



Draw a neat block diagram of your circuit below.

Sample Exam #2 Questions

The following is a combinational circuit between two sets of flip-flops. The rise/fall delays (in pS) of each of the gates is shown. You are to analyze the circuit for information relating to the clocking of the system, and to find tests which will exercise the system for different conditions. When generating the tests, assign logic values to the smallest possible set of variables, leaving as many variables with X as possible.



(a) Find the delay through the circuit which will have the maximum impact on the clock frequency, and a test sequence for this delay.

Delay which has maximum impact on clock frequency = ☐

Test which produces this delay in the circuit:

A	B	C	D	E	W	Z

(b) Find the delay through the circuit which will have the largest impact on the hold time requirements, and a test sequence for this delay.

Delay which has largest impact on hold time = ☐

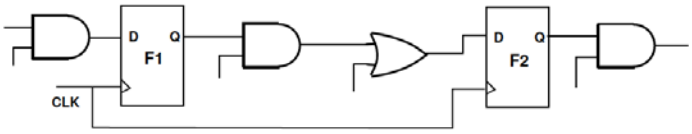
Test which produces this delay in the circuit:

A	B	C	D	E	W	Z

Sample Exam #2 Questions

The circuit below has the following parameters for the components:
Clock period = 90 nS with a 50% duty cycle.
t_{clk-q} **= 5 nS**
t_{setup} **= 20 nS**
t_{hold} **= 45 nS**
AND gate delay = 15 nS
OR gate delay = 20 nS
Inverter delay = 5 nS

Assume that the logic before F1 and after F2 has arbitrary slack and is impervious to timing issues.



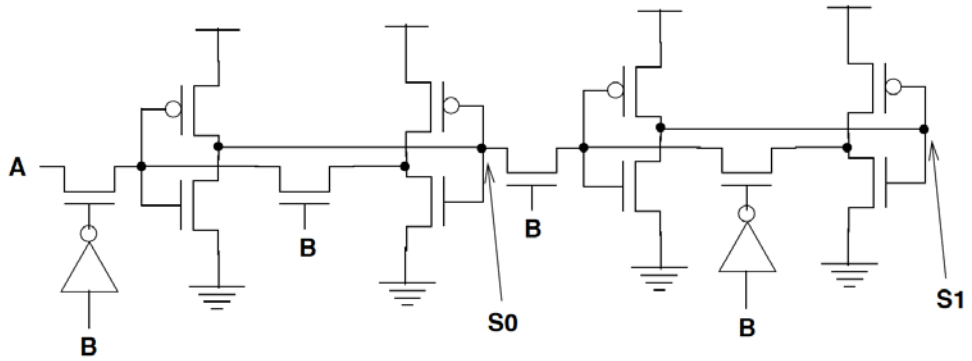
(a) Will this circuit work correctly? Explain, and find the magnitude of the violation, if any.

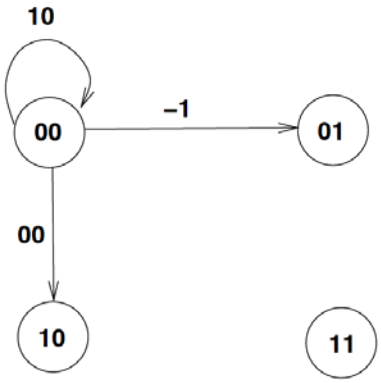
(b) If you cannot move any cells, but can add inverters anywhere in the design, show the new design which fixes the violation but does not change the functionality. Draw the inverters in the diagram above.

(c) If the design above has already been implemented in Silicon, you cannot change the design or add circuitry. Is there still a way to make the circuit work? Explain.

Sample Exam #2 Questions

Complete the state transition diagram for the circuit below ("-" represents a "don't-care").



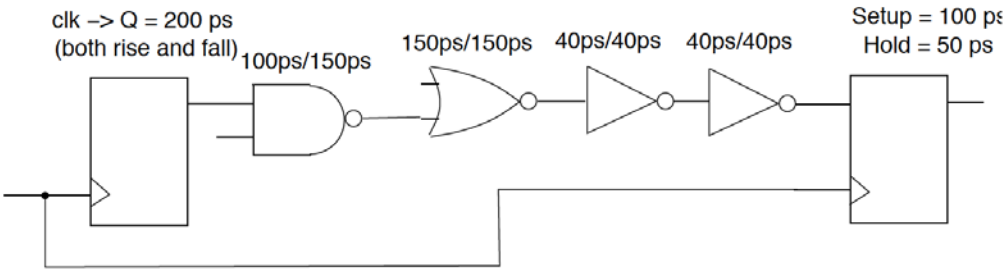


State: S0 S1

Transition: AB

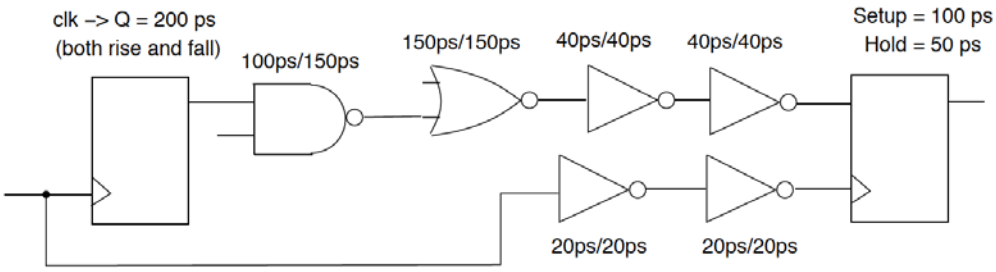
Sample Exam #2 Questions

(a) What is the maximum frequency at which the following design can operate?



Frequency = MHz

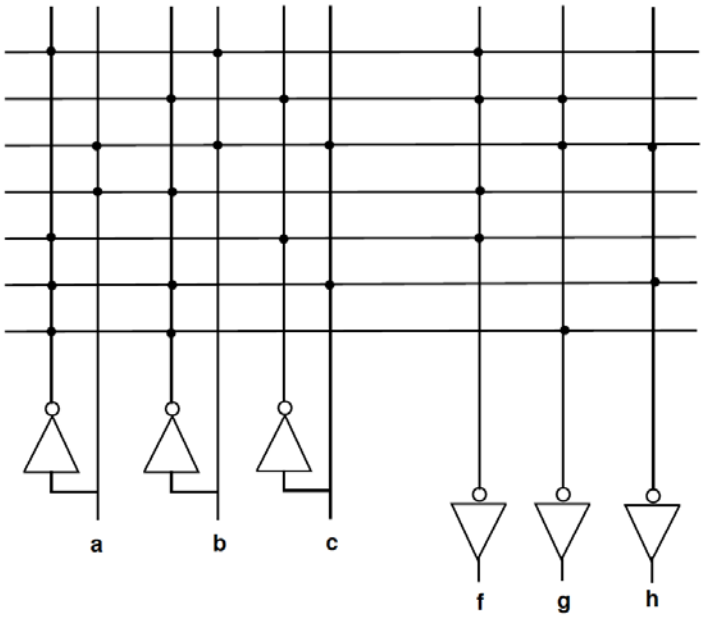
(b) What is the maximum frequency at which the following design can operate?



Frequency = MHz

Sample Exam #2 Questions

Identify the functions, f, g and h implemented by the PLA below, drawn in dot notation.



☐ $f = \overline{a}\ \overline{b}\ \overline{c} + a\ b\ \overline{c}$

☐ $f = \overline{a}\ b + \overline{b}\ \overline{c} + a\ \overline{b} + \overline{a}\ \overline{c}$

☐ $f = a\ \overline{b} + b\ c + \overline{a}\ b + a\ c$

☐ $f = \overline{a}\ \overline{b}\ \overline{c} + b\ c + a\ b$

☐ $g = \overline{a}\ \overline{b}\ \overline{c} + b\ c + a\ b$

☐ $g = a\ b\ c + \overline{b}\ \overline{c} + \overline{a}\ \overline{b}$

☐ $g = \overline{a}\ b + \overline{b}\ \overline{c} + a\ \overline{b} + \overline{a}\ \overline{c}$

☐ $g = a\ b\ c + \overline{a}\ \overline{b}\ c$

☐ $h = a\ \overline{b} + b\ c + \overline{a}\ b + a\ c$

☐ $h = a\ b\ c + \overline{a}\ \overline{b}\ c$

☐ $h = a\ b\ c + \overline{b}\ \overline{c} + \overline{a}\ \overline{b}$

☐ $h = \overline{a}\ \overline{b}\ \overline{c} + a\ b\ \overline{c}$