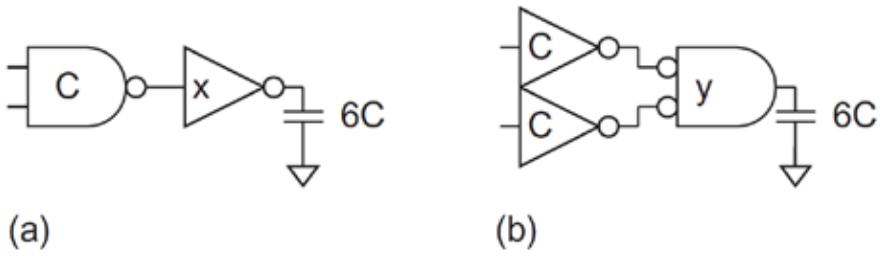
**Fall 2018**
**EE 460R: Introduction to VLSI Design**
**EE 382M-7: VLSI-1**
**Homework #3**

**Assigned: September 25th, 2018** **Due: October 4th, 2018**

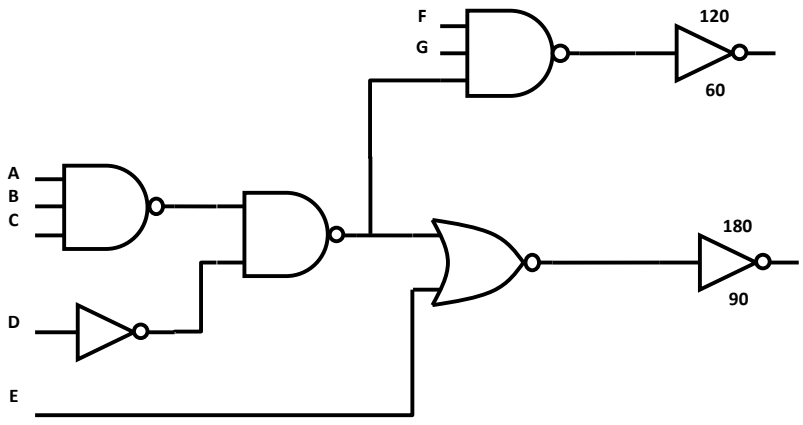
1. Find the rising and falling propagation delays of an AND-OR-INVERT gate using the Elmore delay model. Estimate the diffusion capacitance based on a stick diagram of the layout.

2. Find the worst-case Elmore parasitic delay of an *n*-input NOR gate and an *n*-input NAND gate.

3. Consider the two designs of a 2-input AND gate shown in the following figure. Give an intuitive argument about which will be faster. Back up your argument with a calculation of the Elmore delay, and input capacitances *x* and *y* to achieve the delay.




4. Size the following gates using a stage ratio of 3. Assume a unit inverter has a pMOS transistor of width 4 and an nMOS transistor of width 2.



5. Size the following gate so that it has the same drive strength as an inverter that has a pMOS transistor of width 3 and an nMOS transistor of width 1.