Fall 2018
EE 460R: Introduction to VLSI Design
EE 382M-7: VLSI-1
Homework #6

Assigned: October 30th, 2018 **Due: November 13th, 2018**

1. An embedded SRAM contains 2048 8-bit word/s. If it is physically arranged in a square fashion. How many inputs does each column multiplexer require?

2. Estimate the dimensions of the SRAM array in Problem 1 using a 1.3 x 1.44 μm SRAM cell, assuming periphery circuitry adds 10% to each dimension of the core.

3. How would you make this SRAM **cell more stable** to effects such as Alpha Particles?

4. Sketch designs for a 6:64 decoder with and without pre-decoding. Comment on the pros and cons of pre-decoding.

5. Design the decoder for a register file (from Section 4.5.3) with the following specifications:
    a) 32-word register file
    b) 64-bit words
    c) Each register bit presents a load of 3 unit-sized transistors on the word line.
    d) True and complementary versions of the address bits A[4:0] are available.
    e) Each address input can drive 12 unit-sized transistors.

    Determine the fastest decoder design and estimate the delay of the decoder and the transistor widths to achieve this delay.