1. Find a test for the node N stuck-at-0 in the circuit below.
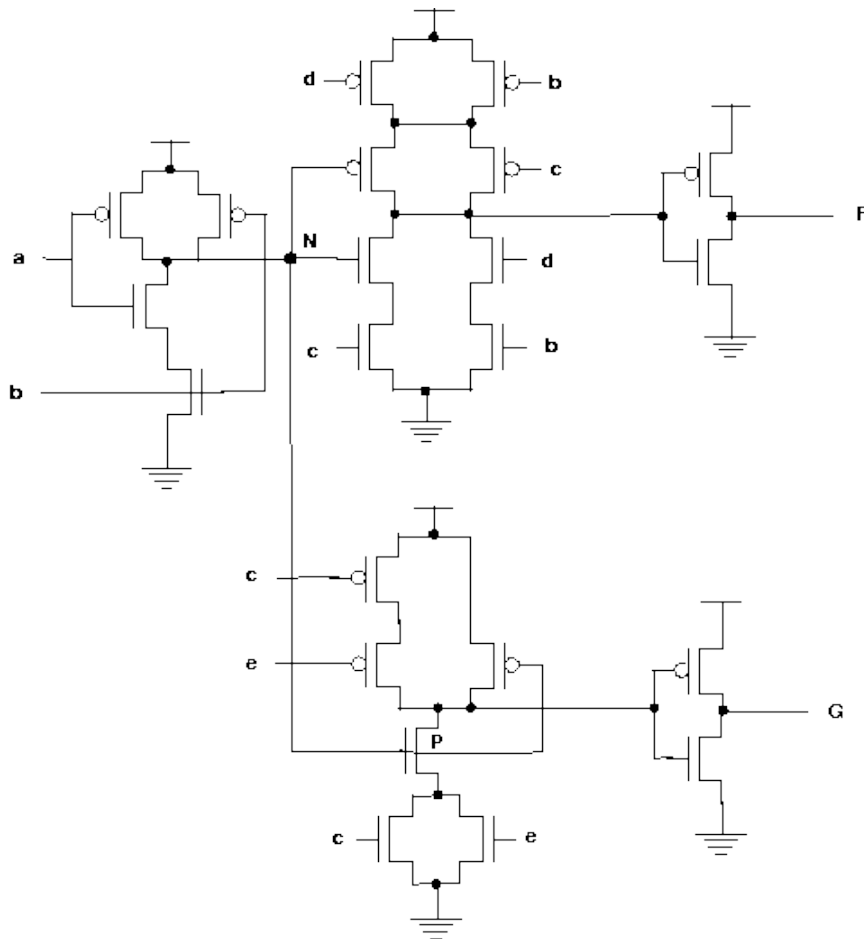
2. Problem 14.4 from the Exercises for Chapter 14 (page 657).

   An FIR filter for a GSM receiver with sigma-delta converter as shown in Figure 14.8(b) has a single-bit input. To what structure do the multipliers degenerate? If the coefficients are a single bit and a 288-tap filter has to operate at 13 MHz, what architecture would you use for the overall design?

3. Problem 14.6 from the Exercises for Chapter 14 (page 657).

   Using the Sea of Gates structure from Figure 14.17(a), design the metallization for a 3-input NOR gate.

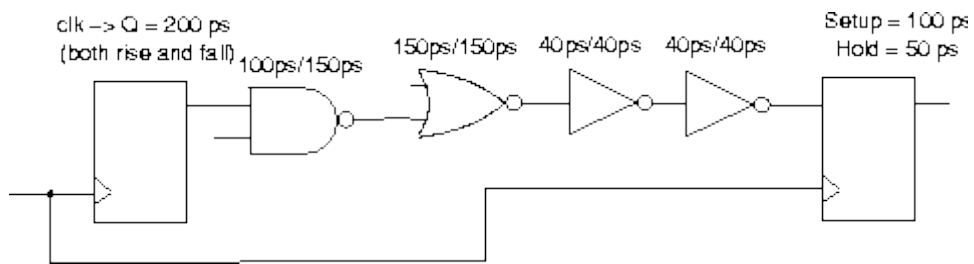4. Problem 12.1 from the Exercises for Chapter 12 (page 546).

An embedded SRAM contains 2048 8-bit words. If it is physically arranged in a square fashion, how many inputs does each column multiplexer require?

5. Problem 12.2 from the Exercises for Chapter 12 (page 546).

Estimate the dimensions of the SRAM array in Exercise 12.1 using a 1.3×1.44 μm SRAM cell, assuming periphery circuitry adds 10% to each dimension of the core.

6. Calculate maximum frequency

(a) What is the maximum frequency at which the following design can operate?

(b) What is the maximum frequency at which the following design can operate?