Lecture 1:
Introduction to VLSI Design

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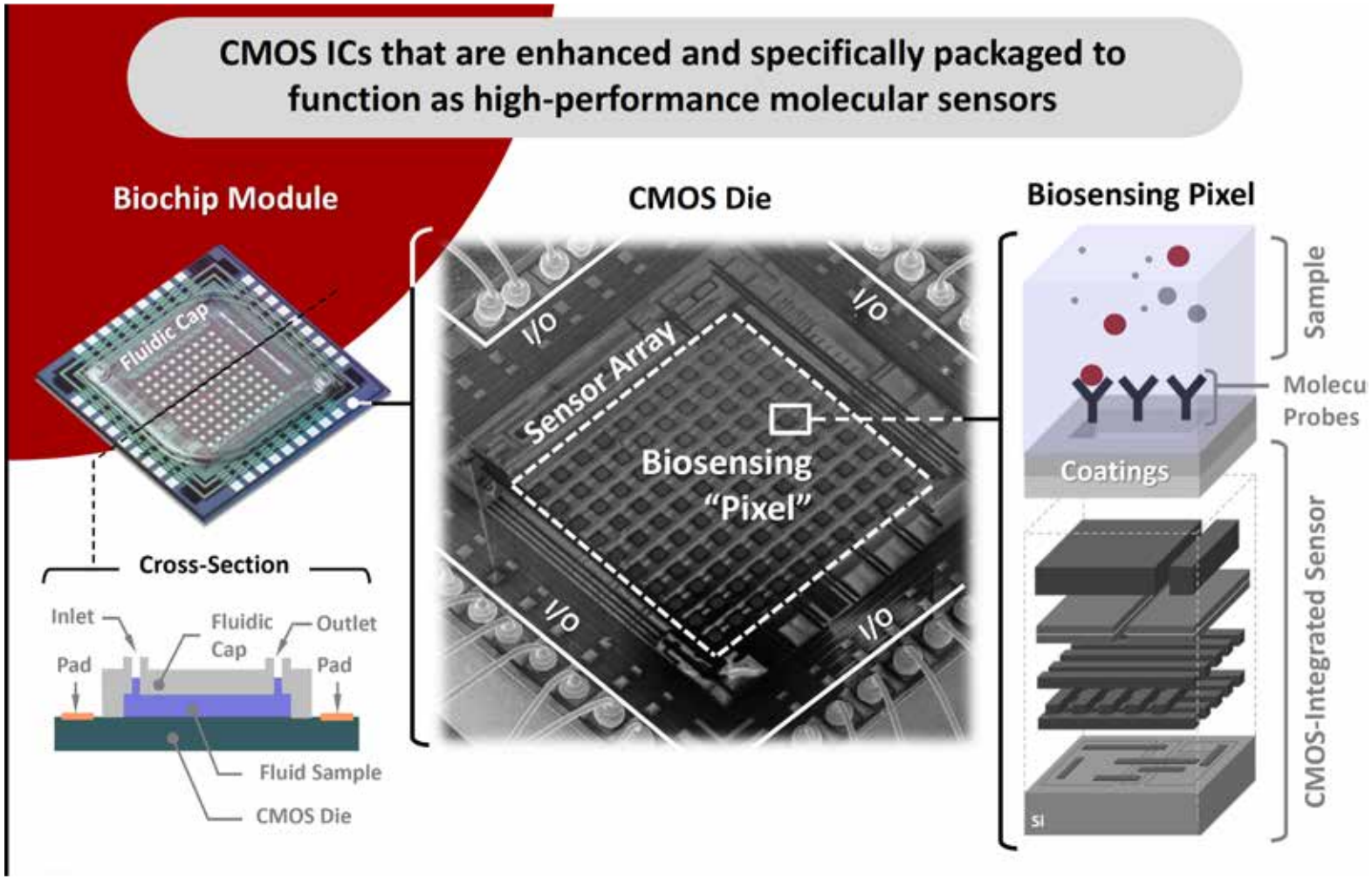
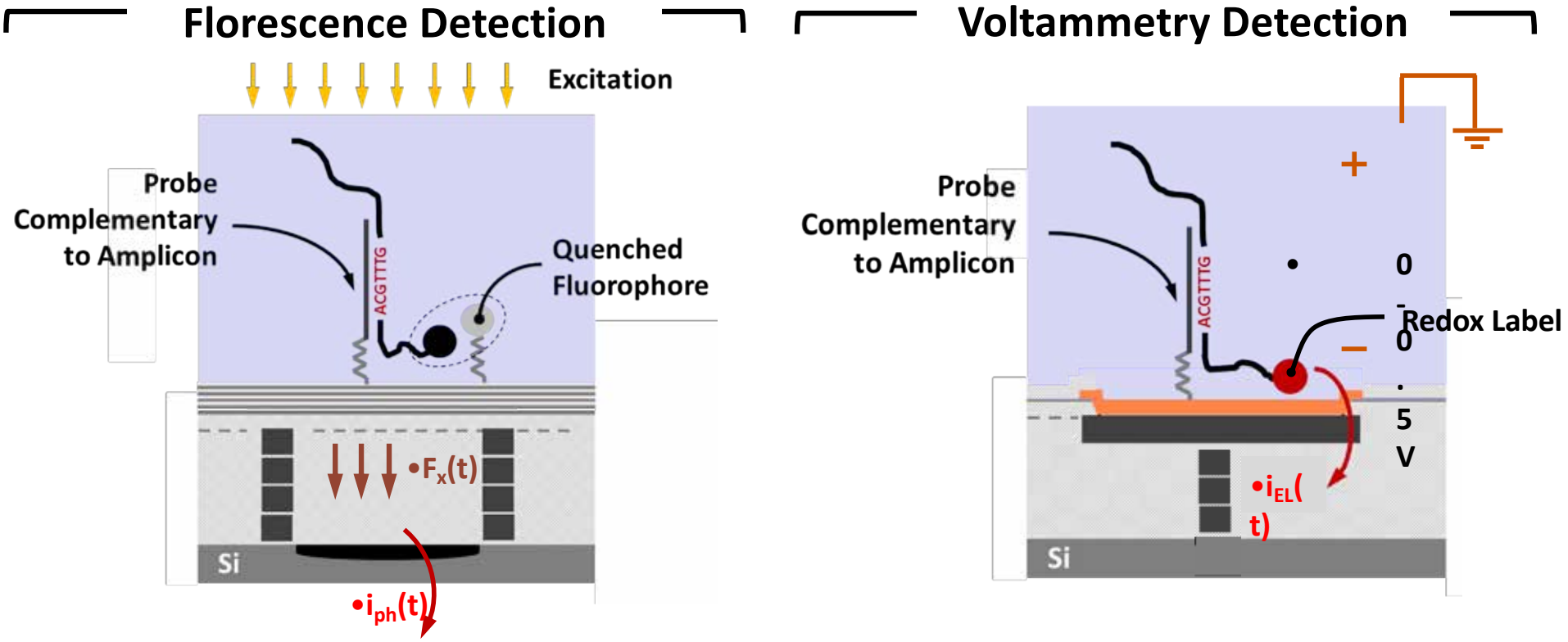
Why is VLSI design still fun?

- Get to work on crazy new applications of IC technology.
- For example: CMOS Bio-Sensors



General Idea of the Biosensor

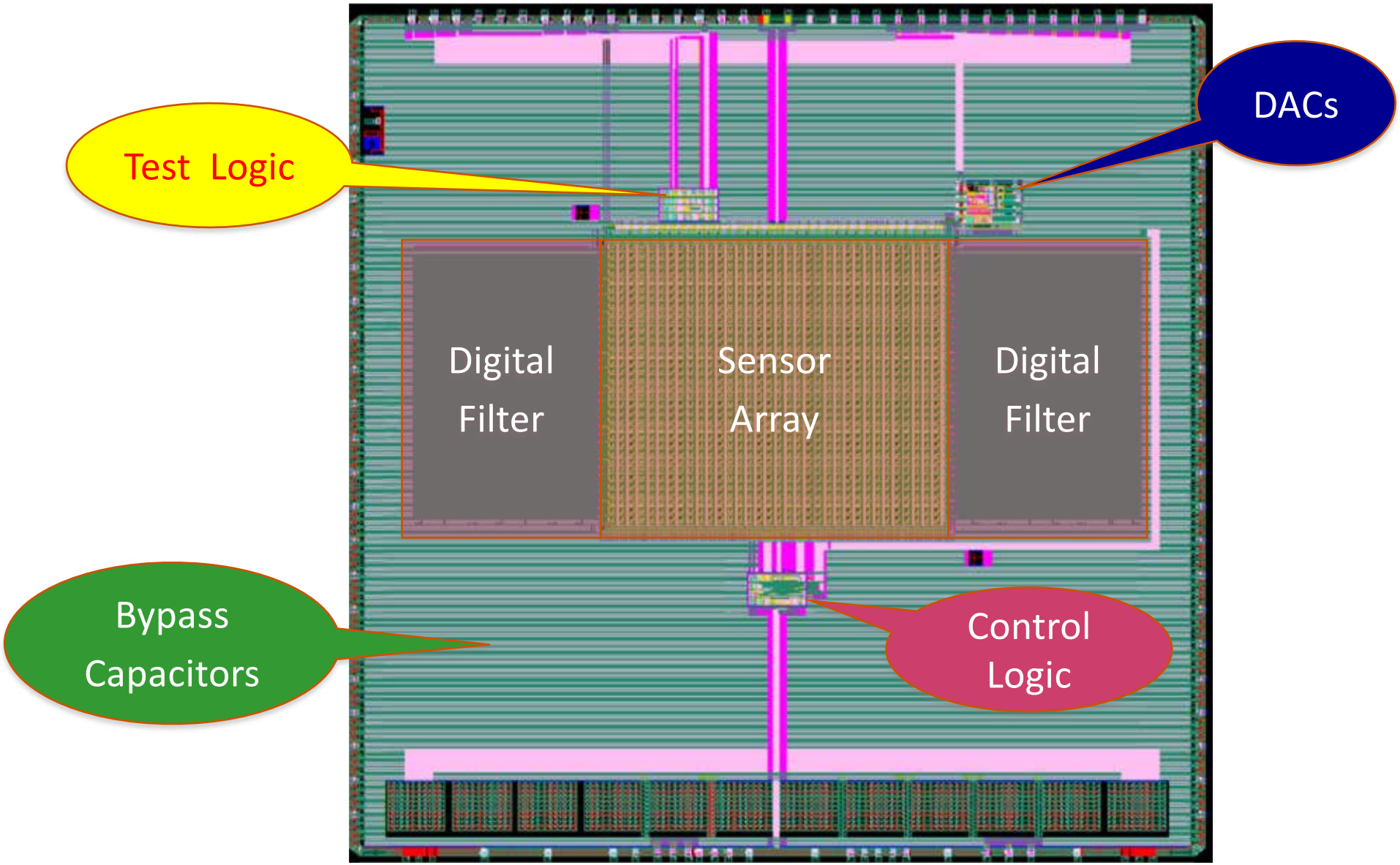
Both fluorescence and voltammetry analysis require very small currents sensing



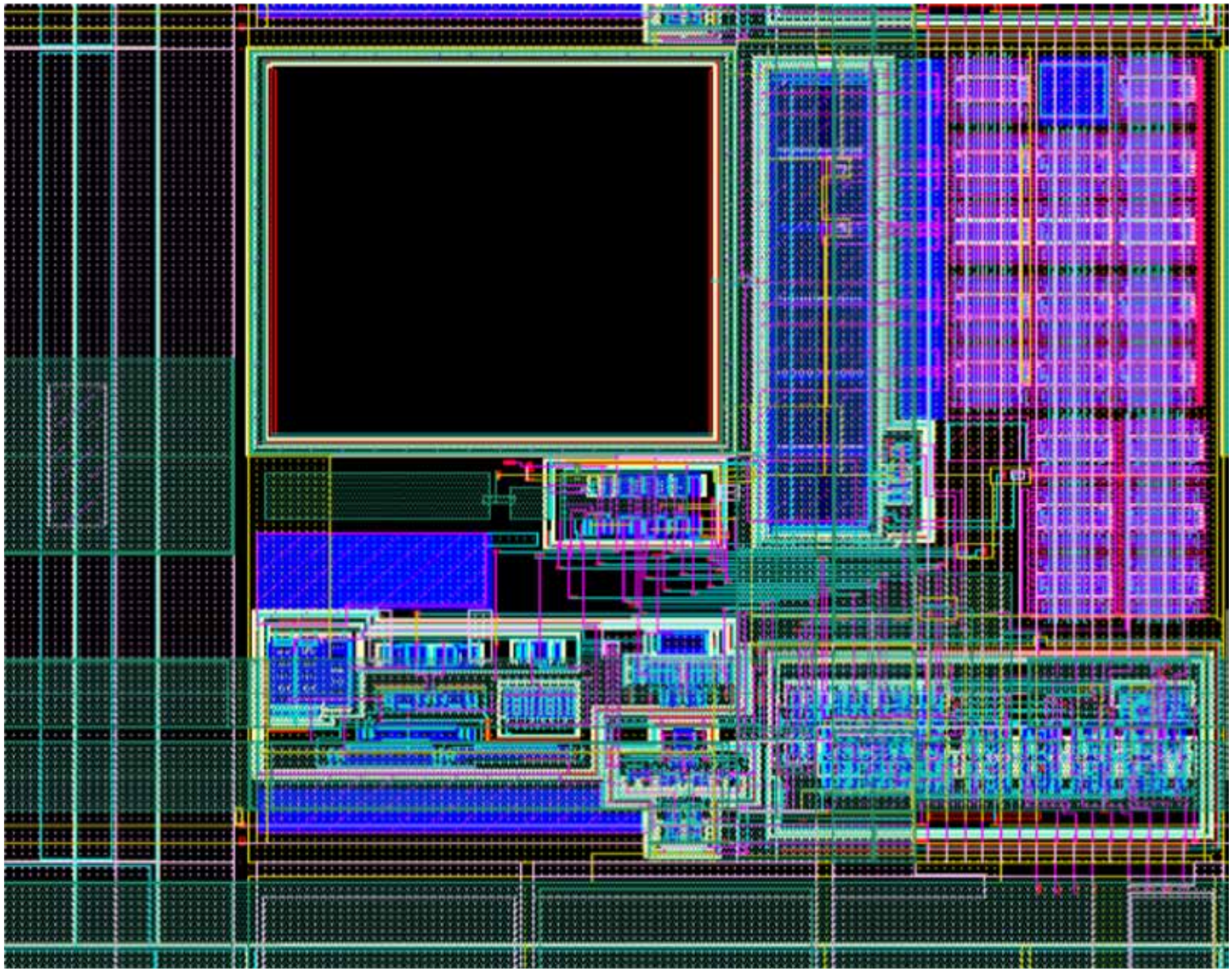
NOTE 1: Post-processing of CMOS is a another task

NOTE 2: Optimizations/generation of probes and amplicons is another task

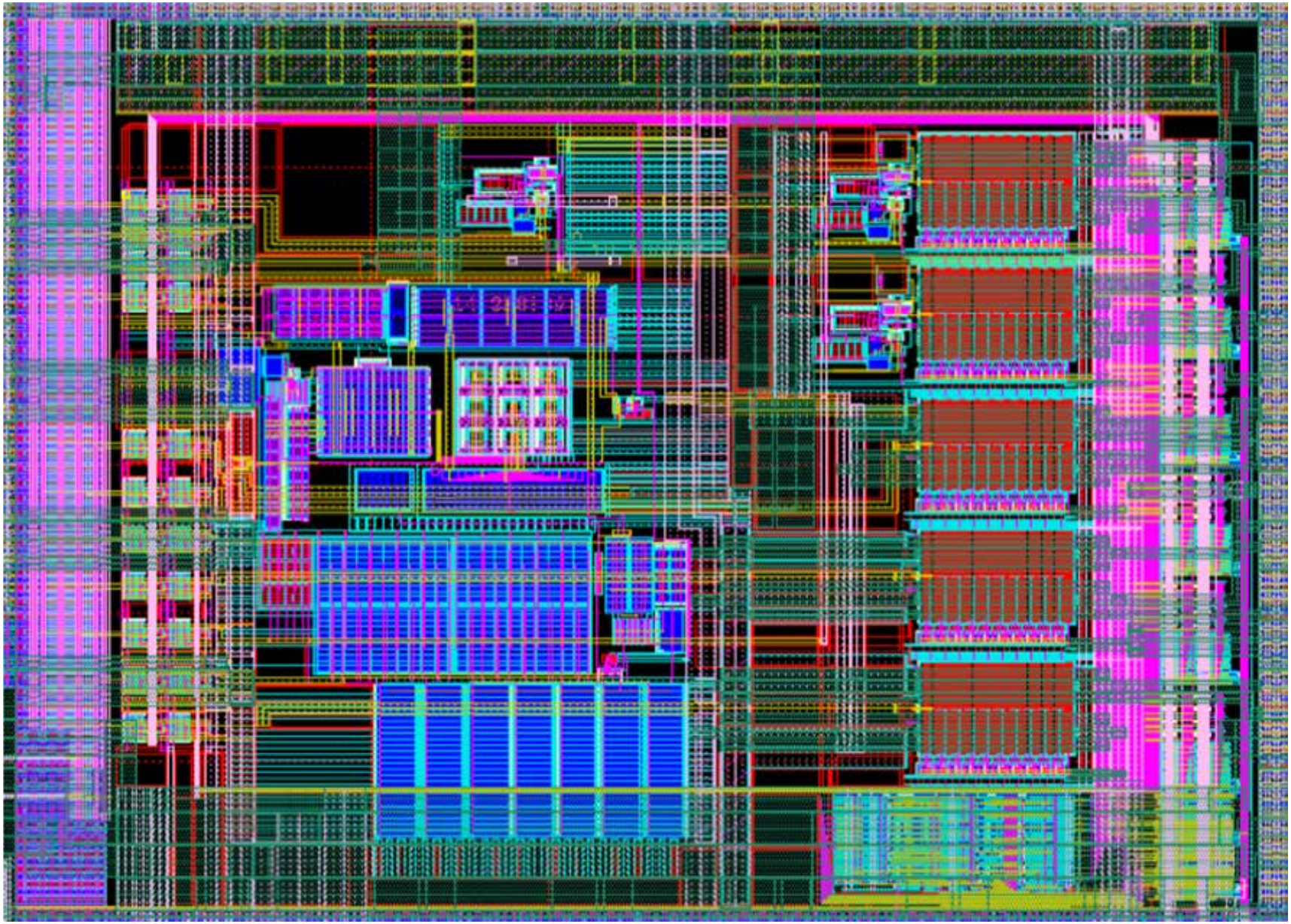
Bio-sensor die plot



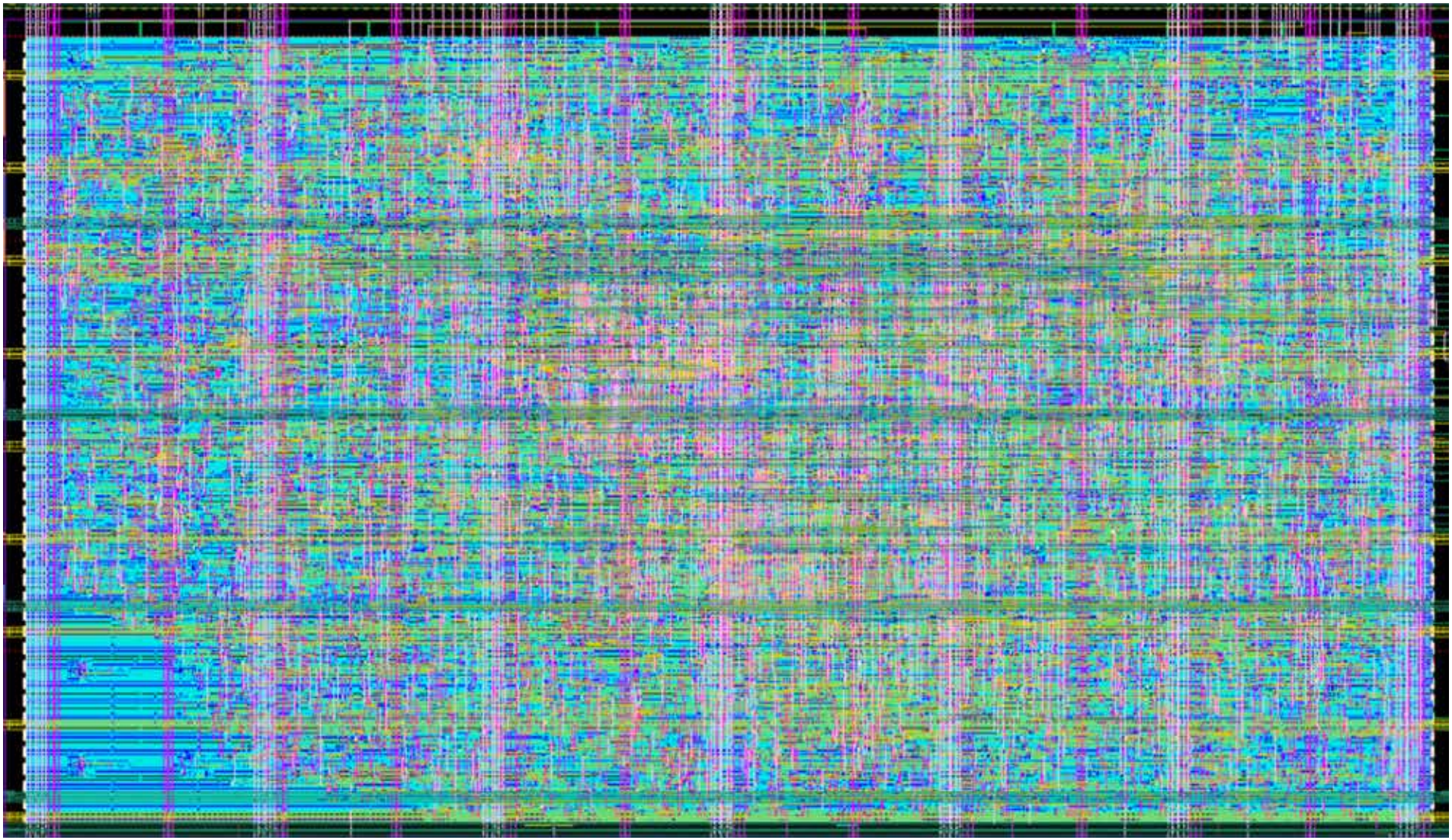
Bio-sensing element



Digital to Analog Converters



Digital control block



What Will You Learn in this course?

- Economics
- How integrated circuits really work
- How do you design chips with 100's of millions of transistors
  - Understand what a "design flow" is
  - Use of commercial design automation tools to speed up the design process
  - Ways of managing the complexity using hierarchical design methods
  - Use integrated circuit cells as building blocks (widgets)
- Understand design issues at the layout, transistor, logic and register-transfer levels
- Concept of robustness
  - Making sure the designs are correct
  - Making the chips testable after manufacturing
- Effects of technology scaling, reducing power consumption, etc.
- Identifying performance bottlenecks and ways of speeding up circuits

Learning General Principles

- Chip design involves simultaneous multi-metric optimization, tradeoffs, etc.
- Need the ability to work as part of a team
- Technology changes fast, so it is important to understand the general principles which would span technology generations
- Systems are implemented using building blocks (which may be technology-specific)
- There is lots of work in this course, but you will learn a lot too!!

Course Information

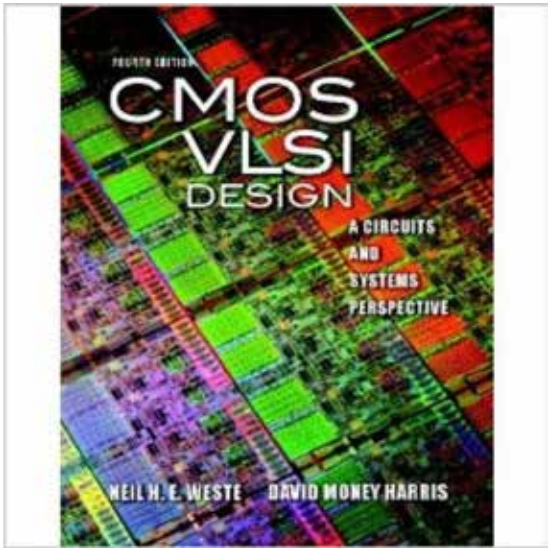
- **Class meets Tue/Thu, 14:00–15:30, ECJ 1.318**
  - Lab & TA hours posted on the class web site

- **Instructor: Mark McDermott**
  - Office: EER 5.826 (512) 471-3253
    - Email: mcdermot@ece.utexas.edu
  - Office hours:
    - Tue/Thu: 12:00 - 13:30
    - Mon/Wed: 9:00 - 11:00
    - And by appointment.

- **Course Web Pages:**
  - http://users.ece.utexas.edu/~mcdermot/ee460r_fall_2018.htm

Course Information (cont)

- Prerequisites: A working knowledge of digital logic design (EE316), fundamentals of electronic circuits (EE438) is required.
- Textbook: Weste and Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Addison Wesley/Pearson, 4th Edition, 2011
- Lectures and discussion in class will cover basics of course
- Homework, Laboratory exercises will help you gain a deep understanding of the subject
- Acknowledgements
  - Jacob Abraham (UT)
  - Gian Gerosa (Intel)
  - Steve Sullivan (Apple)
  - Kevin Nowka (IBM)
  - Michael Orshansky (UT)
  - Raghuram Tupuri
  - Adnan Aziz
  - David Harris (HMC)
  - Neil Weste



Work required by this course

- **Lectures**
  - Read sections in text and slides before class
- **Homework problems**
  - 8 homework assignments
- **Laboratory exercises**
  - Three major exercises dealing with various aspects of VLSI design
  - Complete each section before the deadline
- **Project (EE 382M)**
  - Your opportunity to design a chip of interest to you
  - Design could be completed to the point where it could be fabricated by following process covered this course

- **This course involves a large amount of work throughout the semester. Pace yourself.**

Exams and Grading

- **Two exams, in class, open book and notes which means the exams are hard**
  - **Oct 11th and Nov 8th**
- **Final Exam (EE460R only)**
  - **Date: TBD**
- **Grading**

Grading: 460R		Grading 382M	
Homework	16%	*Homework*	16%
Lab 1	10%	*Lab1*	10%
Lab 2	10%	*Lab2*	10%
Lab 3	14%	*Lab2*	14%
Exam 1	15%	*Exam 1*	15%
Exam 2	15%	*Exam 2*	15%
Final Exam	20%	*Project*	20%
Penalty for late submission: 5% per working day (maximum 25%, no submissions after 5 working days)			

Collaboration is good! Cheating is not!

- ***Collaboration* is good!**
  - Discussing issues with your classmates is a good way to learn and a study group is a very effective learning tool. Feel free to discuss homework, laboratory exercises with classmates, TAs and the instructors
  - Helping each other learn is particularly satisfying
  - But.... *Individual assignments and exams must be done by individuals*

- **Cheating is a serious breach of trust and will not be tolerated**
  - If ever in doubt, don't do it or ask me immediately for a clarification
    - See University Policies for further detail
  - Take some free advice from me: Don't cheat, its not worth it.

VLSI Design - The Big Picture

- **Today we are generally designing VLSI systems for a particular embedded application:**
  - **Need to decompose design into sub-functions**
  - **Need to integrate the various sub-functions into a System-on-a-Chip**
  - **Guess what? Also need to write 1 million lines of code to make your system work.**
- **What do you do with a billion transistors?**
  - **The real question is how do you test a billion transistors to make sure they were manufactured correctly?**
  - **How do you co-verify a million lines of software and the billion transistors?**
- **What is the difference between Test, Verification and Validation?**

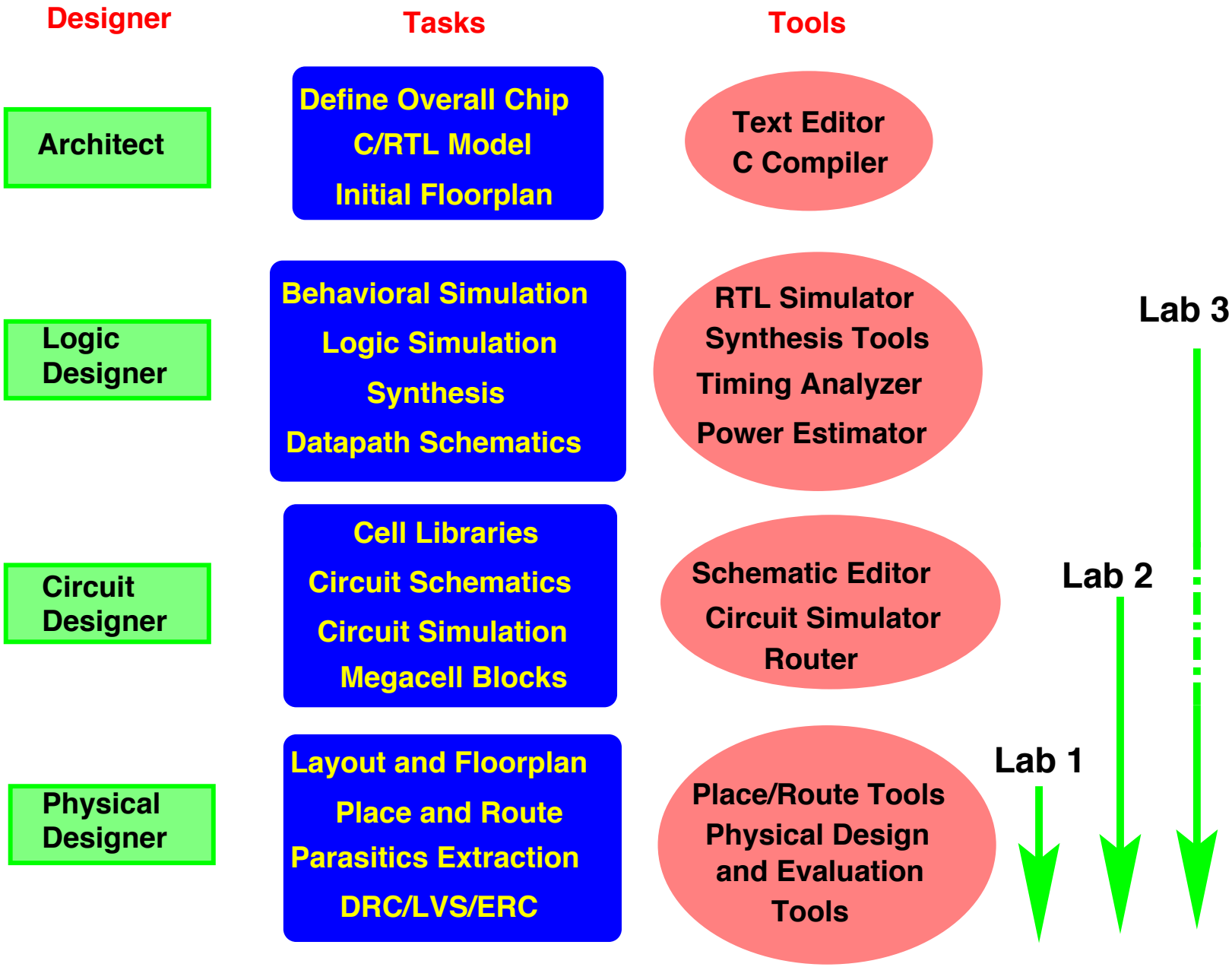
Types of IC Designs

- IC Designs can be Analog or Digital or both!!
- Digital designs can be one of three groups
  - Full Custom
    - Every transistor designed and laid out by hand
  - ASIC (Application-Specific Integrated Circuits)
    - Designs synthesized automatically from a high-level language description
  - Semi-Custom or structured custom
    - Mixture of custom and synthesized modules
- Analog designs are generally full custom
  - Digitally assisted Analog is a combination of full custom and ASIC

Laboratory Exercises

- **Lab Exercise 1**
  - Design, layout and evaluation of a register file
    - Use Cadence layout software, HSpice simulation
- **Lab Exercise 2**
  - Design and evaluation of an ALU with standard cell libraries
    - Cadence schematic editor, Synopsys static timing analysis, Cadence place-and-route
- **Lab Exercise 3**
  - RTL/HDL level design and evaluation of bus controller
    - Synopsys simulation, Synopsys synthesis, Cadence place-and-route

Laboratory Exercises



Purpose of Lab Exercises

- Familiarity with layout, circuit simulation, timing
- Learn schematic design, timing optimization
- Learn register-transfer-level (RTL) design, system simulation, logic synthesis and place-and-route using mix of tools from different vendors that mirrors industry standards

Laboratory Design Tools

- **We will us commercial CAD tools**
  - Cadence, Synopsys, etc.

- **Commercial software is powerful, but very complex**
  - Designers sent to long training classes
  - Students will benefit from using the software, but we don't have the luxury of long training
  - TAs have experience with the software

- **Start work early in the lab**
  - Plan designs carefully and save your work frequently.

Caveats about Design Tools

- Never take anything on blind faith. Work it out -- make sure it works. Many clever circuits that are published either don't work or are very sensitive to certain conditions. Be careful.

- There are NO RIGHT answers, and there are no PERFECT circuits. Everything has its warts. A good circuit simply has the right set of warts to meet the constraints of the problem.

- Simulation is NO substitute for thinking. Simulators can make your job much easier, but it also can make it incredibly harder. Like all tools it helps only if you use it well, AND that requires thinking. Work it out on paper and then let the simulator validate it.

DO NOT BECOME a SLAVE to the TOOLS.

Tools can and <u>will</u> tell you wrong answers.

Courtesy of Mark Horowitz

Back to the beginning: a little history lesson….

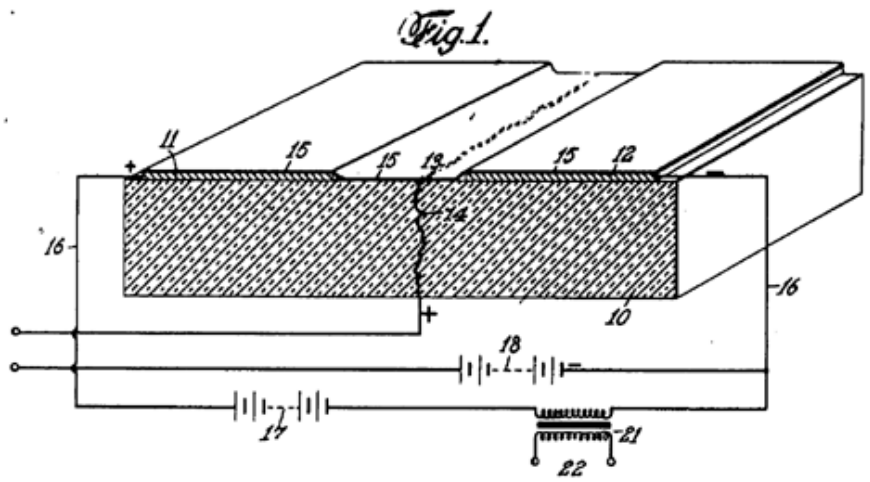
A Brief History of the Transistor

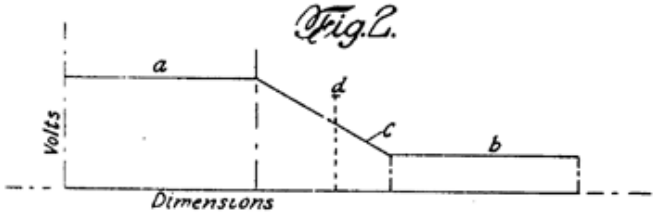
- Some of the events which led to the microprocessor
- Photographs in the following are from "State of the Art: A photographic history of the integrated circuit", Stan Augarten, Ticknor & Fields, 1983.
  - They can also be viewed on the Smithsonian web site http://smithsonianchips.si.edu/
  - Another web site http://www.pbs.org/transistor/
- Another collection of interesting chip photos and other things.
  - http://micro.magnet.fsu.edu/creatures/pages/chili.html

Early Ideas Leading to the Transistor

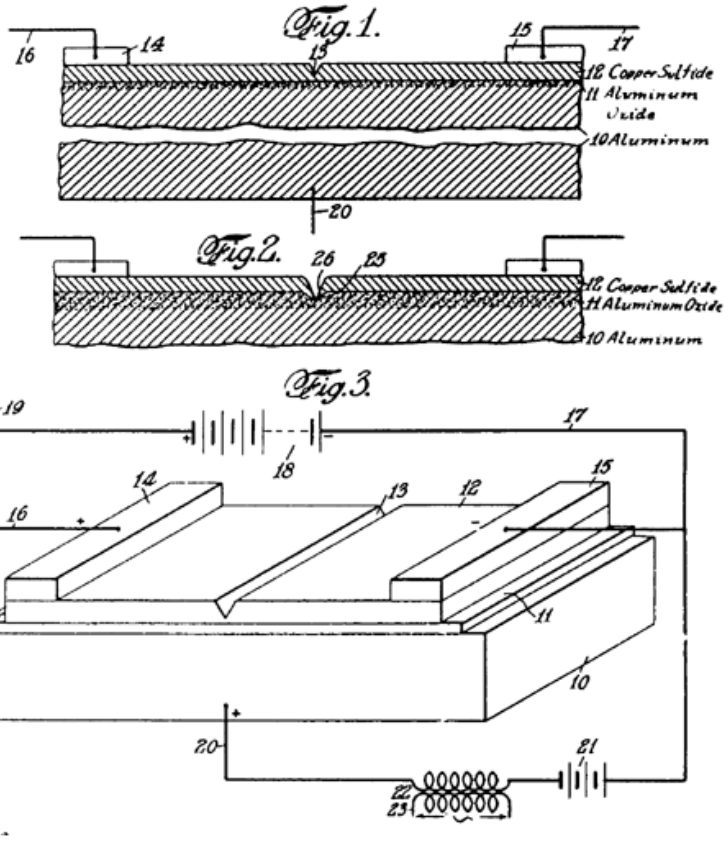
- **J. W. Lilienfeld's patents**

1930: "Method and apparatus for controlling electric currents", U.S. Patent 1,745,175





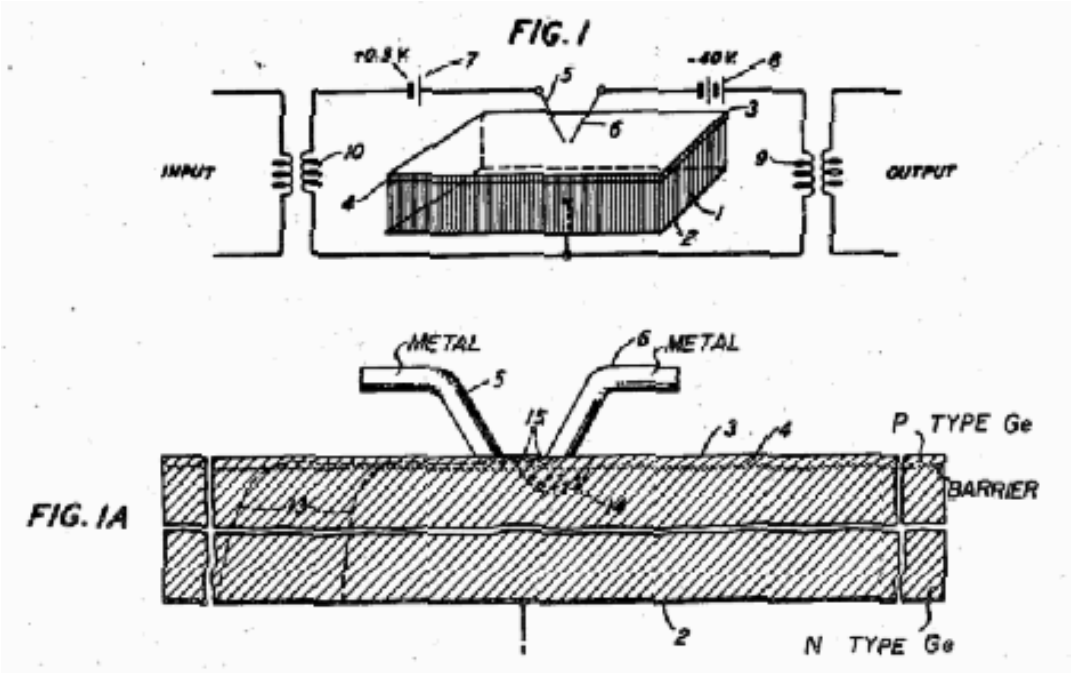
1933: "Device for controlling electric current", U. S. Patent 1,900,018

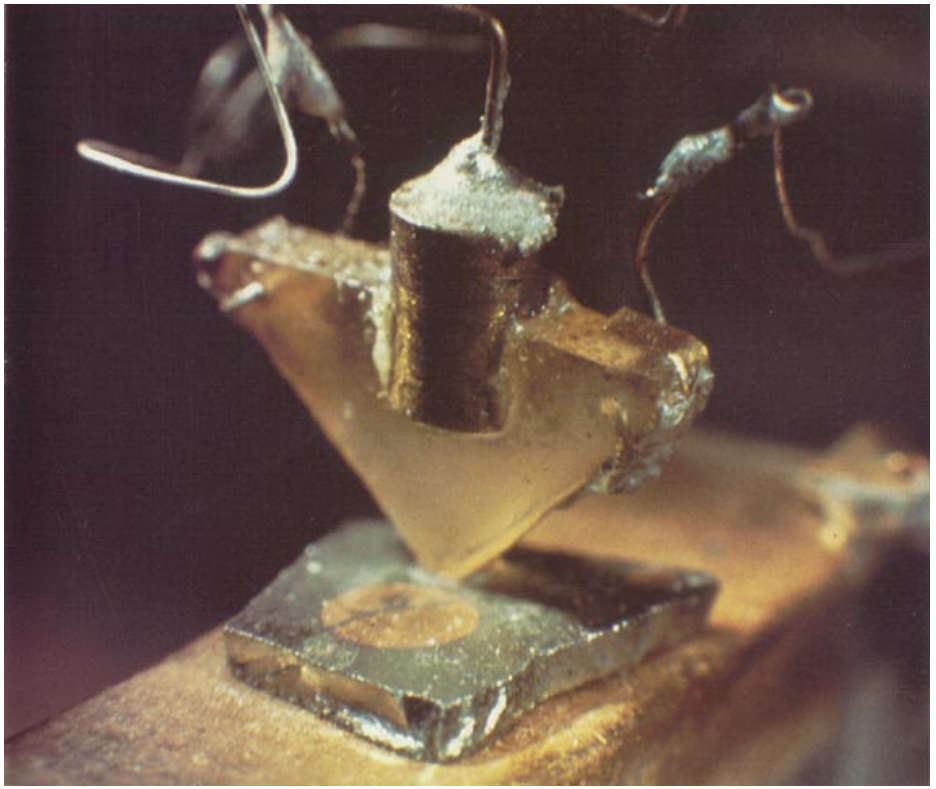


Key Developments at Bell Labs

- **1940: Ohl develops the PN Junction**
- **1945: Shockley's laboratory established**
- **1947: Bardeen and Brattain create point contact transistor (U.S. Patent 2,524,035)**

Diagram from patent application

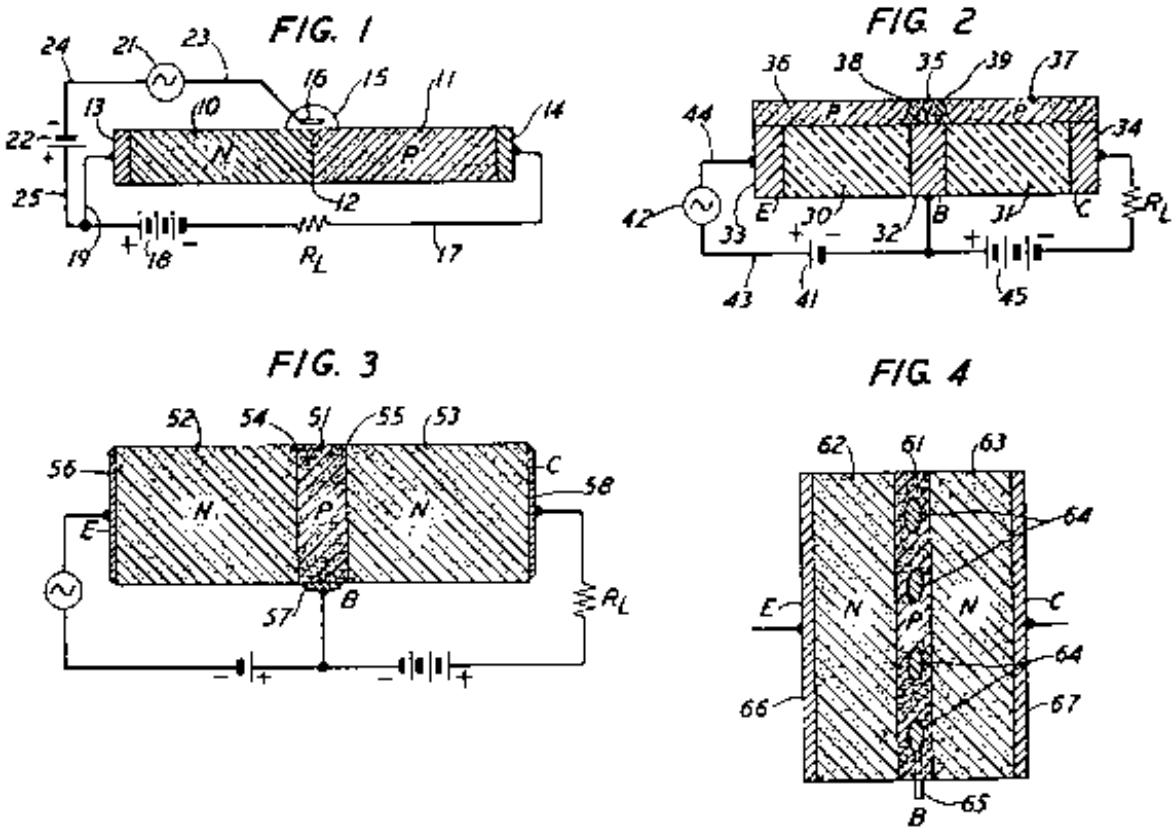


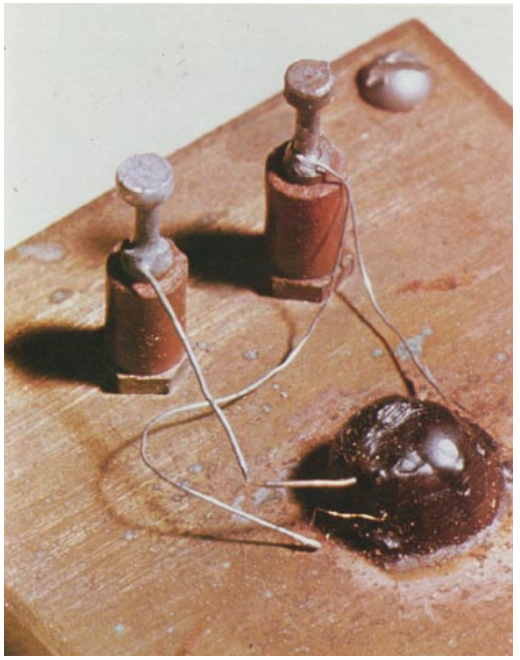


Developments at Bell Labs, Cont'd

- **1951: Shockley develops a junction transistor manufacturable in quantity (U.S. Patent 2,623,105)**

Diagram from patent application





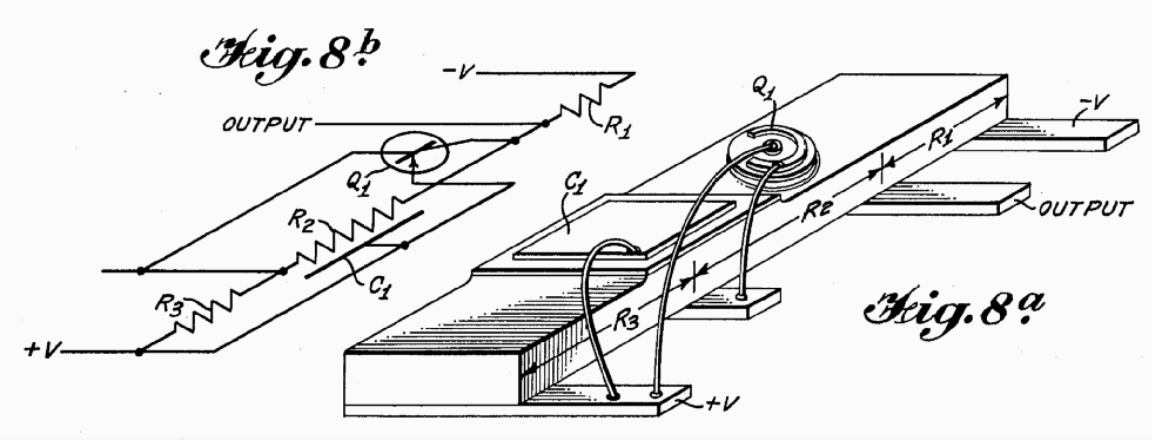
1950s – Silicon Valley

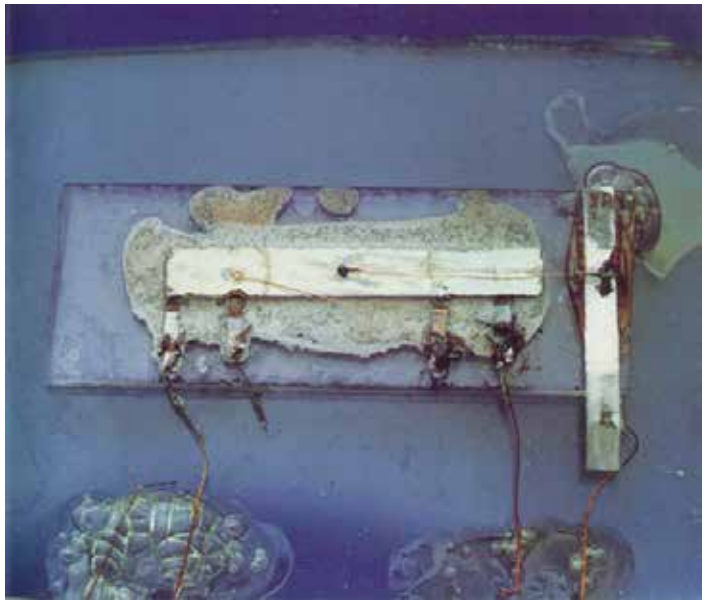
- 1950s: Shockley in Silicon Valley
- 1955: Noyce joins Shockley Laboratories
- 1954: The first transistor radio
- 1957: Noyce leaves Shockley Labs to form Fairchild with Jean Hoerni and Gordon Moore
- 1958: Hoerni invents technique for diffusing impurities into Si to build planar transistors using a SiO2 insulator
- 1959: Noyce develops first true IC using planar transistors, back-to-back PN junctions for isolation, diode-isolated Si resistors and SiO2 insulation with evaporated metal wiring on top

The Integrated Circuit (IC)

- **1959: Jack Kilby, working at TI, dreams up the idea of a monolithic "integrated circuit"**
  - **Components connected by hand-soldered wires and isolated by "shaping", PN-diodes used as resistors (U.S. Patent 3,138,743)**

Diagram from patent application

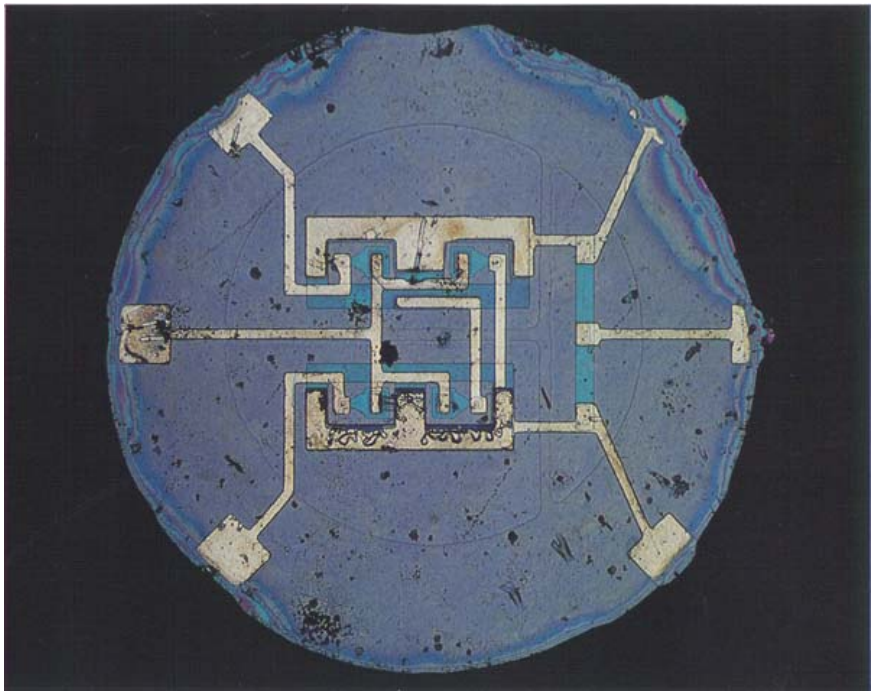




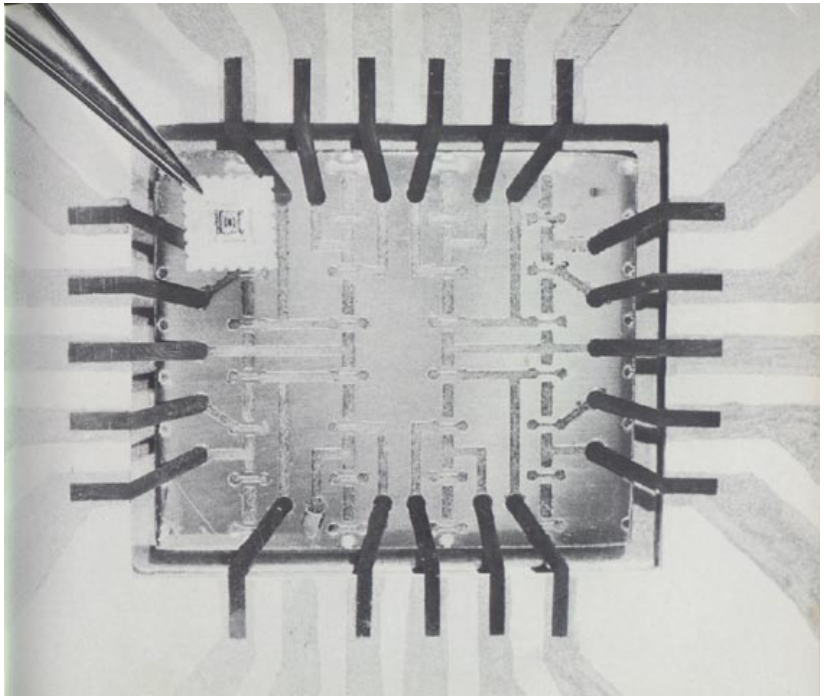
ICs, Cont'd

- **1961: TI and Fairchild introduce the first logic ICs ($50 in quantity)**
- **1962: RCA develops the first MOS transistor**

Fairchild bipolar RTL Flip-Flop

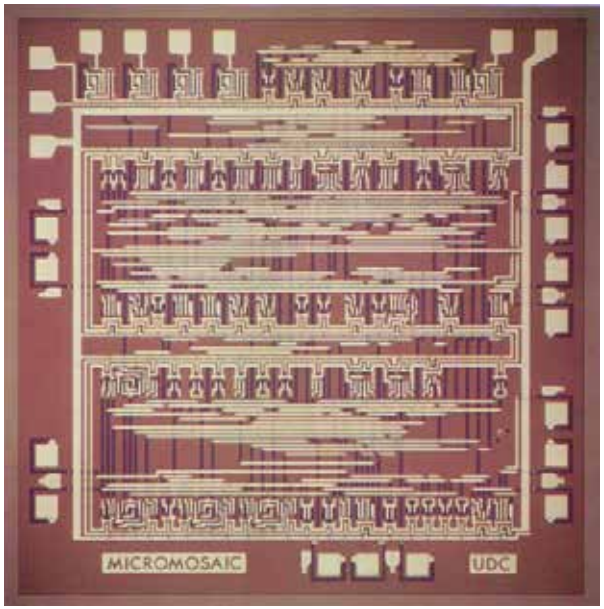


RCA 16-transistor MOSFET IC



Computer-Aided Design (CAD)

- **1967: Fairchild develops the "Micromosaic" IC using CAD**
  - **Final Al layer of interconnect could be customized for different applications**

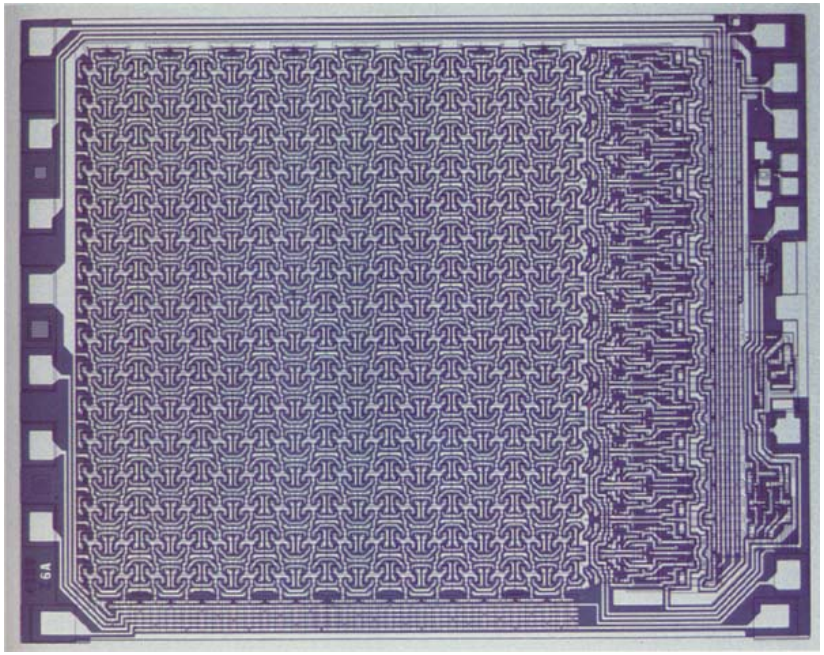


- **1968: Noyce, Moore leave Fairchild, start Intel**

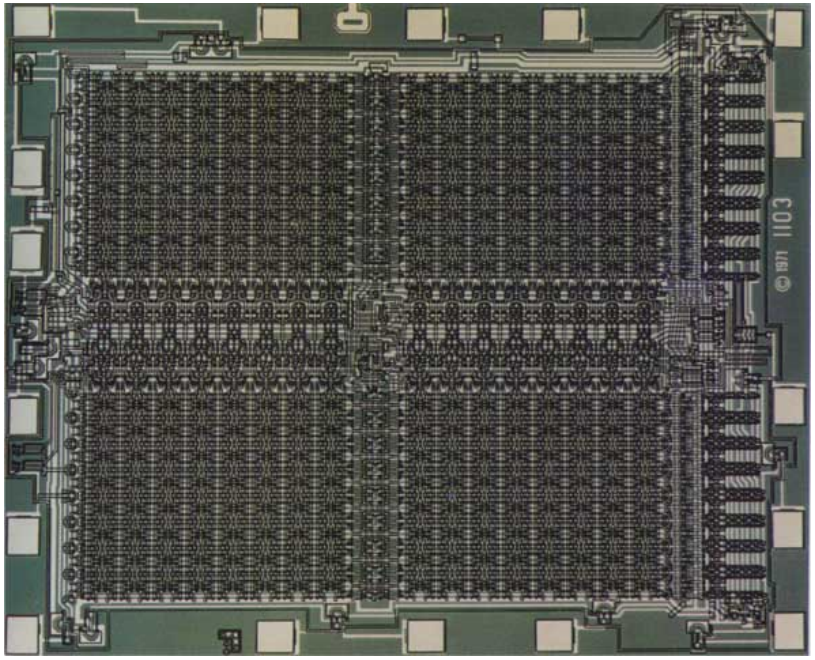
Static and Dynamic RAMs

- **1970: Fairchild introduces the 4100, 256-bit Static RAM**
- **1970: Intel starts selling a1K-bit Dynamic RAM, the 1103**

Fairchild 4100 256-bit SRAM

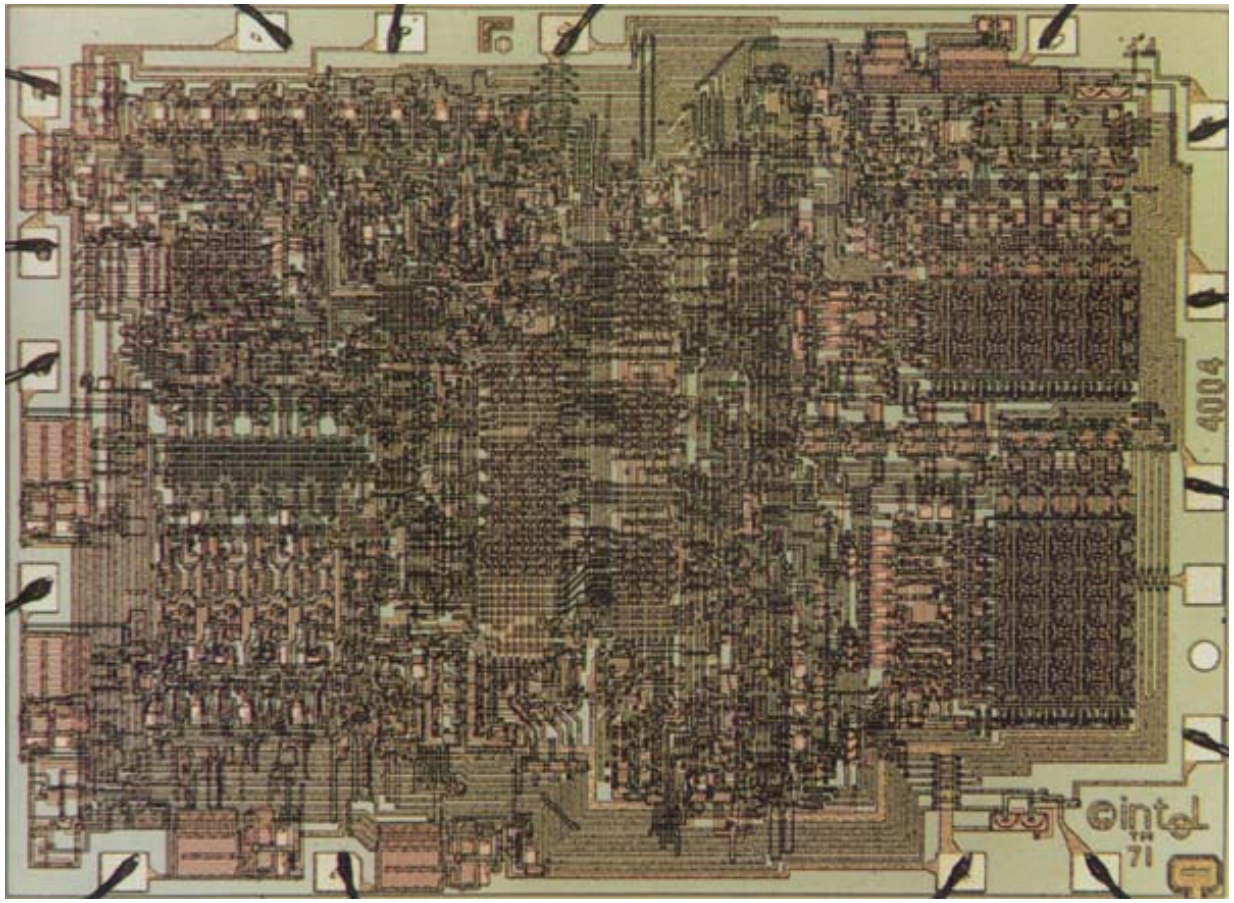


Intel 1103 1K-bit DRAM



The Microprocessor!

- **1971: Intel introduces the first microprocessor, the 4004 (originally designed as a special circuit for a customer)**

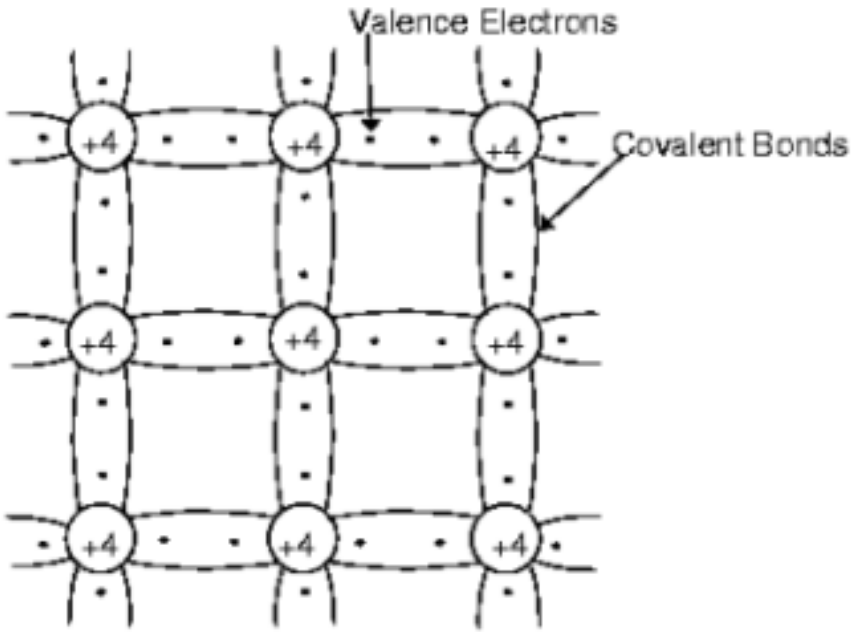


- **1975: Mark McDermott designs and fabricates his first chip.**

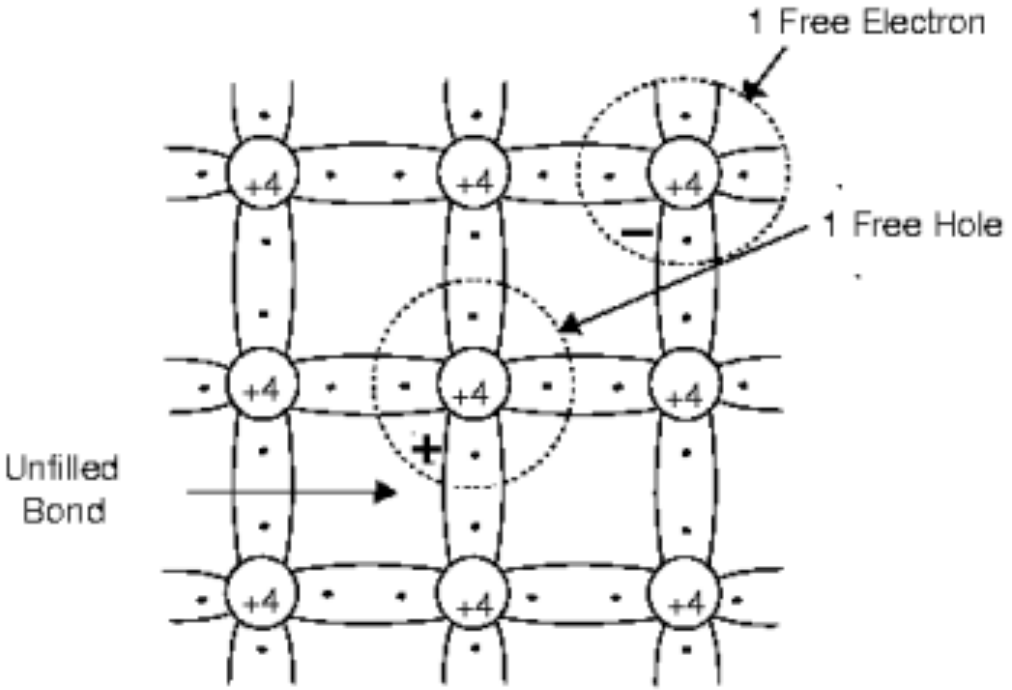
Now, a brief review before we dive into the fun stuff….

Conductivity in Silicon Lattice

- At temperatures close to 0° K, electrons in outermost shell are tightly bound (insulator)
- At higher temps., (300° K), some electrons have thermal energy to break covalent bonds



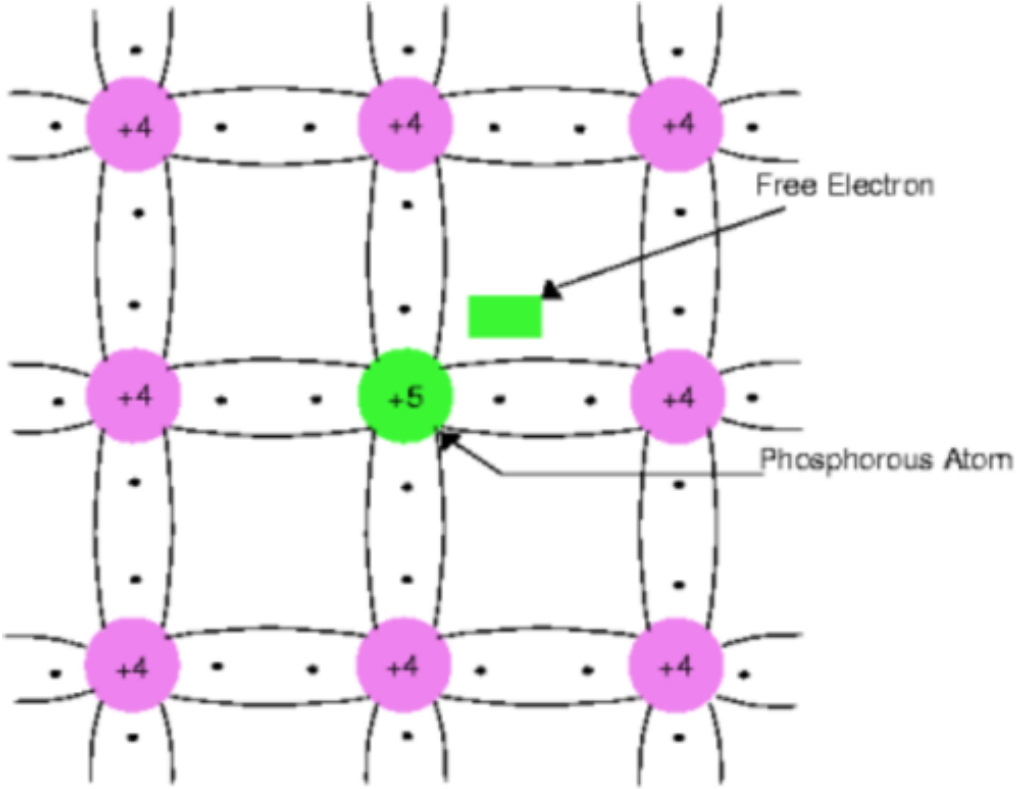
Silicon Lattice With No Free Electron



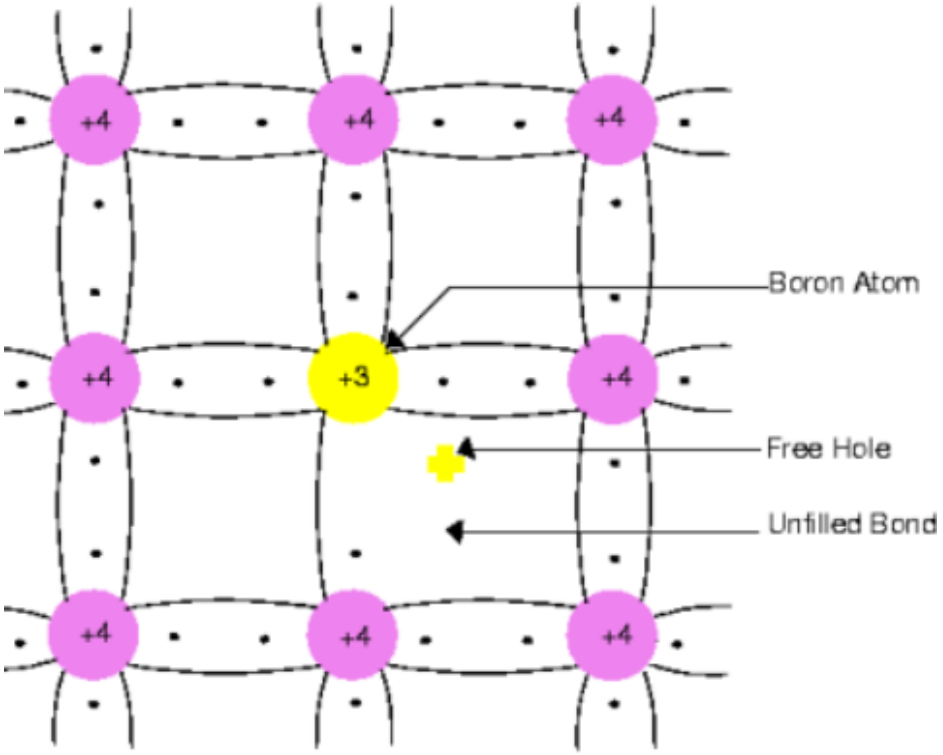
Silicon Lattice With One Covalent Bond Broken

Conductivity in Semiconductors

- **Pure Silicon may be mixed with impurities to change the number of available carriers**



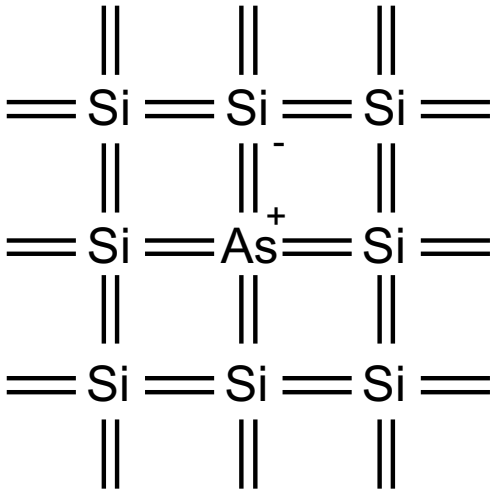
The Effect Of N–Type Doping

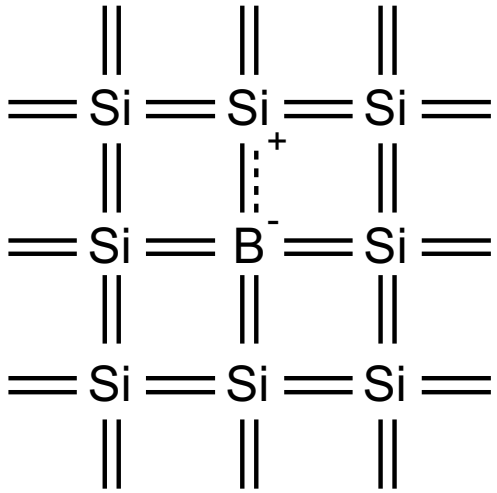


The Efect Of P–Type Doping

Dopants

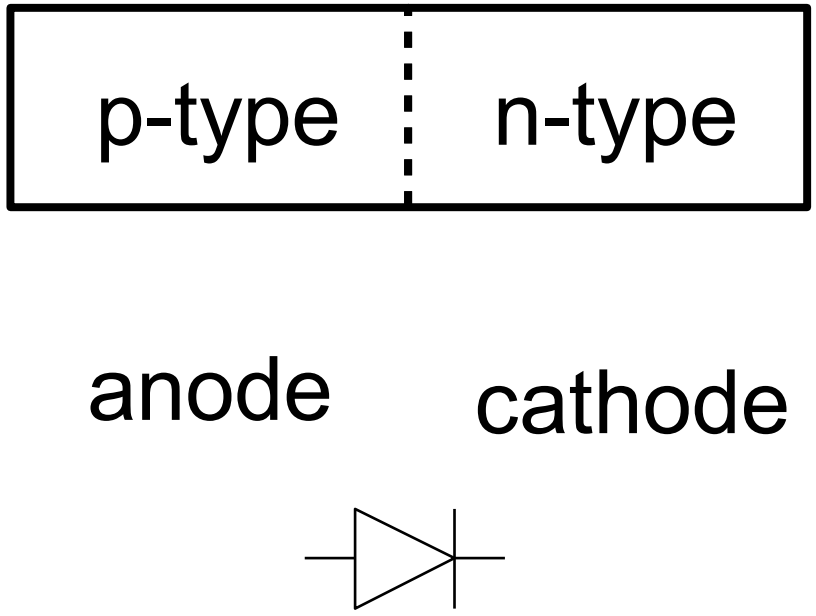
- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)





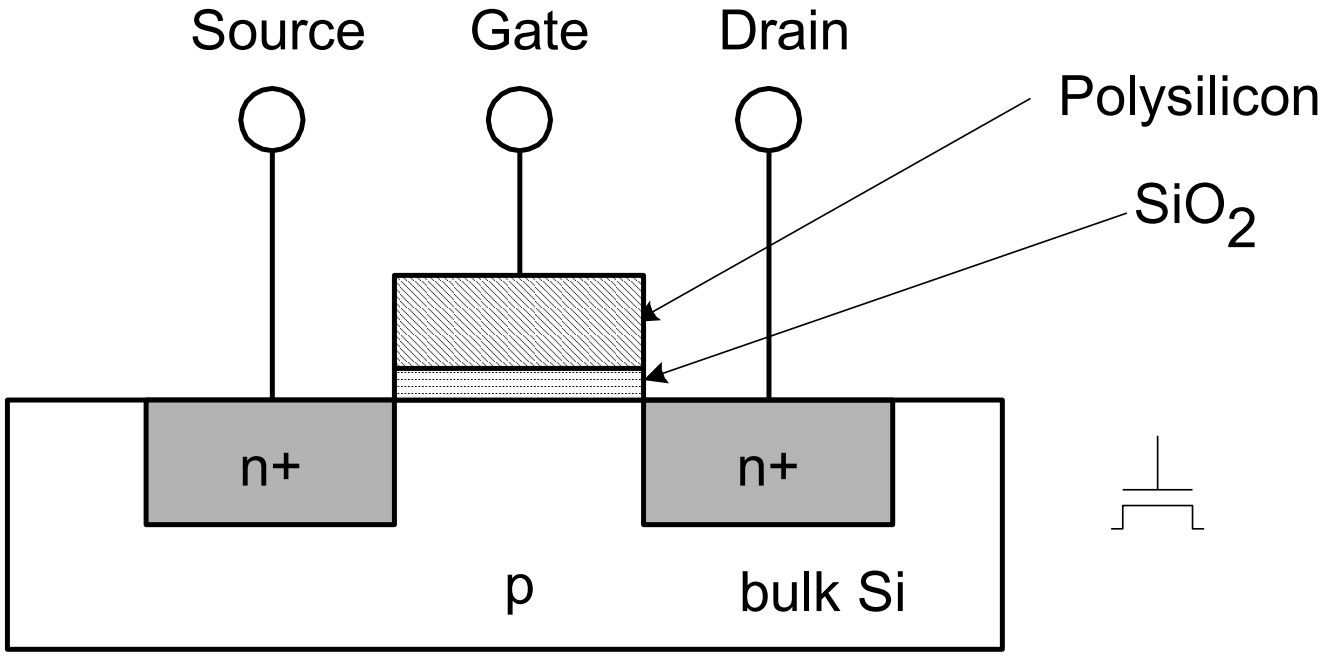
p-n Junctions

- **A junction between p-type and n-type semiconductor forms a diode.**
- **Current flows only in one direction**



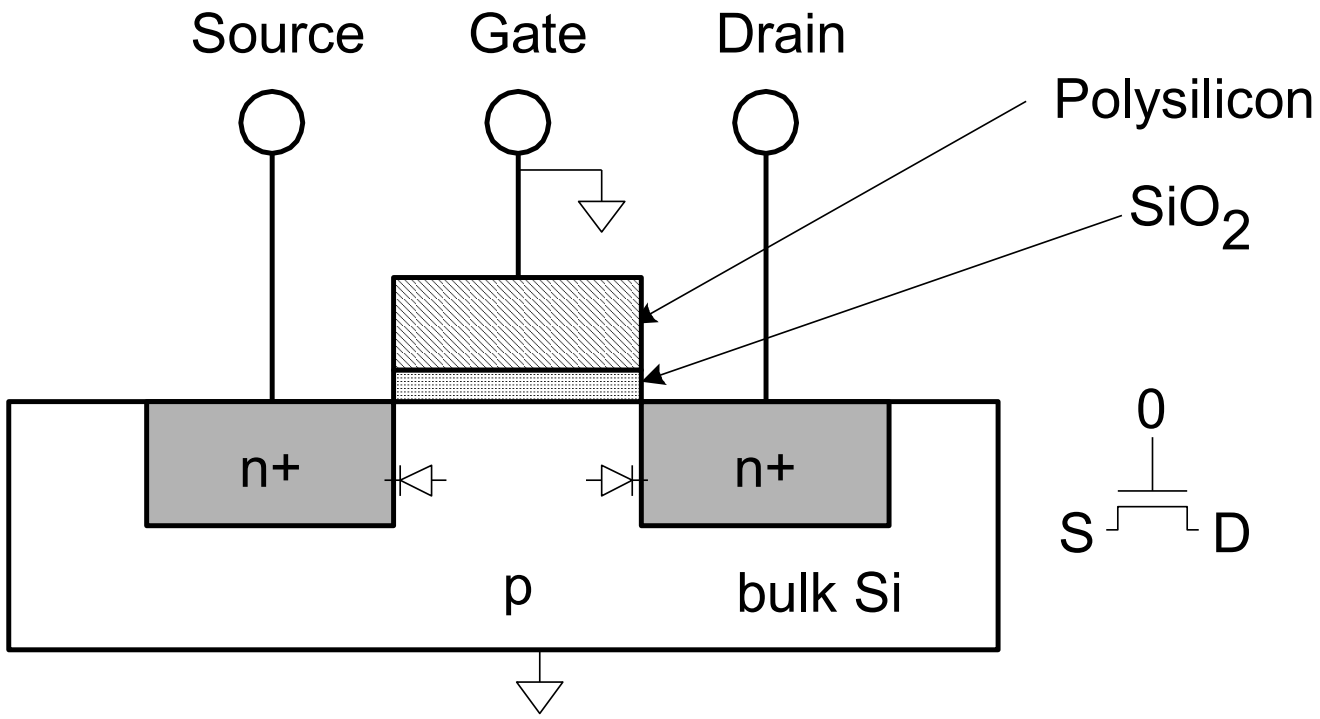
nMOS Transistor

- **Four terminals: gate, source, drain, body**
- **Gate – oxide – body stack looks like a capacitor**
  - **Gate and body are conductors**
  - **SiO_2 (oxide) is a very good insulator**
  - **Called metal – oxide – semiconductor (MOS) capacitor**
  - **Even though the gate is no longer made of metal**
    - **Not true for 45nm and beyond.**



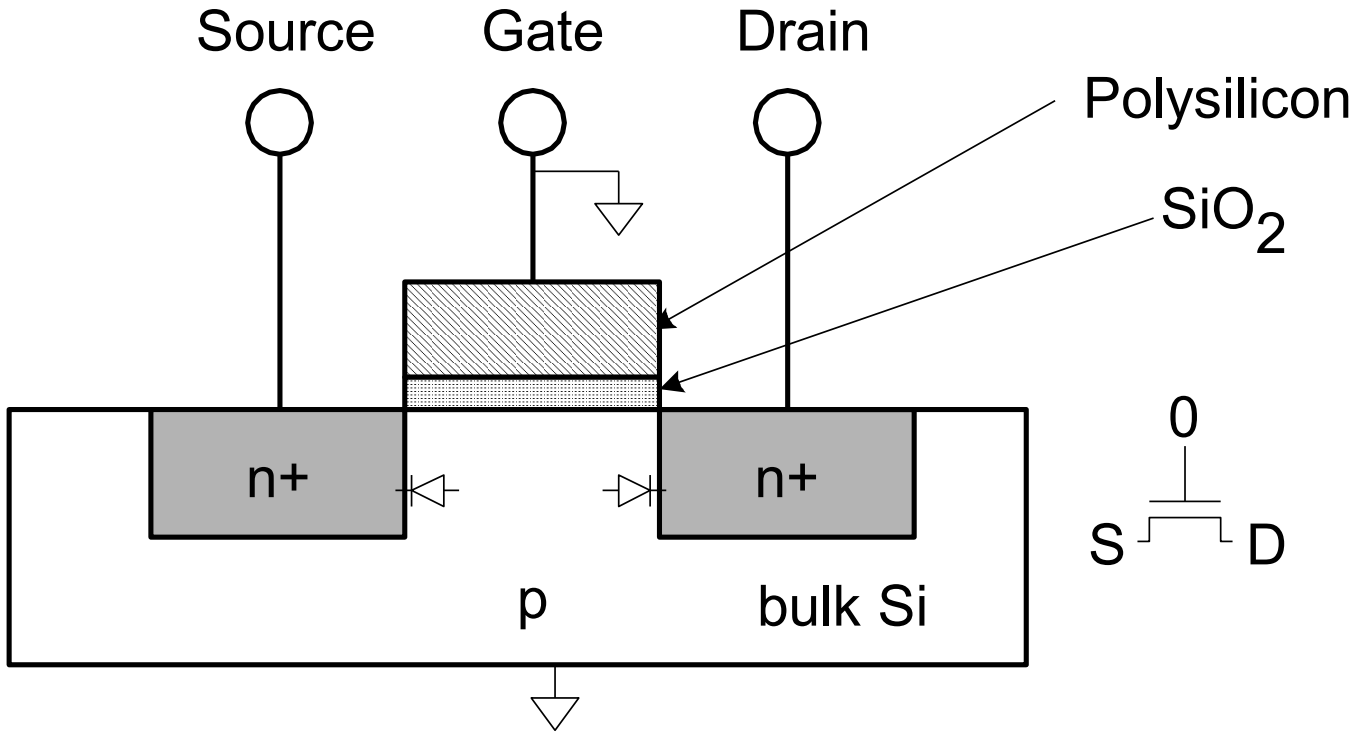
nMOS Operation

- **Body is commonly tied to ground (0 V)**
- **When the gate is at a low voltage:**
  - **P-type body is at low voltage**
  - **Source-body and drain-body diodes are OFF**
  - **No current flows, transistor is OFF**



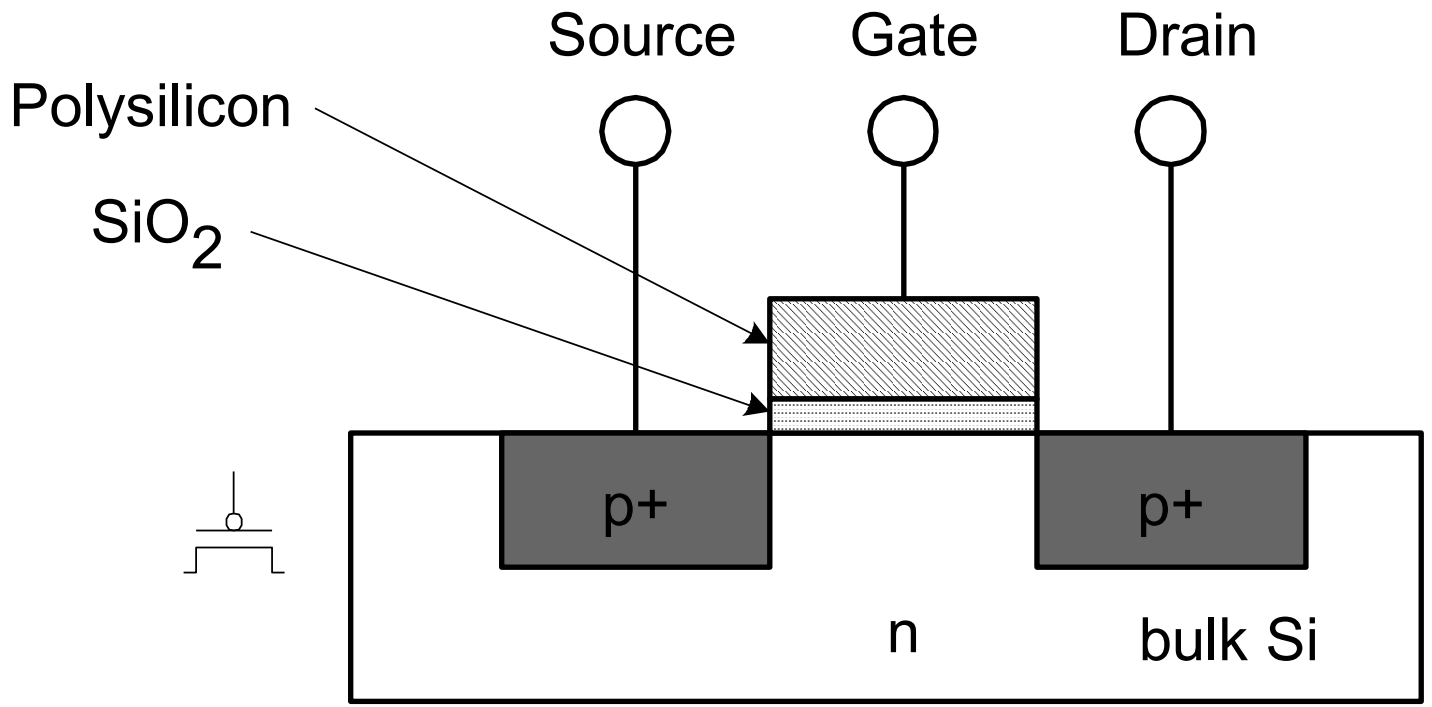
nMOS Operation (cont)

- **When the gate is at a high voltage:**
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



pMOS Transistor

- **Similar, but doping and voltages reversed**
  - **Body tied to high voltage (VDD)**
  - **Gate low: transistor ON**
  - **Gate high: transistor OFF**
  - **Bubble indicates inverted behavior**

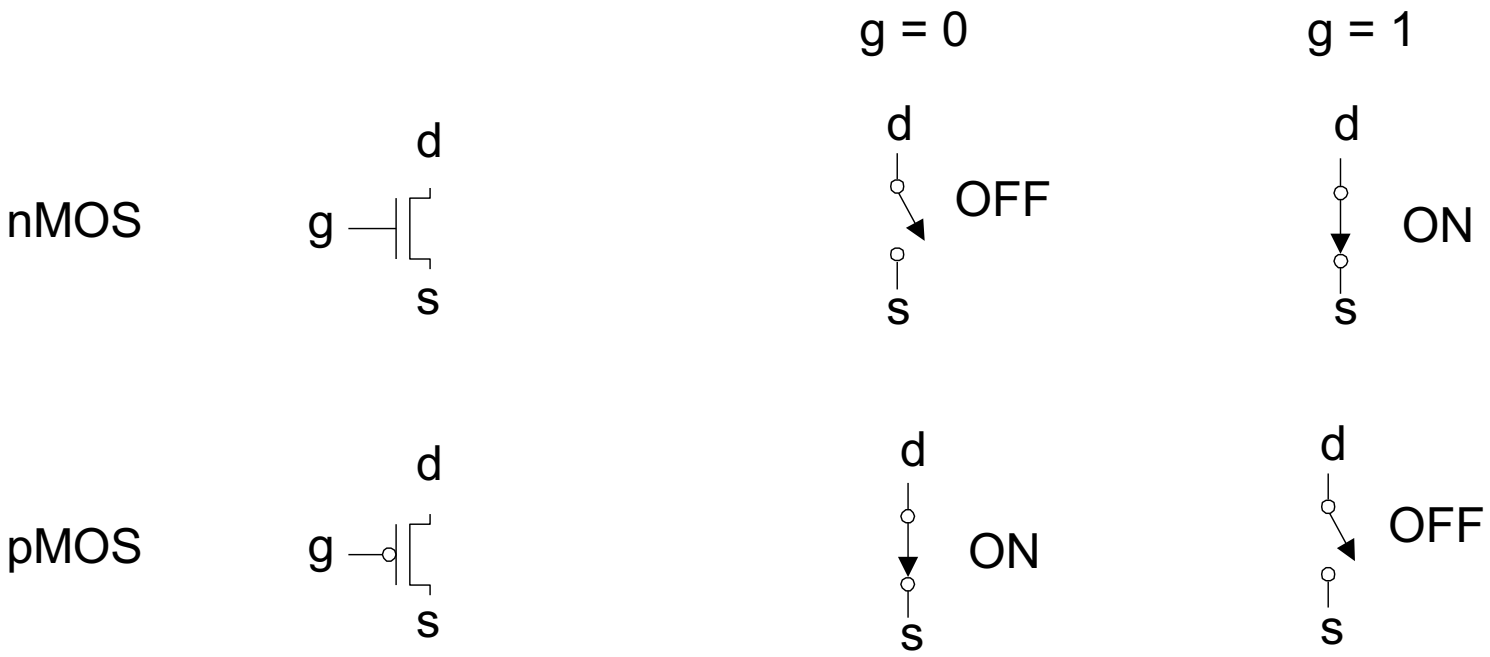


Power Supply Voltage

- In 1970's VDD = 12-18V for Metal Gate CMOS
- In 1980's, VDD = 5V
- VDD has decreased in modern processes
  - High VDD would damage modern tiny transistors
  - Lower VDD saves power
- VDD = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, 0.8, 0.7, 0.6
- GND = 0 V

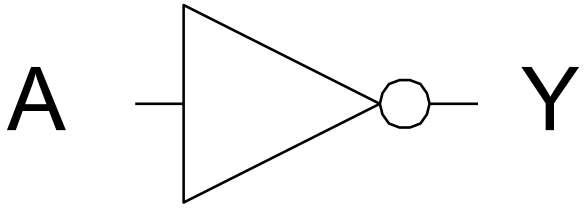
Transistors as Switches

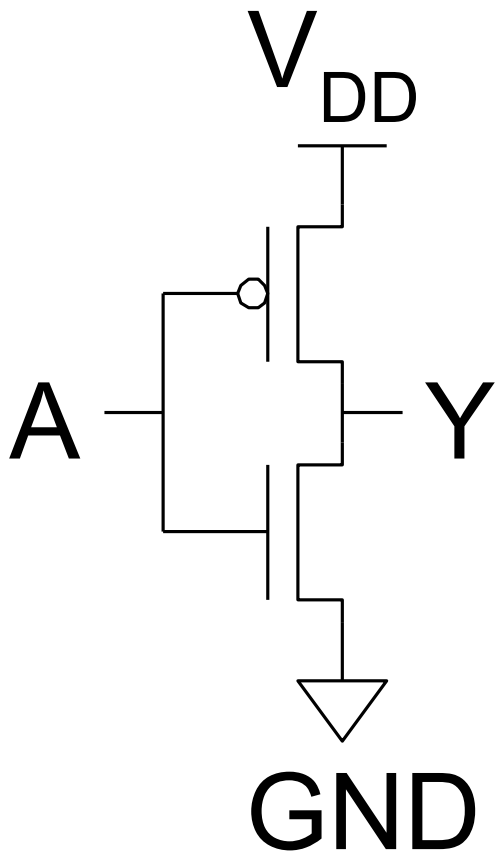
- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS Inverter

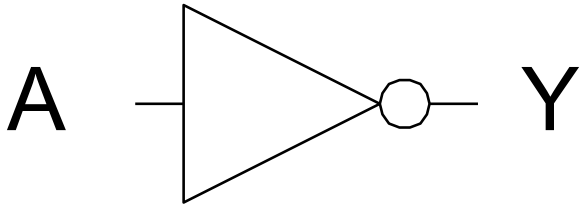
A	Y
0	
1	

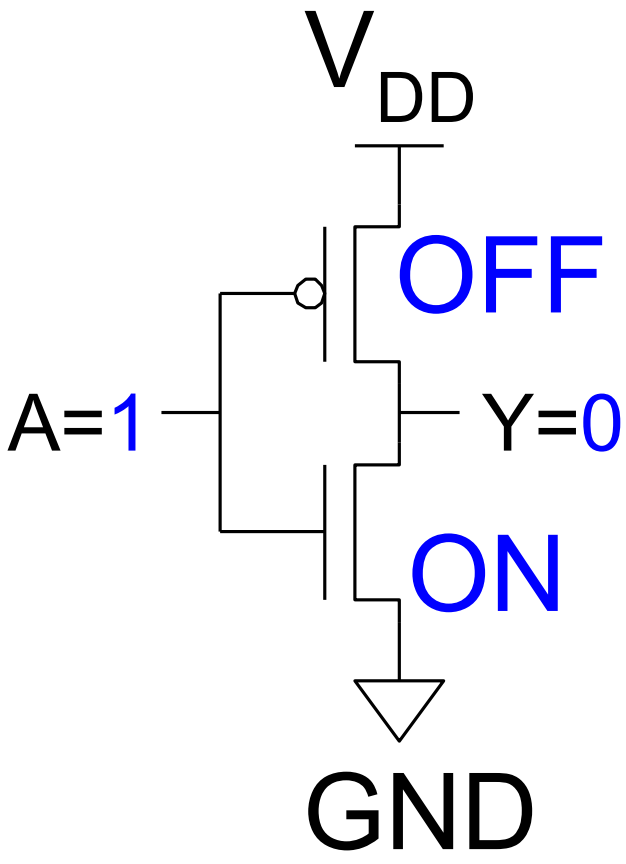




CMOS Inverter

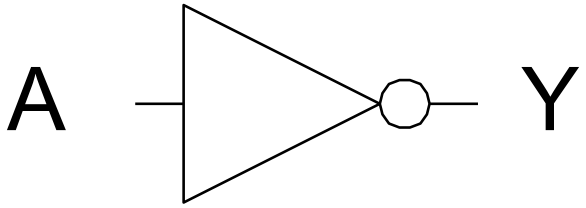
A	Y
0	
1	**0**

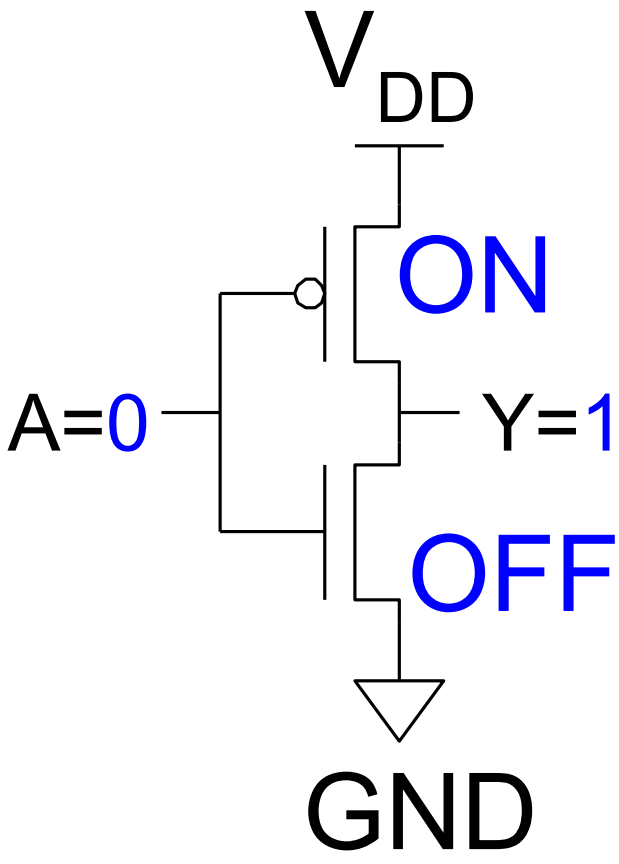




CMOS Inverter

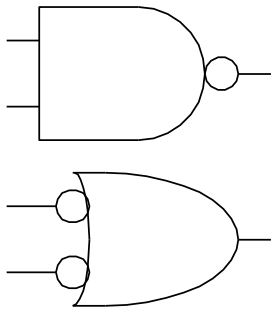
A	Y
0	**1**
1	0

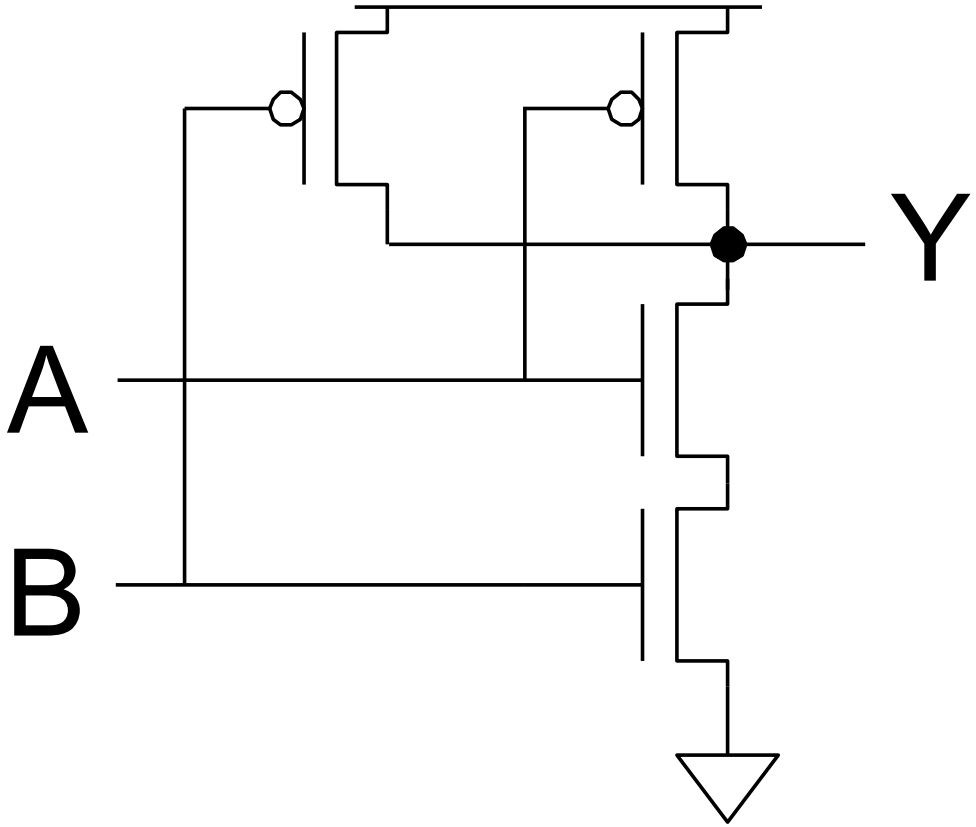




CMOS NAND Gate

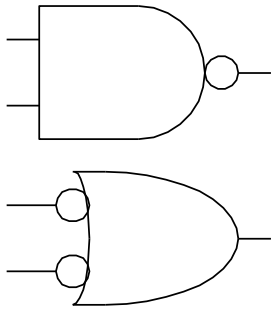
A	B	Y
0	0	
0	1	
1	0	
1	1	

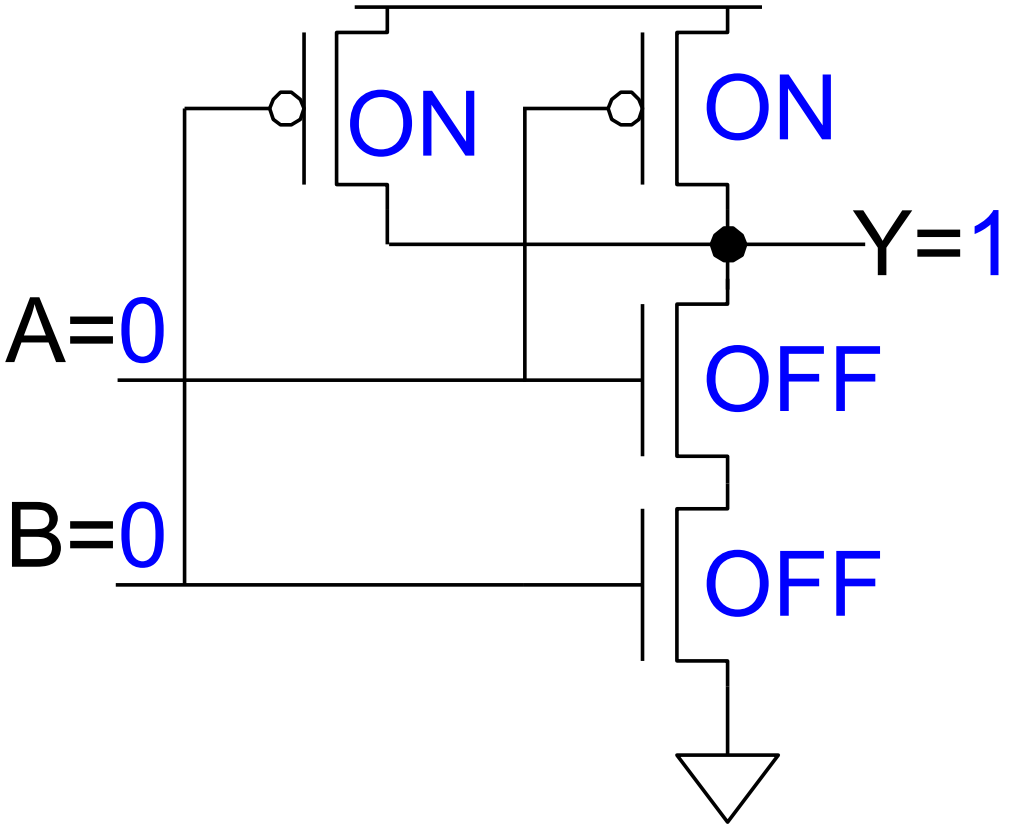




CMOS NAND Gate

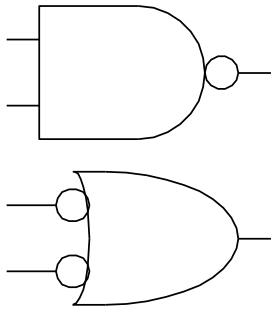
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

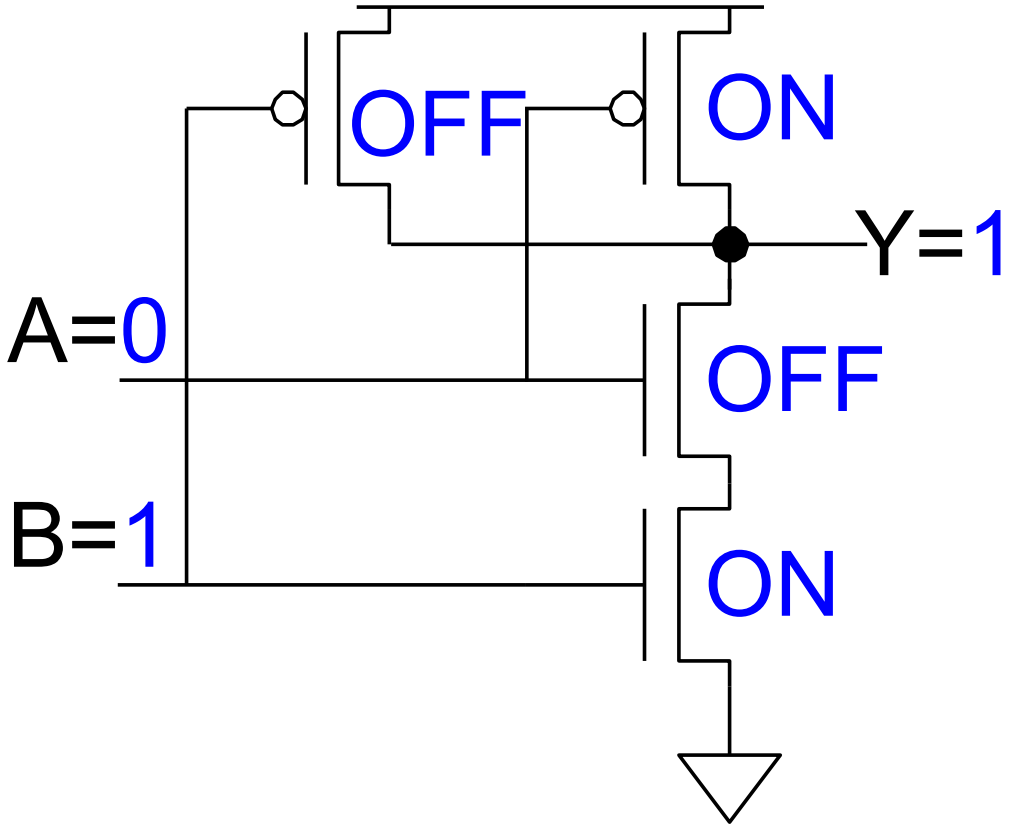




CMOS NAND Gate

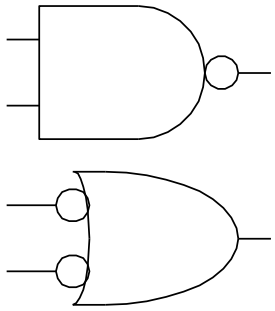
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

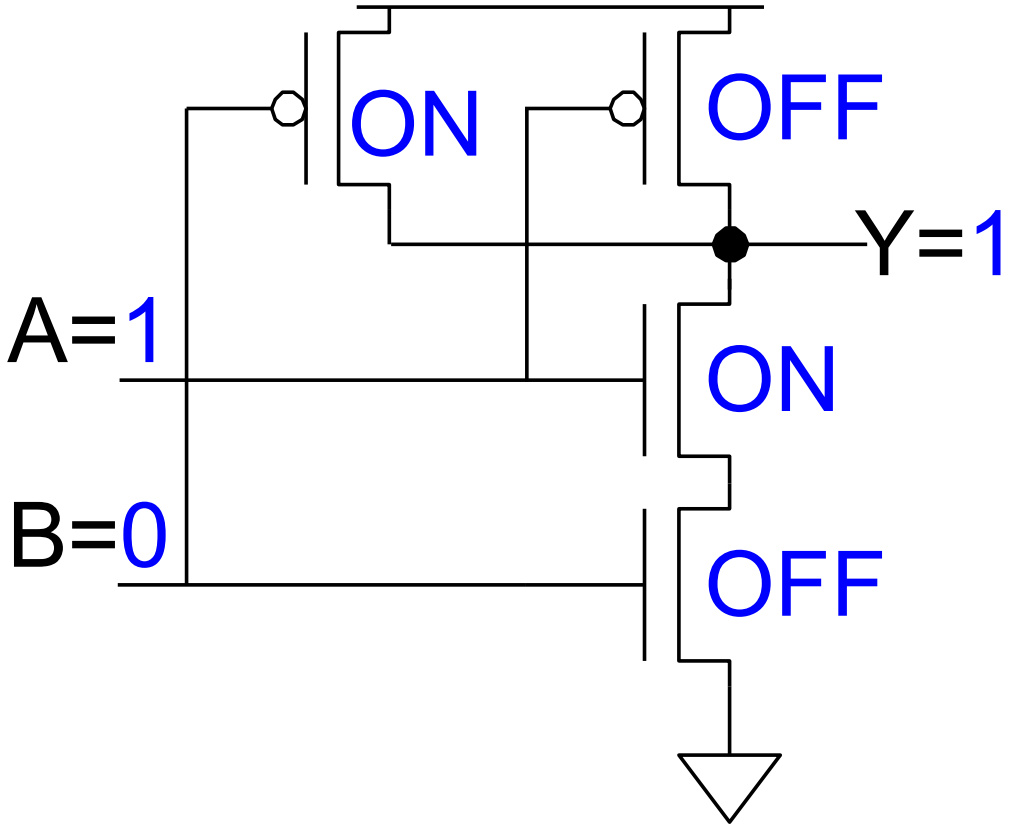




CMOS NAND Gate

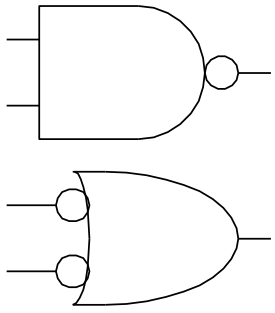
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

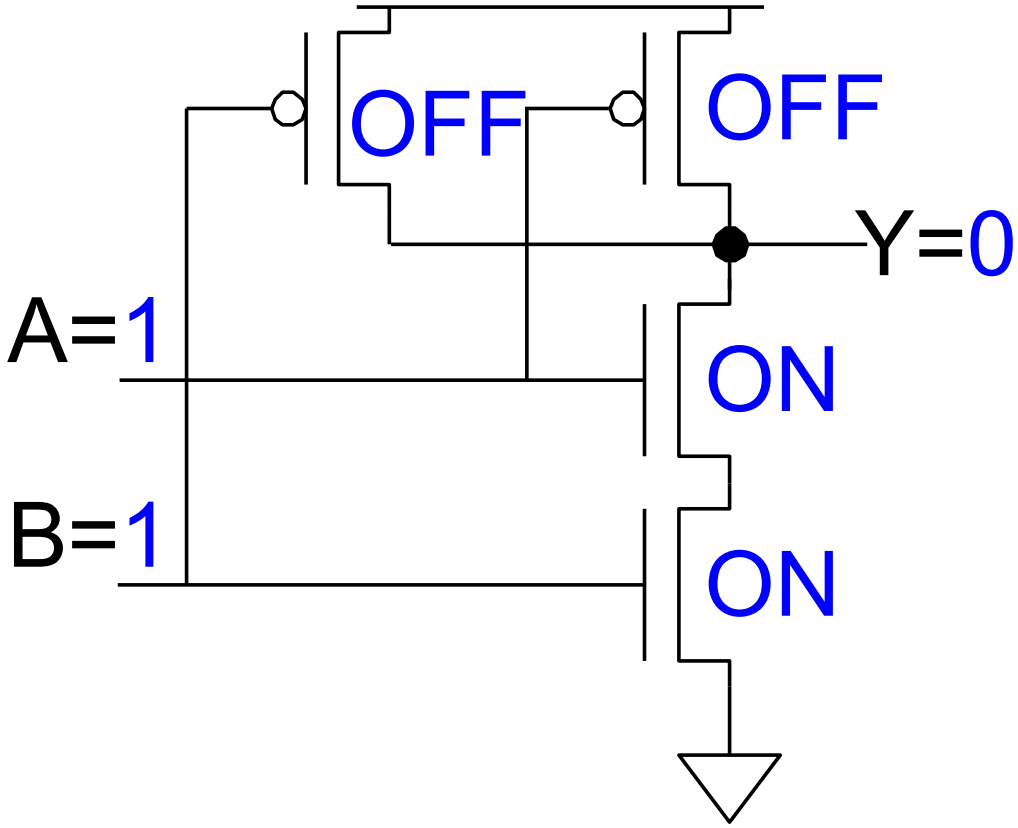




CMOS NAND Gate

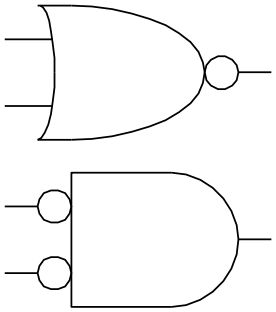
A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

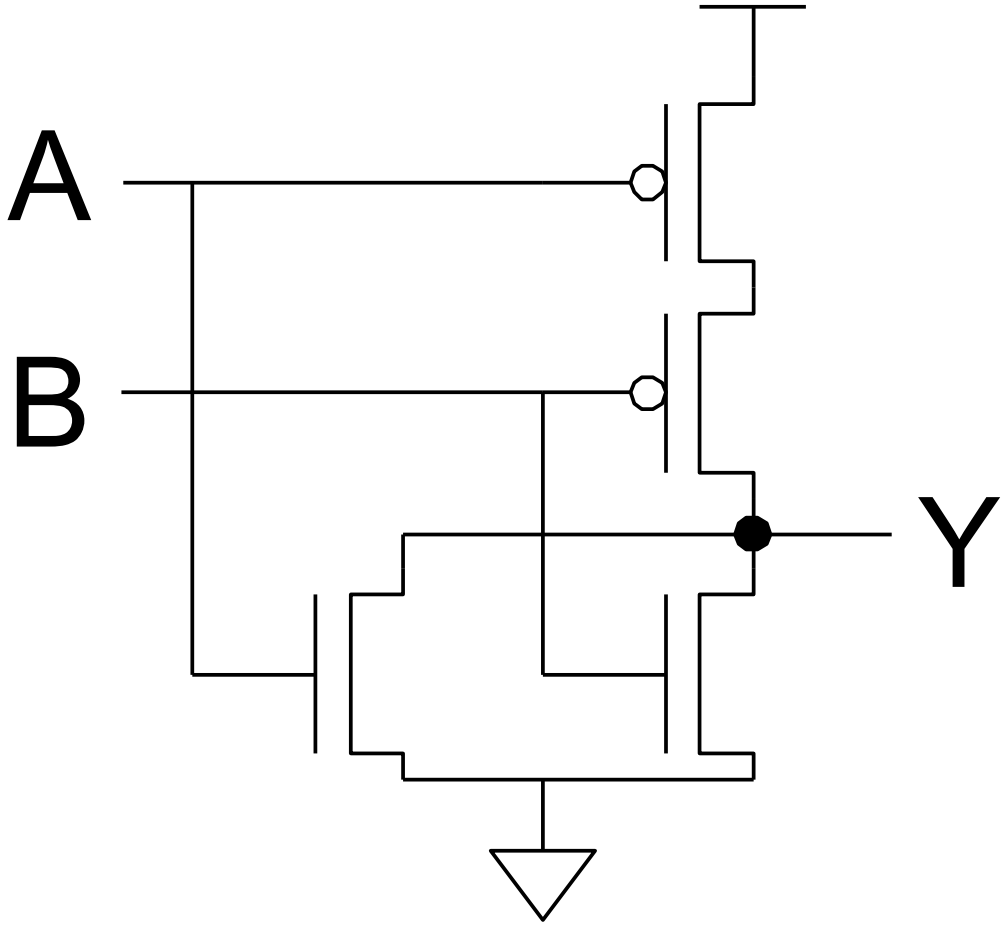




CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



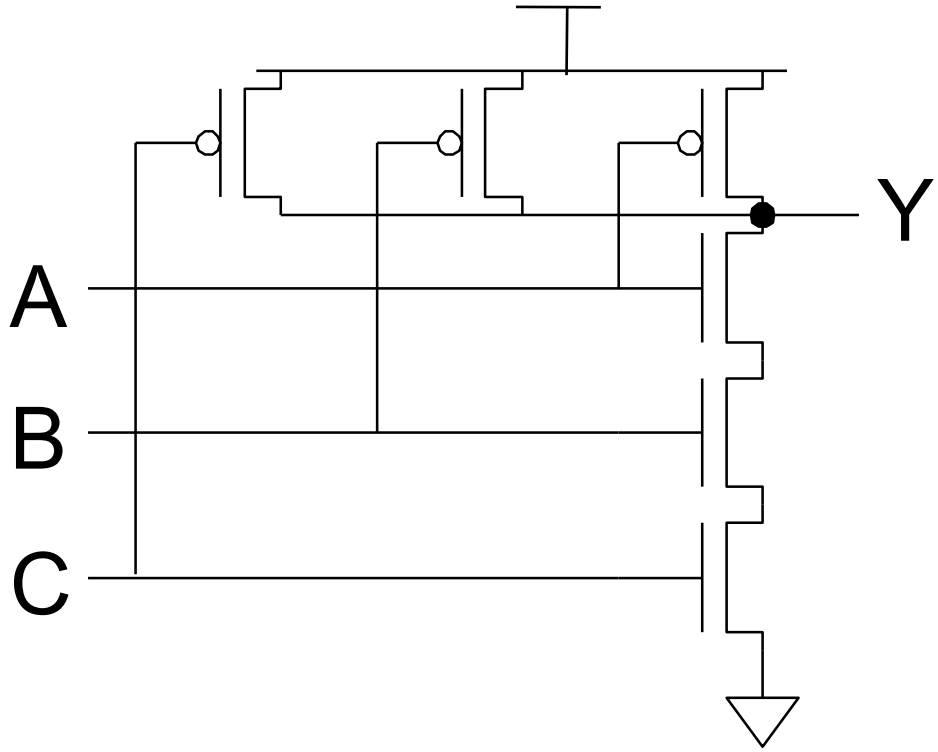


3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

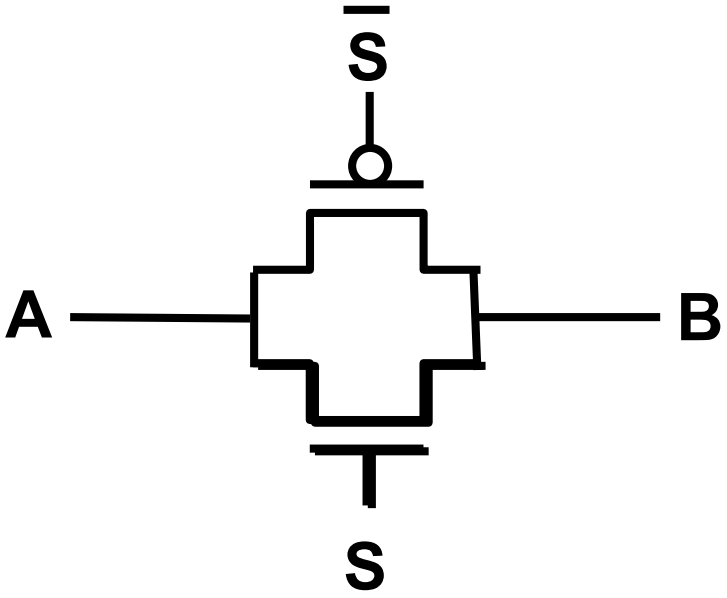


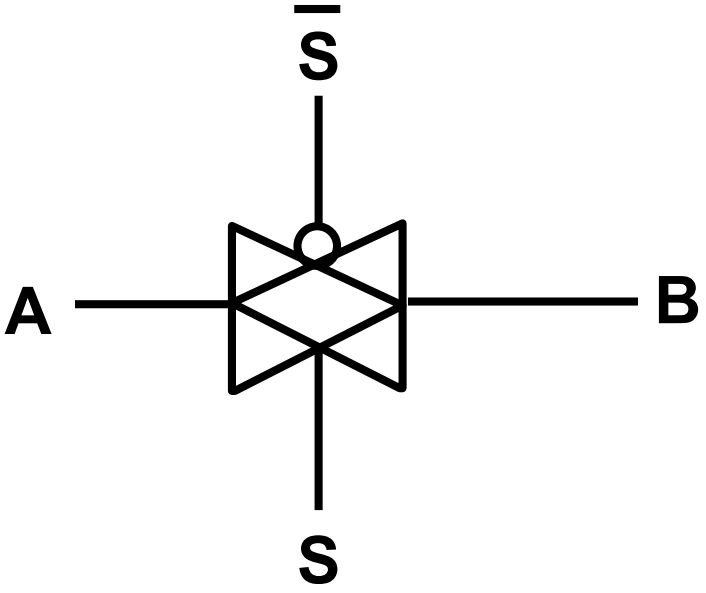
Characteristics of CMOS Gates

- **In general, when the circuit is stable**
  - **There is a path from one supply (VSS or VDD) to the output (low static power dissipation)**
  - **There is NEVER a path from one supply to another**
- **There is a momentary drain of current when a gate switches from one state to the other**
  - **Dynamic power dissipation**
- **If a node has no path to power or ground, the previous value retained due to the capacitance of the node.**
  - **Don't count on it though. Leakage is so bad in DSM that the charge will be lost.**

Complementary Switch (Transmission Gate)

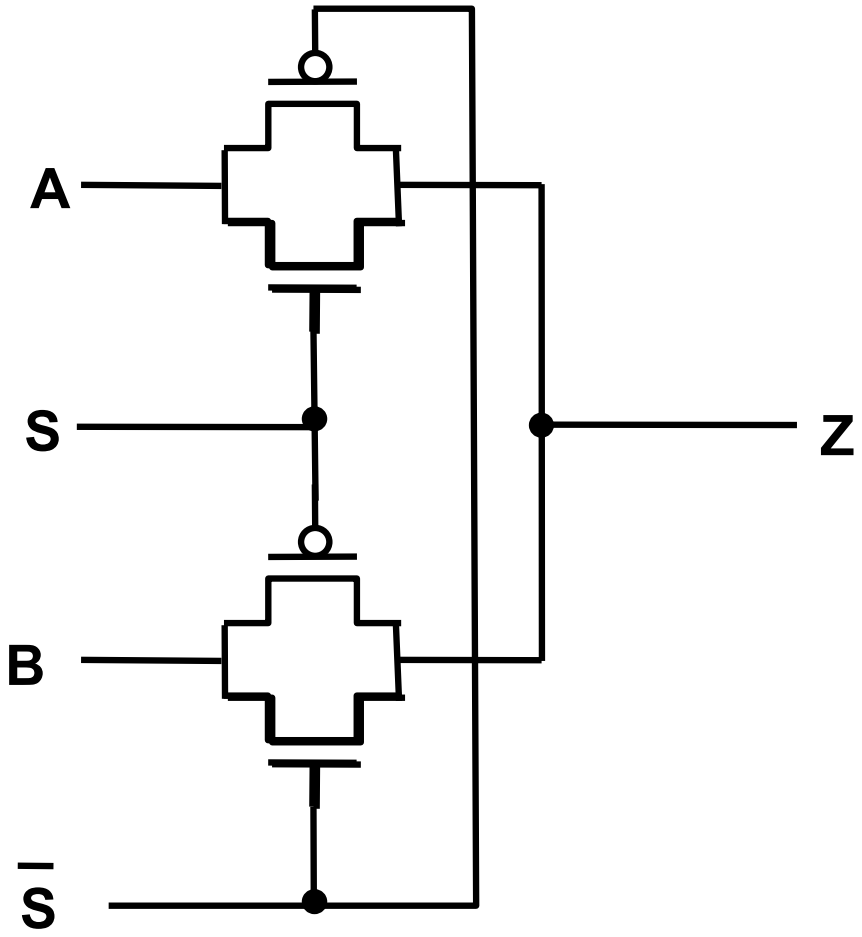
- Combine n- and p-channel switches in parallel to get a switch which passes both "1" and "0" well





Multiplexer

- **Two-input MUX using only switches**



A	B	S	$\overline{S}$	Z	
X	0	0	1	0	B
X	1	0	1	1	
0	X	1	0	0	A
1	X	1	0	1	

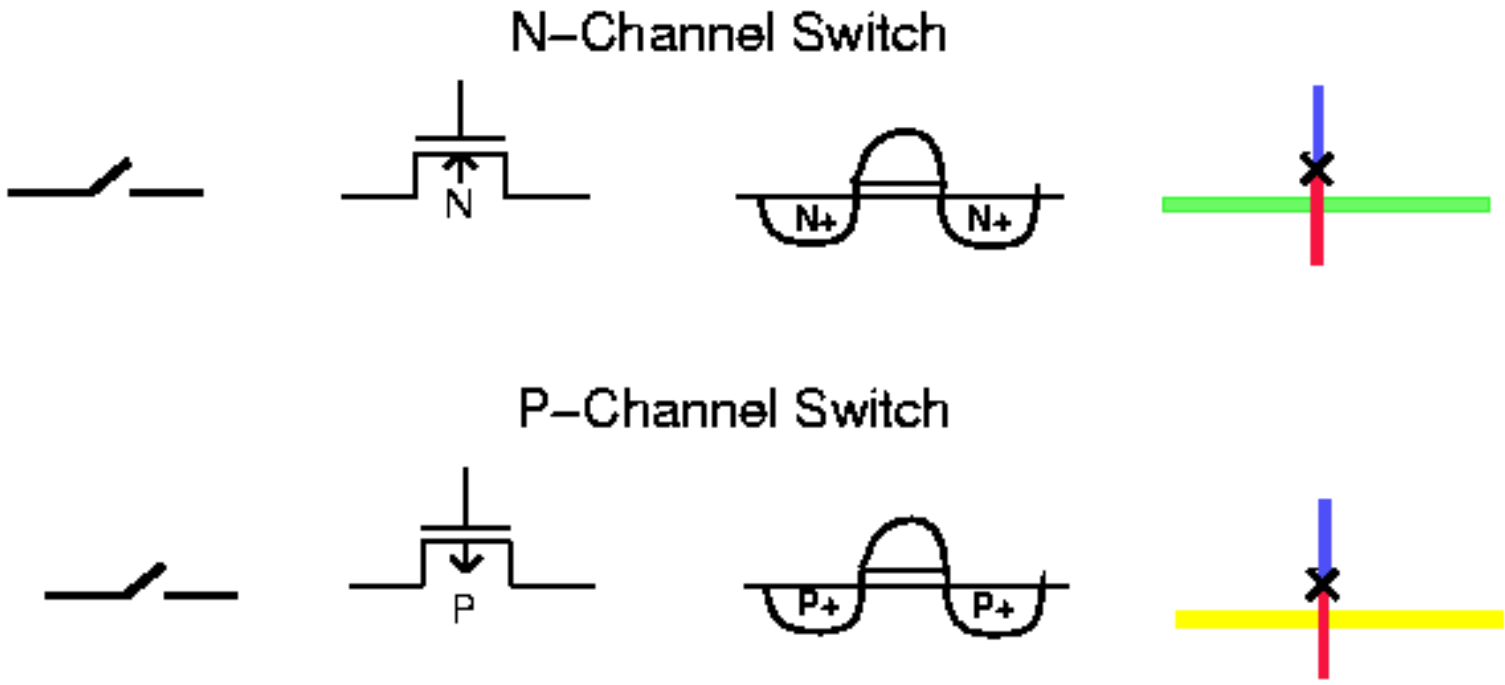
X: don't care

Schematic Vs. Physical Layout

- **In schematic layout, lines drawn between device terminals represent connections**
  - Any non-planar situation is dealt with by crossing lines
  - Provides more information than logic level (sizes of transistors, etc.)
- **Physical layout captures interaction between layers**
  - includes diffusion, polysilicon, metal (many layers of metal), vias (contacts)

Stick Diagram

- Intermediate representation between the schematic level and the mask level
- Gives topological information (identifies different layers and their relationship)
  - Assumes that wires have no width



Basic Layers in CMOS

When two layers of the same material (i.e., on the same layer) touch or cross, they are connected and belong to the same electrical node

When Polysilicon crosses Diffusion (N or P), an N or P transistor is formed

There is no diffusion underneath the poly, but the diffusion must be drawn connecting the source and the drain

The self-aligned gate is automatically formed during fabrication

When a Metal line needs to be connected to a metal line on another layer, or to one of the other three conductors, a contact cut (via) is required