CONTACT INFORMATION

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RESEARCH INTERESTS

My research focus in computer architecture is on the critical aspects of locality, bandwidth, and parallelism, and on improving the cooperation between the hardware, compiler, and programmer. I believe that this direction is the key to enabling new levels of performance, efficiency, and code portability.

EDUCATION

Stanford University, Stanford, California, USA

Ph.D., Electrical Engineering, January 2007

M.S., Electrical Engineering, June 2002

Technion – Israel Institute of Technology, Technion City, Israel

B.Sc., *summa cum laude*, Electrical Engineering, December 1999
B.A., *summa cum laude*, Physics, December 1999

ACADEMIC ACTIVITIES

Invited Talks

- Mattan Erez, "Stream Processing: a New HW/SW Contract for High-Performance Efficient Computation", CScADS Workshop on Automatic Tuning, Snowbird, UT, July 11, 2007.
- Mattan Erez, "Stream Architectures – Programmability and Efficiency", International Symposium on System-on-Chip 2004, Tampere, Finland, November 17, 2004.

EXPERIENCE

The University of Texas at Austin, Austin, Texas, USA

Assistant Professor **2007 –**

Electrical and Computer Engineering Department.

- EE382V Principles of Computer Architecture: Parallelism and Locality, Fall 2007
- EE382V Computer Architecture: User System Interplay, Spring 2007

Stanford University, Stanford, California, USA

Instructor **2000 – 2002**

Co-taught graduate level courses at the Department of Electrical Engineering. Shared responsibility for course development, lectures, homework assignments, projects, and grading.

- EE482C Advanced Computer Organization: Stream Processor Architecture, Spring 2001/2002
- EE482A Advanced Computer Organization: Processor Architecture, Spring 1999/2000

Research Assistant **1999 - 2006**

I was the student leader of the Merrimac Streaming Supercomputer project at Stanford, which included over ten Ph.D. students working on architecture, compiler, and application development. I was also the overall coordinator of the Merrimac project under Professor William J. Dally. I was researching and designing hardware, software systems, and streaming programming models for Merrimac, which involves working with application developers from the Mechanical Engineering, Aeronautics & Astronautics, and Structural Biology departments at Stanford University and researchers at NASA Ames Research Center and Lawrence Livermore National Lab. I also worked on Stanford's SmartMemories project developing parallel applications and a hardware architecture simulator.

Intel Corporation, Haifa, Israel

Computer Architect **1997 - 1999**

As a member of the Israeli Processor Architecture Research team, I was involved with inventing, analyzing, and implementing new architectural and micro-architectural concepts for high performance processors. As part of my work, I participated in the development of a timing-based performance simulator. My work at Intel was concurrent to my studies at the Technion.

Israel Defense Force, Israel

Non-Commissioned Officer **1993 - 1996**

Israel Defense Force, non-commissioned officer at a technical research branch.

SELECTED PUBLICATIONS

1. Jayanth Gummaraju, Mattan Erez, Joel Coburn, Mendel Rosenblum, William J. Dally, "Architectural Support for the Stream Execution Model on General-Purpose Processors", *in the Proceedings of the 16th IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT'07)*, Brasov, Romania, September 15-19, 2007.
2. Mattan Erez, Jung Ho Ahn, Jayanth Gummaraju, Mendel Rosenblum, and William J. Dally, "Executing Irregular Scientific Applications on Stream Architectures", *in the Proceedings of the 21st ACM International Conference on Supercomputing (ICS'07)*, pp. 93–104, June 2007.
3. Jung Ho Ahn, William J. Dally, and Mattan Erez, "Tradeoff between Data-, Instruction-, and Thread-level Parallelism in Stream Processors", *in the Proceedings of the 21st ACM International Conference on Supercomputing (ICS'07)*, pp. 126–137, June 2007.
4. Kayvon Fatahalian, Timothy J. Knight, Mike Houston, Mattan Erez, Daniel Reiter Horn, Larkhoon Leem, Ji Young Park, Manman Ren, Alex Aiken, William J. Dally, Pat Hanrahan, "Programming the Memory Hierarchy", *in the proceedings of the 2006 International Conference for High Performance Computing, Networking, Storage, and Analysis (SC'06)*, Tampa, Florida, November 2006.
5. Jung Ho Ahn, Mattan Erez, William J. Dally, "The Design Space of Data-Parallel Memory Systems", *in the proceedings of the 2006 International Conference for High Performance Computing, Networking, Storage, and Analysis (SC'06)*, Tampa, Florida, November 2006. (*award paper*)
6. Ulrich Barnhoefer, Moon-Jung Kim, Mattan Erez, "A Low Power, Passively Cooled 2000cd/m2 Hybrid LED-LCD Display", *in the proceedings of the IEEE International Symposium on Consumer Electronics 2006*, St. Petersburg, Russia, June 2006. (*award paper*)

7. Mattan Erez, Nuwan Jayasena, Timothy J. Knight, William J. Dally, "Fault Tolerance Techniques for the Merrimac Streaming Supercomputer", *in the proceeding of the 2005 International Conference for High Performance Computing, Networking, Storage, and Analysis (SC'05)*, Seattle, Washington, November 2005. (*award finalist, 1 out of 4 chosen from over 40 eligible papers*)
8. Jung Ho Ahn, Mattan Erez, William J. Dally, "Scatter-Add in Data Parallel Architectures", *in the proceedings of the Eleventh International Symposium on High-Performance Computer Architecture (HPCA-11)*, San Francisco, California, February 2005.
9. Mattan Erez, Jung Ho Ahn, Ankit Garg, William J. Dally, Eric Darve, "Analysis and Performance Results of a Molecular Modeling Application on Merrimac", *in the proceeding of the 2004 International Conference for High Performance Computing, Networking, Storage, and Analysis (SC'04)*, Pittsburgh, Pennsylvania, November 2004. (*award paper, chosen from over 40 eligible papers*)
10. Nuwan Jayasena, Mattan Erez, Jung Ho Ahn, William J. Dally, "Stream Register Files with Indexed Access", *in the proceedings of the Tenth International Symposium on High-Performance Computer Architecture (HPCA-10)*, Madrid, Spain, February 2004.
11. William J. Dally, Patrick Hanrahan, Mattan Erez, Timothy J. Knight, Franois Labonte, Jung Ho Ahn, Nuwan Jayasena, Ujval J. Kapasi, Abhishek Das, Jayanth Gummaraju, Ian Buck, "Merrimac: Supercomputing with Streams", *in the proceeding of the 2003 International Conference for High Performance Computing, Networking, Storage, and Analysis (SC'03)*, Phoenix, Arizona, November 2003. (*award finalist, 1 out of 5 chosen from over 60 eligible papers*)
12. Mattan Erez, Brian Towles, and William J. Dally, "Spills, Fills, and Kills - An Architecture for Reducing Register-Memory Traffic", *Concurrent VLSI Architecture Technical Report (TR-23)*, Stanford, California, November 2000.
13. Stephan Jourdan, Lihu Rappoport, Yoav Almog, Mattan Erez, Adi Yoaz, Ronny Ronen, "eXtendedBlock Cache", *in the proceedings of the Sixth International Symposium on High-Performance Computer Architecture (HPCA-6)*, Toulouse, France, January 2000.
14. Adi Yoaz, Mattan Erez, Ronny Ronen, Stephan Jourdan, "Speculation Techniques for Improving Load Related Instruction Scheduling", *in the proceedings of the 26th International Symposium on Computer Architecture (ISCA-26)*, Atlanta, Georgia, May 1999.

ISSUED PATENTS

15. Adi Yoaz, Ronny Ronen, Lihu Rappoport, Mattan Erez, Stephan Jourdan, Robert Valentine, "Memory Cache Bank Prediction", *US Patent #6,880,063*, Issued April 12, 2005. (Intel)
16. Adi Yoaz, Gregory Pribush, Freddy Gabbay, Mattan Erez, Ronny Ronen, "Fast Branch Misprediction Recovery Method and System", *US Patent #6,757,816*, Issued June 29, 2004. (Intel)
17. Adi Yoaz, Mattan Erez, Ronny Ronen, "System and Method for Early Resolution of Low Confidence Branches and Safe Data Cache Accesses", *US Patent #6,697,932*, Issued February 24, 2004. (Intel)
18. Adi Yoaz, Ronny Ronen, Lihu Rappoport, Mattan Erez, Stephan Jourdan, Robert Valentine, "Cache Memory Bank Access Prediction", *US Patent #6,694,421*, Issued February 17, 2004. (Intel)

AWARDS AND NON-ACADEMIC ACTIVITIES

SC'06 best student paper award.

ISCE 2006 best paper award.

SC'05 best student paper finalist (1 of 4 chosen from over 40 eligible papers).

SC'04 best student paper award (over 40 eligible papers).

SC'03 best paper finalist (1 of 5 chosen from over 60 eligible papers).

*n*Vidia Fellowship, 2003 – 2004.

Stanford Israeli Student Organization Treasurer, 2000 – 2003.

Technion President's list, 1997 – 1999.

Achievement award from the Haifa Youth Symphony Orchestra, 1992.