Digital Logic Design (EE316)

Prof. Michael Orshansky, Fall 2019

Course: EE316; Unique #s: 16095, 16100, 16105, 16110
Lecture: M W 10:30am -12:00pm in UTC 4.110
Exam-1: 10/11/19 (Friday), 7-8.30pm, UTC 2.112A
Exam-2: 11/15/19 (Friday), 7-8.30pm, UTC 2.112A
Final Exam: To be Announced by UT Registrar
Lab: In EER 0.716

Unique Number	Day	Time
16095	Tu	100 to 200p
16100	Tu	200 to 300p
16105	Tu	300 to 400p
16110	Tu	400 to 500p

Instructor:
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Text:
Required: Online Textbook: Digital Design by F. Vahid, zyBooks.
Signup instructions: (1) Sign in or create an account at learn.zybooks.com; (2) Enter zyBook code: UTEXASEE316OrshanskyFall2019; (3) Subscribe

Recommended (on reserve in library):
Digital Design with RTL Design, VHDL, and Verilog by Frank Vahid, Wiley and Sons, 2010.

In addition, as we begin to work with the FPGA board (Basys3 from Digilent using the Xilinx Artix-7), you will need to be familiar with the Xilinx Tool: Vivado WebPACK Edition. This version does not require a software license and will work with the Artix-7 FPGA on the Basys3 board. See the Xilinx website for more information: http://www.xilinx.com/support/download.html

The boards can be borrowed (checked out) at the EER lab check out window.

Course Objectives:
The course offers a contemporary approach to digital design emphasizing the separation of design and optimization tasks and introducing design methods as currently practiced. The course introduces students to the widely used hardware description language *Verilog*. The course covers: Boolean algebra, combinational and sequential logic components and design processes, storage elements, timing and timing-related non-idealities (setup/hold constraints, hazards), finite state machines, datapath components (adders, multipliers), RTL design, optimization techniques for combinational and sequential circuits (2-level logic minimization, FSM state encoding, Mealy vs. Moore FSMs), datapath component tradeoffs (slow vs. fast adders).

The students will work with a modern configurable logic design platform (FPGA) and design tools (Xilinx Vivado) for logic simulation, synthesis, and FPGA configuration.

Prerequisites:
EE 306: Introduction to Computing OR CS 429: Computer Organization and Programming

Attendance:
You are **expected to attend** each and every lecture.

Lecture Schedule
Below is a tentative schedule of lectures. Midterm exam **tentative** dates are also listed.

Week			HW/Labs	Lecture Slides Set	zyBook Reading and activities
1	8/28	Course Overview, Binary Numbers, Boolean Algebra		Lec 1	
2	9/4	Boolean Algebra, Combinational Logic (Continued)		Lec 2	1.3-1.11, 1.14, **due 10:00am on 9/4**
3	9/9	Combinational Optimization: Boolean Minimization	Lab 1 due 9/11	Lec 3	2.1, 2.2, 2.3, 2.4, 2.5 **due 10:00am on 9/9**
	9/11	Common Combinational Components Verilog: Combinational Logic Design	HW1 due 9/13	Lec 4	2.8, 2.9, 7.1, 7.2, 7.3, 7.4 **due 10:00am on 9/11**
4	9/16	Common Combinational Components (Continued)			2.6, 2.7 **due 10:00am on 9/16**
	9/18	Basic Storage Elements	Lab 2 due 9/20	Lec 5	3.1, 3.2 **due 10:00am on 9/18**
5	9/23	Basic Storage Elements (Continued)			3.3, 3.4, 3.5, 3.6, 3.7 **due 10:00am on 9/23**
	9/25	Controller/Finite State Machines	HW 2 due 9/27	Lec 6	
6	9/30	Controller/Finite State Machines (Continued)		Lec 7	3.12 **due 10:00am on 9/30**

	10/2	FPGA Design Implementation	Lab 3 due 10/4	Lec 8	7.5 **due 10:00am on 10/2**
7	10/7	Datapath Components: Multifunction Registers		Lec 9	6.5 **due 10:00am on 10/2**
	10/9	Review			
	10/11	**Exam 1 at 7-8:30pm**			Location: UTC 2.112A
8	10/14	Verilog: Sequential Logic Design;		Lec 10	
	10/16	Datapath Components: Adders	HW 3 due 10/18	Lec 11	4.1, 4.2, 4.3 **due 10:00am on 10/16**
9	10/21	Datapath Components: Comparators, Subtractors, Multiplier		Lec 12	4.4, 4.5 **due 10:00am on 10/21**
	10/23	Datapath Components: Shifters, Counters, Timers	Lab 4 due 10/25	Lec 13	6.3, 6.5 **due 10:00am on 10/23**
10	10/28	Datapath Components: ALUs, Register Files		Lec 14	6.4, 6.6 **due 10:00am on 10/28**
	10/30	Introduction to RTL Design	HW 4 due 11/1	Lec 15	5.1-5.4 **due 10:00am on 10/30**
11	11/4	RTL Design (cont)		Lec 15	5.5-5.8 **due 10:00am on 11/4**
	11/6	Timing and non-idealities (metastability, setup/hold constraints, hazards)	Lab 5 due 11/8	Lec 16	3.13 **due 10:00am on 11/6**
12	11/11	Advanced Logic Optimization		Lec 17	2.10, 2.11, 2.12 **due 10:00am on 11/11**
	11/13	Review			
	11/15	**Exam 2 at 7-8:30pm**			Location: UTC 2.112A
13	11/18	Advanced FSM Optimization: Mealy/Moore, State Reduction		Lec 18	3.9, 3.10, 3.11, 3.12 **due 10:00am on 11/18**
	11/20	Advanced FSM Optimization: Sate Encodings	Lab 6 due 11/22		
14	11/25	Advanced FSM Optimization: Design with T, JK Flip-Flops			
	11/27	**Thanksgiving Holiday**			
15	12/2	Memory components		Lec 19	6.7, 6.8, 6.9 **due 10:00am on 12/2**
	12/4	Review	HW 5 due 12/6		
16	12/9	Review			

For-Credit Book Reading/Participation Activities

A number of reading and participation activities using our interactive book will be assigned. **You need to do all activities in each designated book section before 10:00am on the day of the lecture.** You will not be able to do these activities for credit after that time.

Homeworks:
A number of homework assignments will be assigned throughout the semester. You are expected to submit your homework online through Canvas by 11:59PM on the due date. No late submission will be graded.

Labs:
You are expected to sign up for one of the lab sessions associated with the class. The labs will be conducted in EER 0.716. Lab assignments are due by 11:59pm on the "Due by" date. **Submissions need to be made online through Canvas.** After submitting on Canvas, students still need to have the lab checked out by any TA during your lab time slot. If the wait is too long, students can come back and checkout anytime during the week after the lab is due. **Labs turned in late receive 5% penalty per day (up to a week, after which there is no credit) that it is late.** Labs need to be demoed to one of the TAs ("checked out") within a week after the due date, after which students will not receive any credit for the lab. Please put name and lab section on lab submissions.

Lab	Topic
1	Combinational logic and logic simulation with schematic entry
2	Logic simulation in Vivado and Verilog design entry
3	Programming Combinational Logic on the Basys3 FPGA Board
4	Sequential Logic Design
5	Calculator with Adders and Registers
6	Term Project – Custom Processor Design: Programmable Stopwatch/Timer

Grading Policy:

Reading/Participation Activities	5%
Homework Assignments	10%
Labs	25%
Exams (2)	30%
Final	30%

Class information on-line:
The on-line information for this course is available on the Canvas site: http://courses.utexas.edu. In order to use this site you need your EID. Some things that will be available on this site:

- All lecture slides
- Homework assignments for the semester.
- Lab documents.

We will also be using an online messaging/discussion system Piazza at piazza.com/utexas/fall2019/ee316

Web-based, password-protected class sites are associated with all academic courses taught at The University. Syllabi, handouts, assignments and other resources are types of information that will be available within these

sites. Site activities could include exchanging e-mail, engaging in class discussions and chats, and exchanging files. In addition, electronic class rosters will be a component of the sites. Students who do not want their names included in these electronic class rosters must restrict their directory information in the Office of the Registrar, Main Building, Room 1. For information on restricting directory information see: http://www.utexas.edu/student/registrar/ferpa/ferpa.qs.faculty.htm

Getting help: If you have a question please ask! Do not wait till the last minute. The instructor and teaching assistants are here to help you.

Drop Policy: The last day to drop this course without permission from the Dean is the 4th class day. After this day, drops are approved only in the case of health or personal problems. An engineering student should make an appointment with his/her departmental advisor to discuss adding or dropping any course if the change will alter the classes that were originally approved by the departmental advisor. If the add or drop requires the approval of the Dean, then the student will need to schedule an appointment with an Academic Advisor in the Office of Student Affairs, ECJ 2.200 (471-4321) to discuss the request.

Additional information can be found at: http://www.engr.utexas.edu/current/policies/pol_add-drop-wdraw.cfm

Academic Dishonesty: Cheating will **not** be tolerated and will be dealt with according to the policy established by the office of the Dean of Students.

Students with disability: The University of Texas at Austin provides, upon request, appropriate academic adjustments for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, or the College of Engineering Director of Students with Disabilities at 471-4321.