EE 360S - Digital Integrated Circuits
Spring 2011

Lecture: Tu Th 9:30-11am in ENS 115
Unique No.: 16755

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Course Objectives: The students will learn to (i) hand-analyze the electrical characteristics of logical gates, (ii) design digital combinational and memory circuits according to specifications using computer-aided design tools, and (iii) discuss the trade-offs involved in design of semiconductor integrated circuits and the evolution of technology.

Description: This course thoroughly covers the fundamentals in design and analysis of CMOS digital integrated circuits. Topics to be covered include the following:

- MOS devices: MOS transistor operation and SPICE models
- CMOS invertors: noise margins and robustness, dynamic performance
- CMOS logic: static CMOS, pass-transistor logic, dynamic logic
- Interconnect: capacitance, inductance, impact on timing
- Semiconductor memories: DRAM, SRAM, ROM
- Low power design: techniques for minimizing power in logic and memories
- Design robustness: impact of variability, manufacturability

Prerequisite: EE 438 and EE 339

Required Textbook:

- Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd Edition, Prentice Hall, ISBN: 0-13-090996-3, 2003.

Reference Textbooks:

- D.A. Hodges, H.G. Jackson, and R.A. Saleh, *Analysis and Design of Digital Integrated Circuits In Deep Submircon Technology*, McGraw Hill, ISBN 0-07-228365-3, 2003.
- S.M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design (3rd edition)*, McGraw Hill, ISBN 0-07-246053-9, 2003.

Grading: Will drop lowest Homework. You must turn in Lab #4 to receive a grade for the class.

25% Midterm
35% Final
40% Homework/Lab Assignments

Homework Policy: Homework and lab assignments can be turned in during class or slid under my office door ACES 5.442 (it is fine to turn it in early). There will be a 10% penalty for homework and labs that are turned in late up until a week after it is due. Solutions to the homework and lab assignments will be made available during class the week after it is

due. Homework and lab assignments will not be accepted after solutions are made available. To summarize, homework and lab assignments turned in during or before the class period when they are due will receive full credit. Homework and lab assignments turned in late during or before the start of class the week after it is due will be penalized 10%. Homework assignments turned in after the start of class on the week after it is due will receive NO CREDIT.

Course Web Page: http://courses.utexas.edu/
We will rely heavily on the course management system Black Board. It will be used for posting the homework assignments and course handouts, and for making the announcements. The students are required to regularly check the course site.

College Drop/Add Policy: An engineering student must have the Dean's approval to add or drop a course after the fourth class day of the semester.

Students with Disabilities: The University of Texas at Austin provides upon request appropriate academic accommodations for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4641 TTY.

Scholastic Dishonesty: Faculty in the ECE Department are committed to detecting and responding to all instances of scholastic dishonesty and will pursue cases of scholastic dishonesty in accordance with university policy. Scholastic dishonesty, in all its forms, is a blight on our entire academic community. Scholastic dishonesty includes, but is not limited to, cheating, plagiarism, collusion, falsifying academic records, or any act designed to give an unfair academic advantage to the student. Penalties for scholastic dishonesty are severe and can include, but are not limited to, a written reprimand, a zero on the assignment/exam, re-taking the exam in question, an F in the course, or expulsion from the University. Don't jeopardize your career by an act of scholastic dishonesty.

Tentative Schedule for Spring 2010 Semester

Week	Date	Lecture Topic	Reading
1	Tu., Jan 18	**Introduction** Design Metrics	1.1-1.3
	Thur., Jan 20	**Manufacturing Process**	2.1, 2.2, 2.5
2	Tu., Jan 25	**Devices - 1** Semiconductor Basics: PN-Junction, MOS Cap	3.1, 3.2, notes
	Thur., Jan. 27	**Devices - 2** MOS Transistor I-V Characteristics	3.3
3	Tu., Feb. 1	**Devices -3** MOS Transistor Capacitance	3.4, 3.5
	Thur., Feb. 3	**Devices - 4** Nanometer Scale MOS Transistor	Notes
4	Tu., Feb. 8	**CMOS Inverter 1** Static Behavior	5.2, 5.3
	Thur., Feb. 10	**CMOS Inverter 2** Dynamic Behavior	5.4
5	Tu., Feb. 15	**CMOS Inverter 3** Components of Energy and Power	5.5, 5.6
	Thur., Feb. 17	**Combinational Logic - 1** Static CMOS Logic, Ratioed Logic	6.2.1
6	Tu., Feb. 22	**Combinational Logic - 2** Pass-Transistor Logic, Transmission Gate Logic	6.2.2
	Th., Feb. 24	**Combinational Logic - 3** Dynamic Logic	6.2.3

7	Tu., Mar. 1	**Combinational Logic - 4** Power Consumption in CMOS Logic Performance Optimization	6.3
	Th., Mar. 3	**Sequential Circuits -1** Static Latches and Registers	7.2
8	Tu., Mar. 10	**Sequential Circuits -2** Dynamic Latches and Registers	7.3
	Th., Mar. 12	**Midterm Exam**	
	Mar. 14-19	*SPRING BREAK*	
9	Tu., Mar. 22	**Interconnect - 1** Capacitance Estimation, Inductance	4.1-4.4
	Thur., Mar. 24	**Interconnect – 2** Buffer Chains, Power Distribution	4.5, 9.2-9.5
10	Tu., Mar. 29	**Clock Distribution** Clock Skew, Jitter, PLL	10.3, 10.6
	Thur., Mar. 31	**Memory – 1** Organization / Architecture, ROM, EPROM,	12.1, 12.2.1, 12.2.2
11	Tu., Apr. 5	**Memory – 2** SRAM Design	12.2.3
	Thur., Apr. 7	**Memory – 3** DRAM Design	12.2.3
12	Tu., Apr. 12	**Memory – 4** Peripheral Circuitry	12.3
	Thur., Apr. 14	**Low Power Design – 1** Design Time Power Reduction	11.7.1
13	Tu., Apr. 19	**Low Power Design – 2** Runtime Power Management	11.7.2
	Thur., Apr. 21	**Low Power Design – 3** Standby Power Reduction	11.7.3
14	Tu., Apr. 26	**Low Power Design – 4** Power Reduction in Memories	12.5
	Thur., Apr. 28	**Design Robustness - 1** Device Variability and Impact on Yield	3.4, 3.5
15	Tu., May 3	**Design Robustness – 2** Reliability, Manufacturability	
	Thur., May 5	**Review for Final Exam**	
	TBD	**FINAL EXAM**	