

Veynu Narasiman

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Education:

The University of Texas at Austin

Degree (Current): **PhD, Electrical/Computer Engineering** (Computer Engineering Track)

Supervising Professor: **Yale N. Patt**

Expected Graduation Date: **May 2010**

GPA: **3.97/4.0** (A = 4.0, A- = 3.67, etc.)

Degree: **Master of Science, Electrical/Computer Engineering** (Computer Engineering Track)

Graduation Date: **May 2006**

GPA: **3.97/4.0** (A = 4.0, A- = 3.67, etc.)

Degree: **Bachelor of Science, Electrical/Computer Engineering Honors**

Graduation Date: **May 2004**

Engineering GPA: **4.0/4.0** (A = 4.0, B = 3.0, etc.)

Degree: **Bachelor of Arts, Plan II Honors** (Liberal Arts Honors Program)

Graduation Date: **May 2004**

GPA: **3.97/4.0** (A = 4.0, B = 3.0, etc.)

Related Courses (Graduate): Micro-architecture, Parallel Computer Architecture, VLSI II, VLSI I, VLSI Communication Systems, High Speed Computer Arithmetic, Compilers, Distributed Computing, Computer Performance Evaluation and Benchmarking, Engineering Programming Languages

Related Courses (Undergraduate): Computer Architecture, Operating Systems, Embedded and Real-Time Systems Lab, Micro-controllers, Data Structures and Algorithms, Antennas and Wireless Propagation, Microwave/RF Engineering, Solid-State Electronic Devices, Modern Physics for Engineers, Special Topics in Modern Physics

Work Experience:

- **Summer 2007/2008: Intern, GPU Architecture Group, NVIDIA** – Santa Clara, CA
Tested both the correctness and performance impacts of conditional branches on NVIDIA's next generation Streaming Multiprocessor. Also augmented the architecture simulators used by the GPU architecture group. Further details of work are subject to privacy clauses.
- **Summer 2005/2006: Intern, Architecture & Verification Group, PA SEMI** – Santa Clara, CA
Worked for a start-up semiconductor company designing a low-power, high-performance microprocessor for the PowerPC Instruction Set Architecture. Details of work are subject to privacy clauses.
- **Summer 2004: Hardware/Software Engineering Intern, Schlumberger** – Houston, TX
Developed new simulation software used to test electronic measurement tools. Primary responsibility involved improving the low-level communication between a host computer and embedded measurement devices. Programming was done in C++ for the host computer and in C for the embedded devices.
- **Summer 2003: Hardware Engineering Intern, National Instruments** – Austin, TX
Developed a highly automated testing system for the PXI controllers manufactured at National Instruments. Wrote TCP/IP socket programs in both C as well as LabVIEW in order to remotely run tests on the PXI controllers from a host computer. Worked with both TestStand 2.0 and Ultimate II test software extensively.
- **Summer 2000: Information Technology Intern, Supplierone.com** – Houston, TX
Oversaw transfer of data from Microsoft Access 2000 to Microsoft SQL Server. Also wrote programs/scripts involving string parsing, searching, and sorting in Visual Basic, C++, and Python.

Academic Experience:

- **Fall 2006: Teaching Assistant, Introduction to Computing – The University of Texas at Austin**
Head TA for freshman level computer engineering course taught by Professor Yale N. Patt. Primary responsibilities included teaching weekly discussion sections, maintaining course webpage, creating homework/programming assignments, writing scripts to grade programming assignments, and creating/grading exam questions.

- **Fall 2005: Teaching Assistant, Computer Architecture – The University of Texas at Austin**
TA for junior/senior level course in computer architecture taught by Professor Yale N. Patt. Primary responsibilities included teaching weekly discussion sections, creating/grading homework problems, programming assignments, and exam questions.
- **Fall 2004: Teaching Assistant, Introduction to Computing – The University of Texas at Austin**
TA for freshman level computer engineering course taught by Professor Yale N. Patt. Primary responsibilities included teaching weekly discussion sections, creating/grading homework problems, programming assignments, and exam questions.

Skills:

- Knowledge of x86, PowerPC, and Motorola 6812 Instruction Set Architectures
- Proficient in Verilog, VHDL, C/C++, Java, LabVIEW, Perl, and HTML
- Experienced with CAD/EDA tools from Cadence, Synopsis, and Novas

Notable Awards/Distinctions:

- NVIDIA Fellowship (2007 – 2008)
- Cockrell Fellowship (2004 – 2008)
- Microelectronics and Computer Development Fellowship (2004 – 2006)
- Cockrell Scholarship (2000 – 2004)
- National Merit Scholarship (2000 – 2004)

Projects:

- **Microprocessor Design** - Micro-architecture Class Project, Spring 2006
Completed the architectural design and gate level implementation of a 7-stage, in-order pipelined processor for a subset of the x86 ISA. The processor ran at 100 MHz, featured 2-way set associative instruction and data caches, supported precise exceptions/interrupts, and communicated with 2 I/O devices and memory over an external bus. The entire processor design was implemented in Structural Verilog using a CMOS based standard cell library.
- **Cache Coherency** - Parallel Computer Architecture Class Project, Fall 2005
Performed a comprehensive comparison of several existing cache coherency protocols including the MSI, Goodman, MESI, and MOESI protocols. Extended the MOESI protocol by adding new states with the intent of improving load balancing and reducing coherency related bus operations.
- **Microprocessor Implementation** - VLSI II Class Project, Spring 2005
Was the lead implementer for the Exceptions Unit in a class wide processor design project. Behavioral Verilog code was provided; I produced the gate level implementation while meeting strict area, power, and timing requirements.
- **Viterbi Decoder** - VLSI I/VLSI Communication Systems Class Project, Fall 2004
Completed the design and implementation of a low power Convolutional Encoder and Viterbi Decoder. Simulations and high level programming was done using Matlab. Hardware implementation was done in Behavioral Verilog.
- **Compiler Optimization** - Compilers Class Project, Fall 2004
Implemented a compiler optimization aimed at increasing the ILP (Instruction Level Parallelism) within programs by removing unnecessary loop carried dependencies. Used IBM's Jikes RVM Java Compiler for the project.
- **MIMO-OFDM Wireless Communication System** - Honors Senior Design Project, Spring 2004
Prototyped a Multiple Input Multiple Output OFDM wireless communication system. Simulations were done using LabVIEW, and hardware implementation was done using receivers/transmitters from National Instruments.

Employability Status: US Citizen

References: Will be furnished upon request.