Department of Electrical and Computer Engineering
The University of Texas at Austin

EE 379K, Fall, 2000
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Exam 1, October 4, 2000

Name (2 points):_____

Problem 1 (18 points):_____

Problem 2 (15 points):_____

Problem 3 (10 points):_____

Problem 4 (15 points):_____

Problem 5 (15 points):_____

Problem 6 (15 points):_____

Problem 7 (10 points):_____

Total (100 points):_____

Note: Please be sure that your answers to all questions (and all supporting work that is required) are contained in the space provided.

Note: Please be sure your name is recorded on each sheet of the exam.

GOOD LUCK!

Name:_____

Problem 1 (18 points):

Part I (6 points): A memory's addressibility is 64 bits. What does that tell you about the size of the MAR and MDR?
About the size of the MAR:

About the size of the MDR:

Part II (6 points): You wish to express –64 as a 2's complement number.
How many bits do you need (the minimum number):

With this number of bits, what is the largest positive number you can represent (please give answer in both decimal and binary):

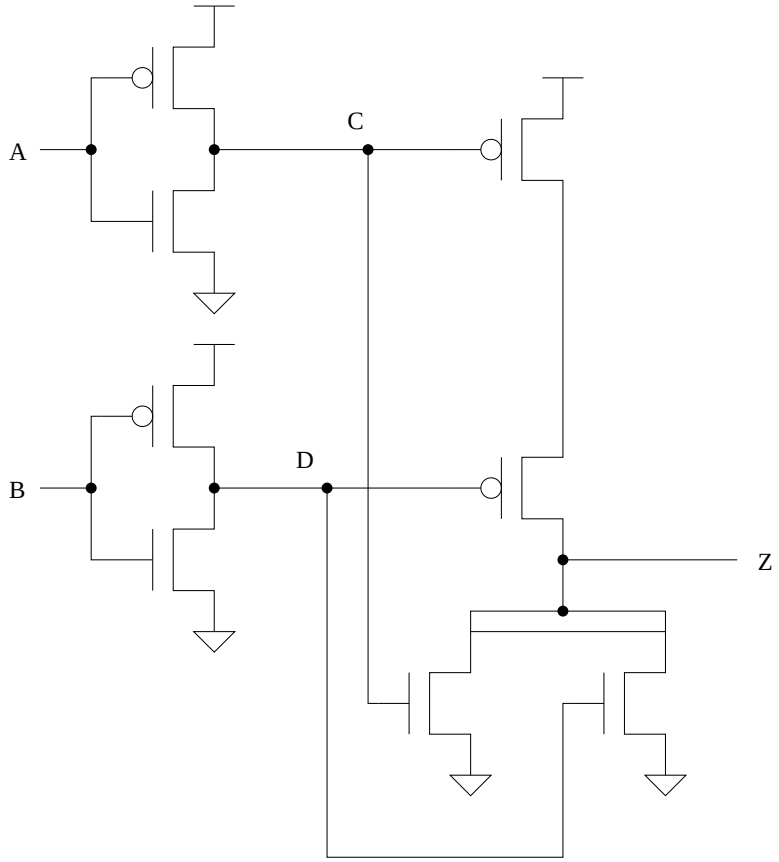
With this number of bits, what is the largest unsigned number you can represent (please give answer in both decimal and binary):

Part III (6 points): We want to increase the number of registers that we can specify in the LC-2 ADD instruction to 32. Do you see any problem with that? Explain.

Name:_____

Problem 2 (15 points):

For the following transistor circuit, fill in the truth table.



A	B	C	D	Z

What is Z in terms of A and B?

Name:_____

Problem 3 (10 points):

During which phases of the instruction cycle is the PC sometimes changed? the IR? the MAR? the MDR? For each table below, if the register specified by the row can be changed during the phase of the instruction cycle specified by the column, put a checkmark in the corresponding entry.

For the instruction whose opcode is 0001 (ADD):

	Fetch Instruction	Decode	Evaluate Address	Fetch Data	Execute	Store Result
PC						
IR						
MAR						
MDR						

For the instruction whose opcode is 0010 (LD):

	Fetch Instruction	Decode	Evaluate Address	Fetch Data	Execute	Store Result
PC						
IR						
MAR						
MDR						

For the instruction whose opcode is 0011 (ST):

	Fetch Instruction	Decode	Evaluate Address	Fetch Data	Execute	Store Result
PC						
IR						
MAR						
MDR						

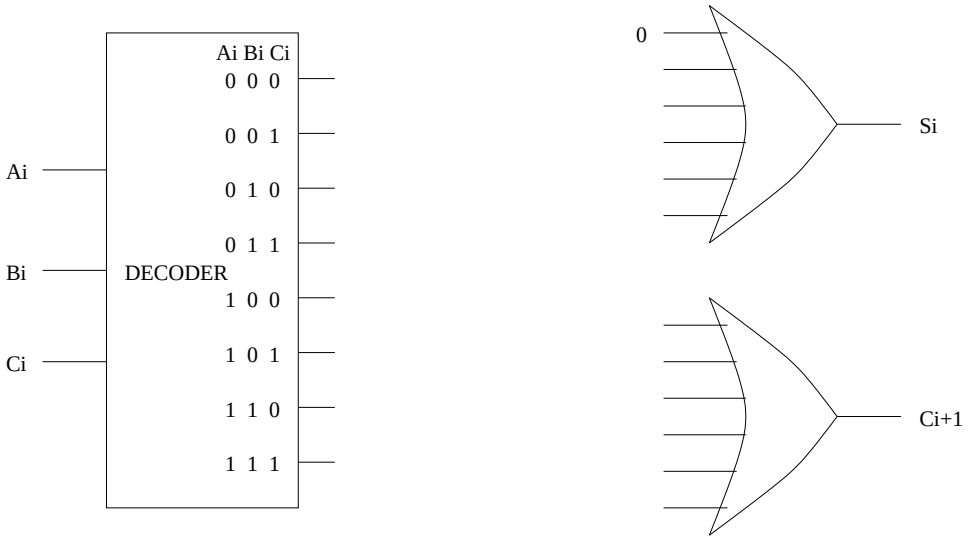
For the instruction whose opcode is 0000 (a control instruction):

	Fetch Instruction	Decode	Evaluate Address	Fetch Data	Execute	Store Result
PC						
IR						
MAR						
MDR						

Name:_____

Problem 4 (15 points):

Recall that the ADDER was built with individual ***slices*** that produced a Sum bit and Carry_out bit based on the two operand bits A and B and the Carry_in bit. We called such an element a Full Adder. Suppose we have a 3-to-8 Decoder and two six input OR gates, as shown. Can we connect them so that we have a Full Adder? If so, please do. [Hint: if an input to an OR gate is not needed, we can simply put a input 0 on it and it will have no effect on anything. For example, see figure.]



Name:_____

Problem 5 (15 points):

The LC-2 does not have an opcode for the logical function OR. That is, there is no instruction in the LC-2 ISA that performs the OR operation. However, we can write a sequence of instructions to implement the OR operation. The four instruction sequence below performs the OR of the contents of register 1 and register 2 and puts the result in register 3. Fill in the two missing instructions so that the four instruction sequence will do the job. The LC-2 instruction set is provided on the page for your use.

(1): 1001 100 001 111111

(2): | | |

(3): 0101 110 100 000 101

(4): | | |

Name:_____

Problem 6 (15 points):

Define a new 8-bit floating point format with 1 sign bit, 4 bits of exponent, using an excess-7 code (that is, the bias is 7), and 3 bits of fraction. If xE5 is the bit pattern for a number in this 8-bit floating point format, what value does it have (express as a decimal number):

Name:_____

Problem 7 (10 points):

Shown below is our favorite memory, a 2^2 by 3 bit memory. We have labeled each of the 12 gated latches A, B, C, D, E, F, G, H, I, J, K, L and the lines D<2:0> M, N, P. We have also indicated the values on certain wires.

Part A: What are the values at M and N and P?

Part B: Suppose WE changes from 0 to 1 for a short period of time and then changes back to 0. Which of the values A, B, C, D, E, F, G, H, I, J, K, L are different from what they were in Part A? What are their new values?