

ece 382N  
Spring, 2000  
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Mary Brown, TA  
March 1, 2000

Name (4 points): \_\_\_\_\_

Problem 1 (12 points): \_\_\_\_\_

Problem 2 (12 points): \_\_\_\_\_

Problem 3 (12 points): \_\_\_\_\_

Problem 4 (12 points): \_\_\_\_\_

Problem 5 (12 points): \_\_\_\_\_

Problem 6 (12 points): \_\_\_\_\_

Problem 7 (12 points): \_\_\_\_\_

Problem 8 (12 points): \_\_\_\_\_

Problem 9 (12 points): \_\_\_\_\_

Problem 10 (12 points): \_\_\_\_\_

Total (100 points): \_\_\_\_\_

You may answer any 8 of the 10 questions. Place an "X" in the two lines above for the two problems that you choose to not answer.

Note: Please be sure that your answers to all questions (and all supporting work that is required) are contained in the space provided.

Note: Please be sure your name is recorded on each sheet of the exam.

GOOD LUCK!

Name: \_\_\_\_\_

Problem 1 (12 points):

Some elements are part of the ISA, others are part of the microarchitecture. For each of the following, identify whether it is part of the ISA or part of the microarchitecture. If it could be either, "depending," explain what it depends on. The three elements are: Return address stack, Delayed branch, Second-level cache.

Name: \_\_\_\_\_

Problem 2 (12 points):

The VAX ISA had an instruction, POLYH that, in one instruction, could evaluate an  $n$  degree polynomial, where the coefficients and the argument  $x$  were expressed in Digital's H floating point format: 128 bits per data element. A bright young microarchitect proposed to design a VAX implementation that could execute that instruction more than an order of magnitude faster than the closest competition. Should he be allowed to carry out the design? What fundamental design guideline has been violated, if any. Explain.

An eight-wide issue, out-of-order execution machine has a 256-entry reservation station, one heavily pipelined integer ALU, one heavily pipelined load/store unit, and a retirement unit that can commit eight instructions each cycle. The large number of reservation stations is designed in order to accommodate long latencies due to cache misses that require going off-chip for servicing. From what you have been told, what is the maximum IPC of this design? What fundamental design guideline has been violated, if any. Explain.

Name: \_\_\_\_\_

Problem 3 (12 points):

The compiler is at a disadvantage to the microarchitecture in that it must make all its decisions before the program starts execution and therefore can not benefit from run-time information. Sort, of -- since the compiler can profile the program on a sample data set, and if the data set is representative, the compiler can make some good guesses about what will happen at run time.

In spite of this handicap, the compiler can provide substantial performance improvement. List three things that the compiler can do that can translate to improved performance (0 points). For each, give a specific example to demonstrate the feature (12 points).

Name: \_\_\_\_\_

Problem 4 (12 points):

Newer ISAs have predicated instructions. For example, in addition to an ADD, an ISA can have a predicated-ADD. What benefit do these instructions provide? Show by means of an example. When should such instructions be used? When should such instructions not be used? Explain.

Name: \_\_\_\_\_

Problem 5 (12 points):

A superscalar processor can fetch/decode/issue  $n$  instructions/cycle. A VLIW processor can fetch/decode/issue  $n$  instructions/cycle. What are the advantages/disadvantages of each? Give two other examples of paradigms discussed in class that provide the benefits of both superscalar and VLIW. Explain. [Hint: One is an imminent commercial product. One is a research vehicle.]

Name: \_\_\_\_\_

Problem 6 (12 points):

SPARC is an example of an ISA that has condition codes. Some ISAs do not. What are the advantages/disadvantages of having condition codes or not? IBM's RS6000 provided a twist to condition codes that removed the major disadvantage of everyone else's condition codes. Explain.

IBM's twist on condition codes provided a bonus with respect to conditional branches. Explain.

Name: \_\_\_\_\_

Problem 7 (12 points):

IA-32 has a variable length, densely-encoded instruction; Power-PC has a fixed-length instruction. What is the major advantage of each?

How are these advantages influenced by expected future changes in microprocessor characteristics? For example, higher on-chip frequencies. For example, wider issue-widths.



Name: \_\_\_\_\_

Problem 8 (12 points):

The semantic gap diagram we discussed in class showed that there are (at least) two approaches to get to the control signals that drive the data path. John Cocke suggested exposing the microcode to the compiler. A densely-encoded ISA suggests having higher-level instructions that are implemented on-chip as sequences of successively executing microinstructions. Assume each microinstruction has the capability of performing several operations simultaneously during a microcycle. What is the major advantage of John Cocke's approach? How do the two approaches compare with respect to compiler complexity, bandwidth requirements, cache effectiveness, and concurrency opportunities in the design of the chip itself.

Name: \_\_\_\_\_

Problem 9 (12 points):

What is a load/store ISA? Give an example of an ISA that is load/store. Give an example of an ISA that is not load/store. What are the advantages of each? Are these advantages/disadvantages more or less important today than they were ten years ago? Explain.

Name: \_\_\_\_\_

Problem 10 (12 points):

In two or three years, we will have 400 Million transistors on a chip. You are in charge of product development at XYZ Corporation, and have the job of deciding what chip to build. Your options are a single superscalar processor that utilizes all 400 Million transistors, a SMT uniprocessor that utilizes all 400 Million transistors, or a 2, 4, or 8 processor chip that uses 200 Million, 100 Million, or 50 Million transistors per processor, respectively. Assume design time of the chip is not an issue.

List the major issues you would consider in determining what XYZ Corporation should build. For each issue, identify the tradeoffs.

Which product would you build? Explain. (No points for picking a product; all points for justifying your choice.)