Department of Electrical and Computer Engineering
The University of Texas at Austin

EE 382N, Spring 2004

Homework 3
Due: No Due Date
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Note: This assignment is for your own use in planning your term project. It does not have to be turned in. However, we strongly encourage you to start work on this early. Doing this assignment will aid you in catching problems before they become major hassles.

Part 1. Augment your Data Path to handle the following :

Prefixes: segment override (all), operand size.
Instructions: CMOVC, JNE, JNA, HLT, ROR, SAL, SAR, BSWAP, XCHG, NOP, PUSH, POP.
Addressing Modes: SIB byte.
Data Types: byte, word.

Show all control signals needed to control the new (ie. augmented) data path. (In homework set 4 we shall start specifying the logic needed to produce those control signals).

Part 2. Enter the additions of Part 1 above into your Verilog specification.

Part 3. To test your augmented specification, select five more instructions with appropriate addressing modes and prefixes. Calculate the number of cycles required to execute each of these five instructions. Your results will depend on your choices, of course. For purposes of this assignment, assume 10 nsec cycle time, single-cycle cache access, 100 nsec memory access time, data cache hit ratio of 0.80, instruction cache hit ratio of 0.95. and no page faults.