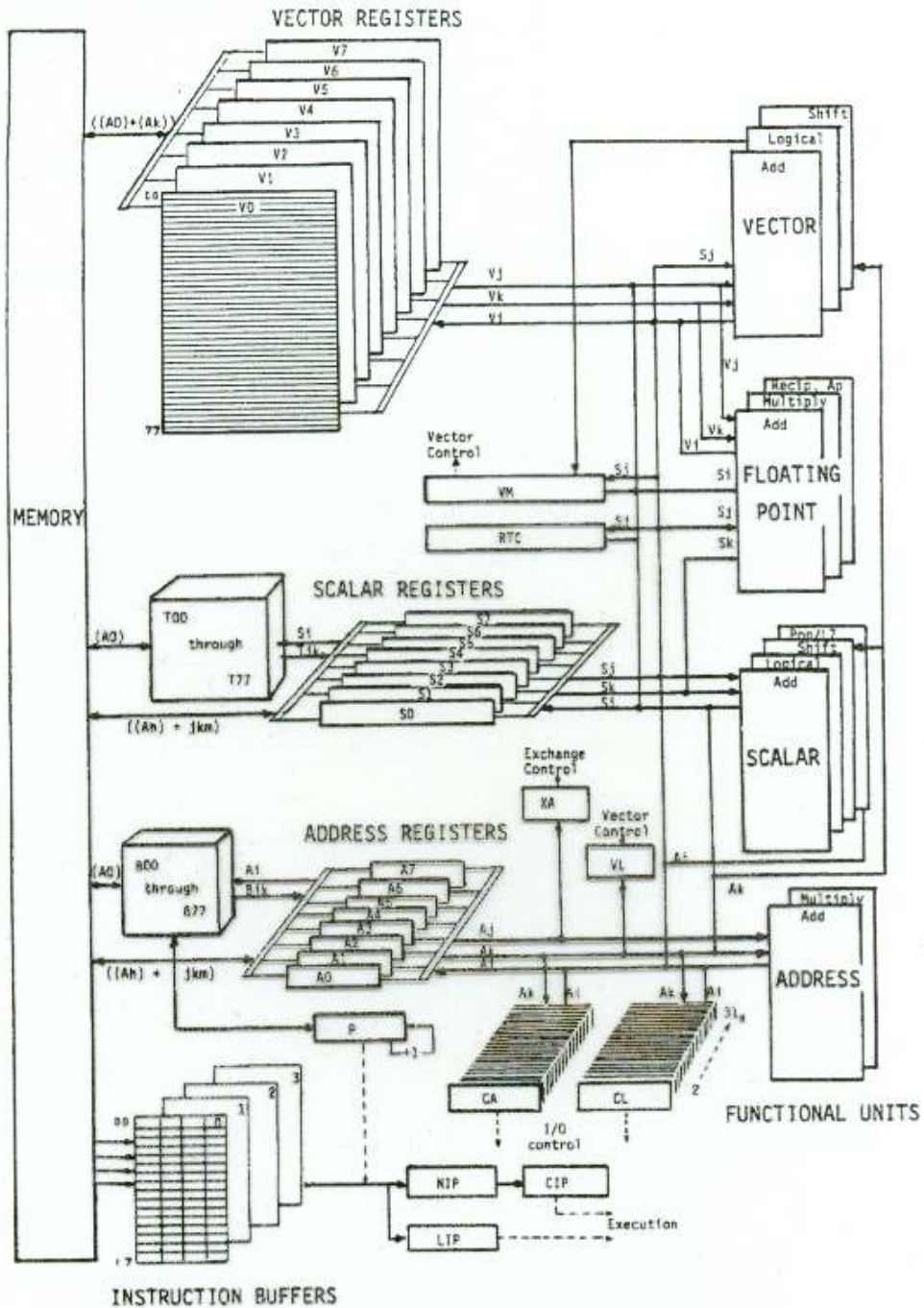


Outline

- * Vector Processing**
 - Without Vectors
 - With Vectors, Without Chaining
 - With Chaining
 - With Adequate Memory Ports

- * Scalar Processing**
 - Scoreboarding
 - Tomasulo (Renaming)

Fig. 5. Block diagram of registers.



Some Characteristics

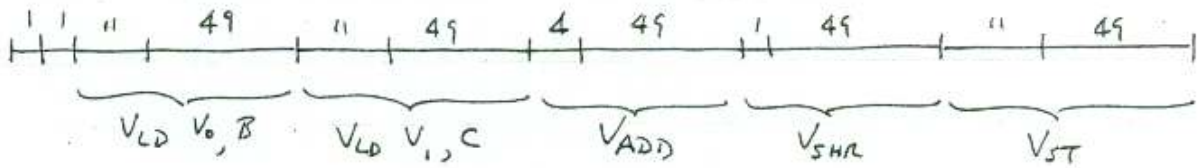
- * Heavy emphasis on timing, packaging**
- * No Cache**
- * Chaining**
- * Load/Store**
- * Single Cycle Issue**
- * Scoreboarding**
- * Instruction Buffer**
- * Back Up Registers**

Example: DO 10 I = 1, 50
 C(I) = (A(I) + B (I))/2
 10 Continue

* <u>Scalar</u>	<u>Cycles</u>
MOVI 50, R0	1
MOVA A, R1	1
MOVA B, R2	1
MOVA C, R3	1
X: LD R4, (R1) +	11
LD R5, (R2) +	11
ADD R4, R5, R6	4
SHR R6, R7	1
ST R7, (R3) +	11
DECBNZ RO, X	2
⋮	

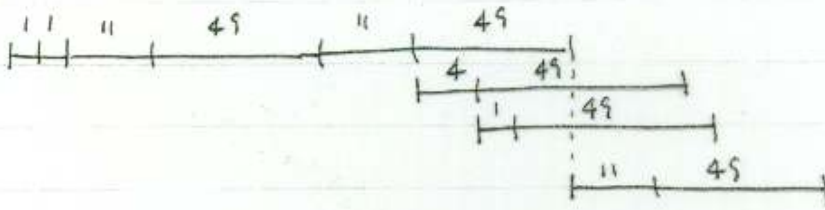
* <u>Vector</u>	
MOVI 50, VLN	1
MOVI 1, VST	1
VLD V ₀ , A	11 + n-1
VLD V ₁ , B	11 + n-1
VADD V ₀ , V ₁ , V ₂	4 + n-1
VHSR V ₂ , V ₃	1 + n-1
VST V ₃ , C	11 + n-1

VECTOR PROCESSING (PAGE 2)



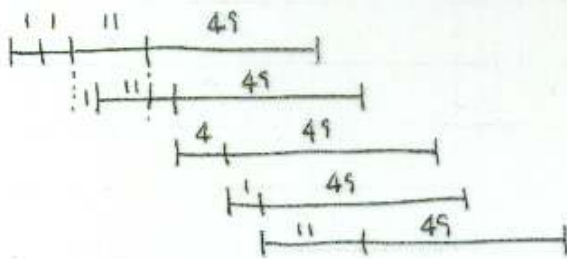
285 CYCLES

WITH CHAINING



182 CYCLES

WITH 2 LD, 1 STORE PORTS



79 CYCLES