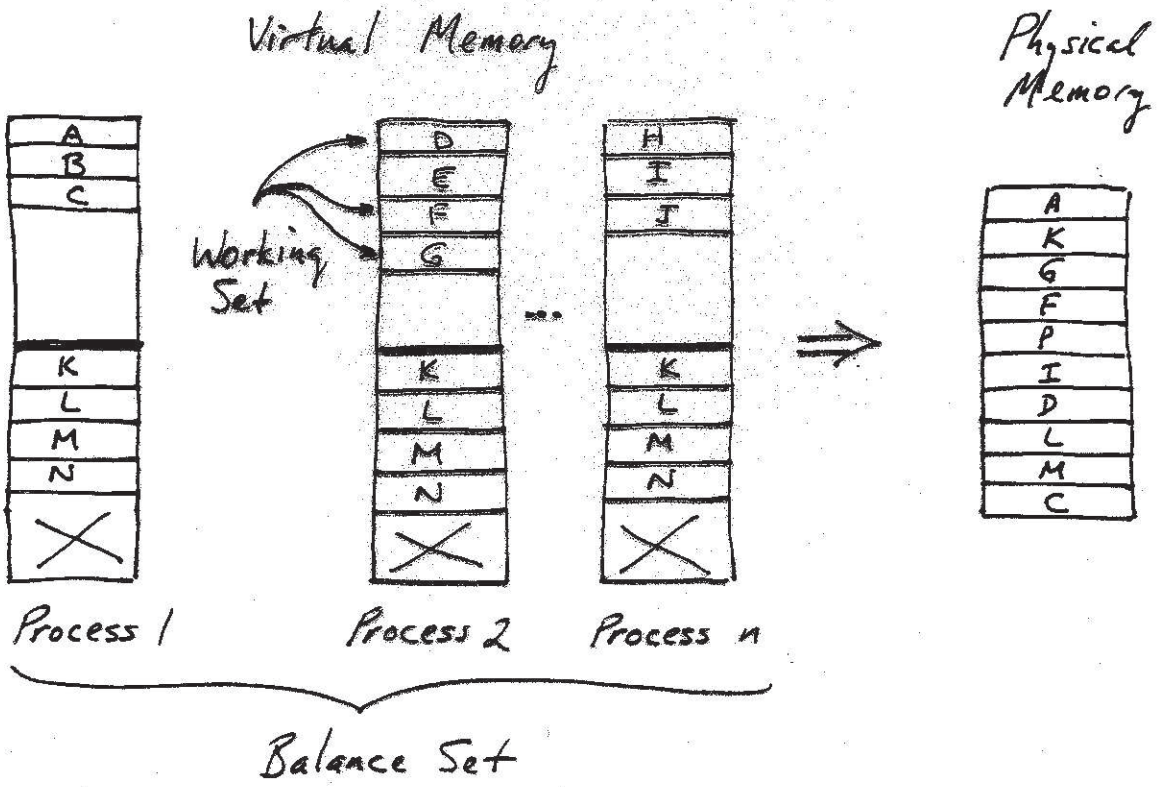
Virtual Memory

* ISA has large VA space.
  - Allows user to uniquely identify lots
* Physical Memory is smaller
  - Cost issue

* Virtual Memory Management
  - Access Control
  - Translation

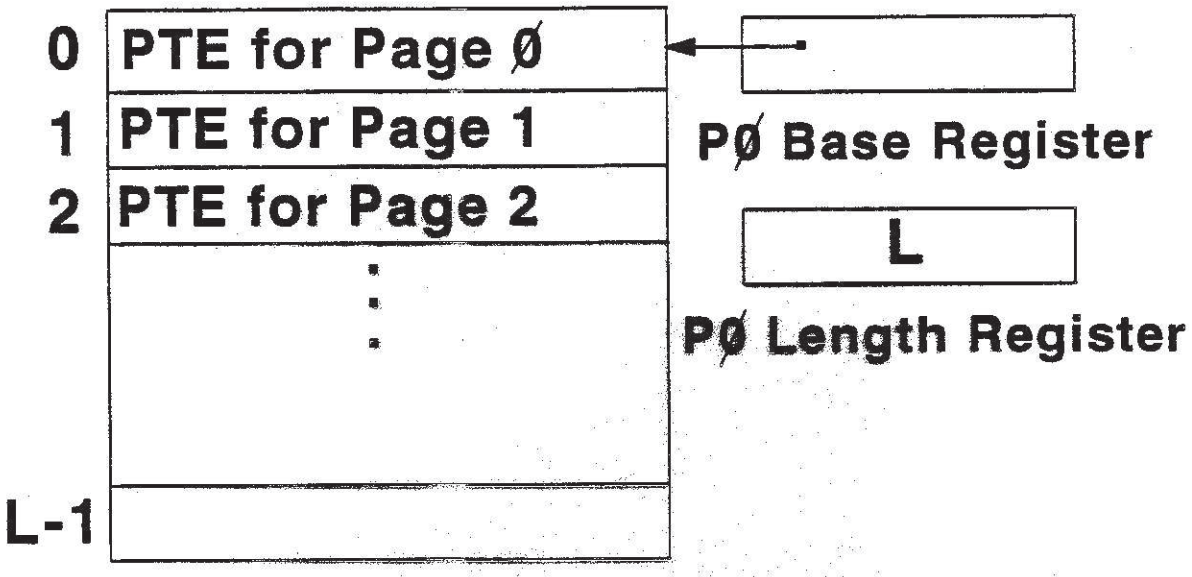
* The VAX Model



Page Tables

* One for each region

* For example, the P0 Page Table

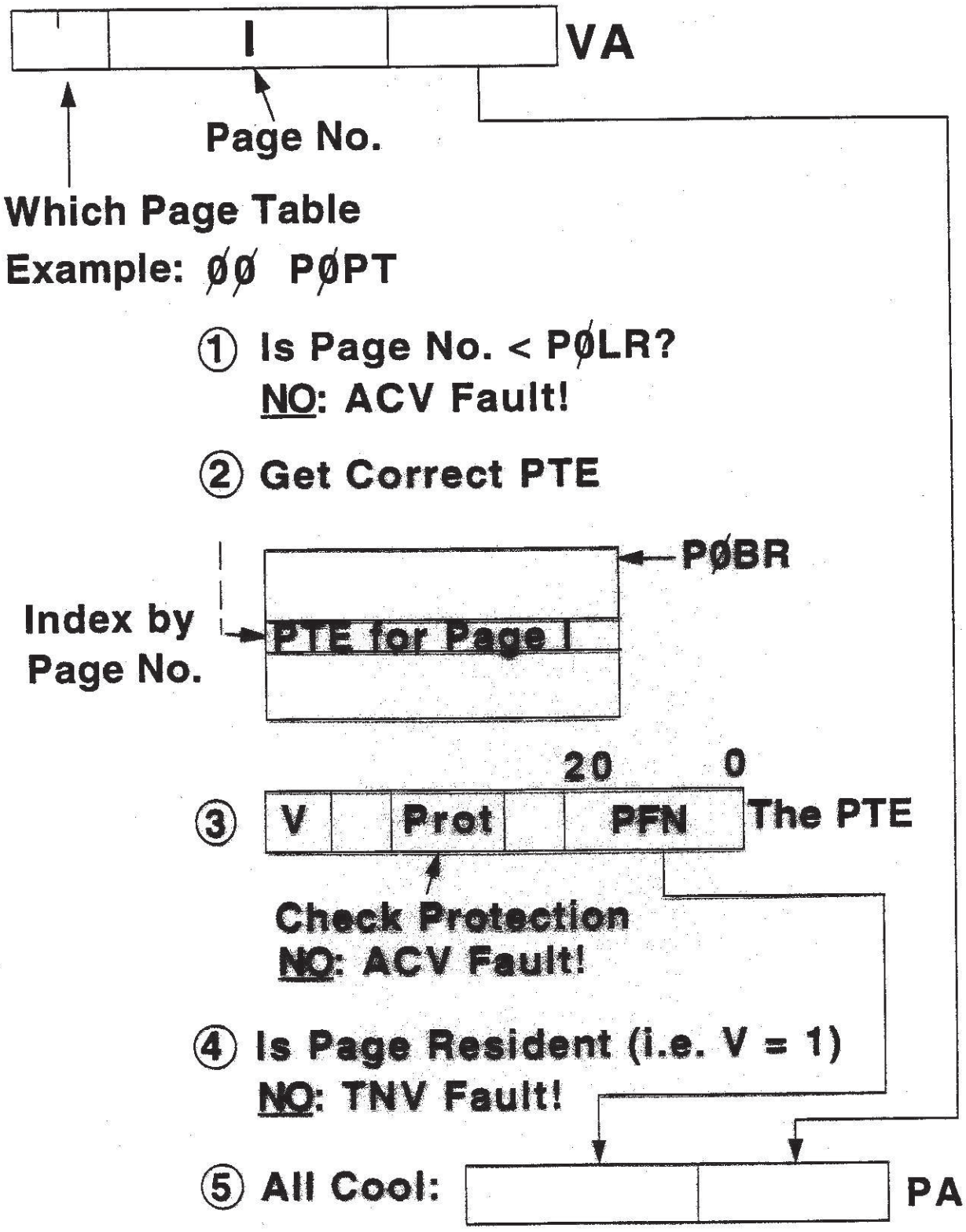


* Sequentially stored in System Virtual Space

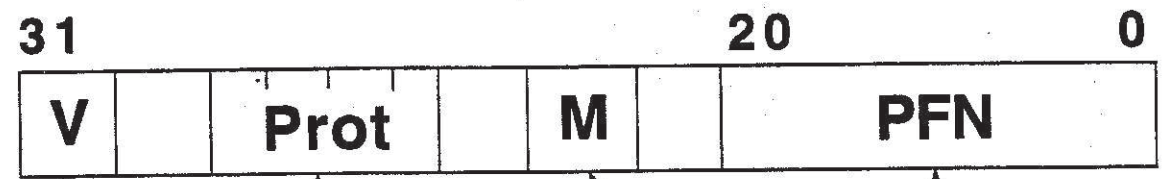
* P0LR used for ACV checks

* PTE used for ACV, TNV checks

The Abstraction



The PTE



Can I Believe The PFN

Has the Page Been Written

Do I have the Right to do this access

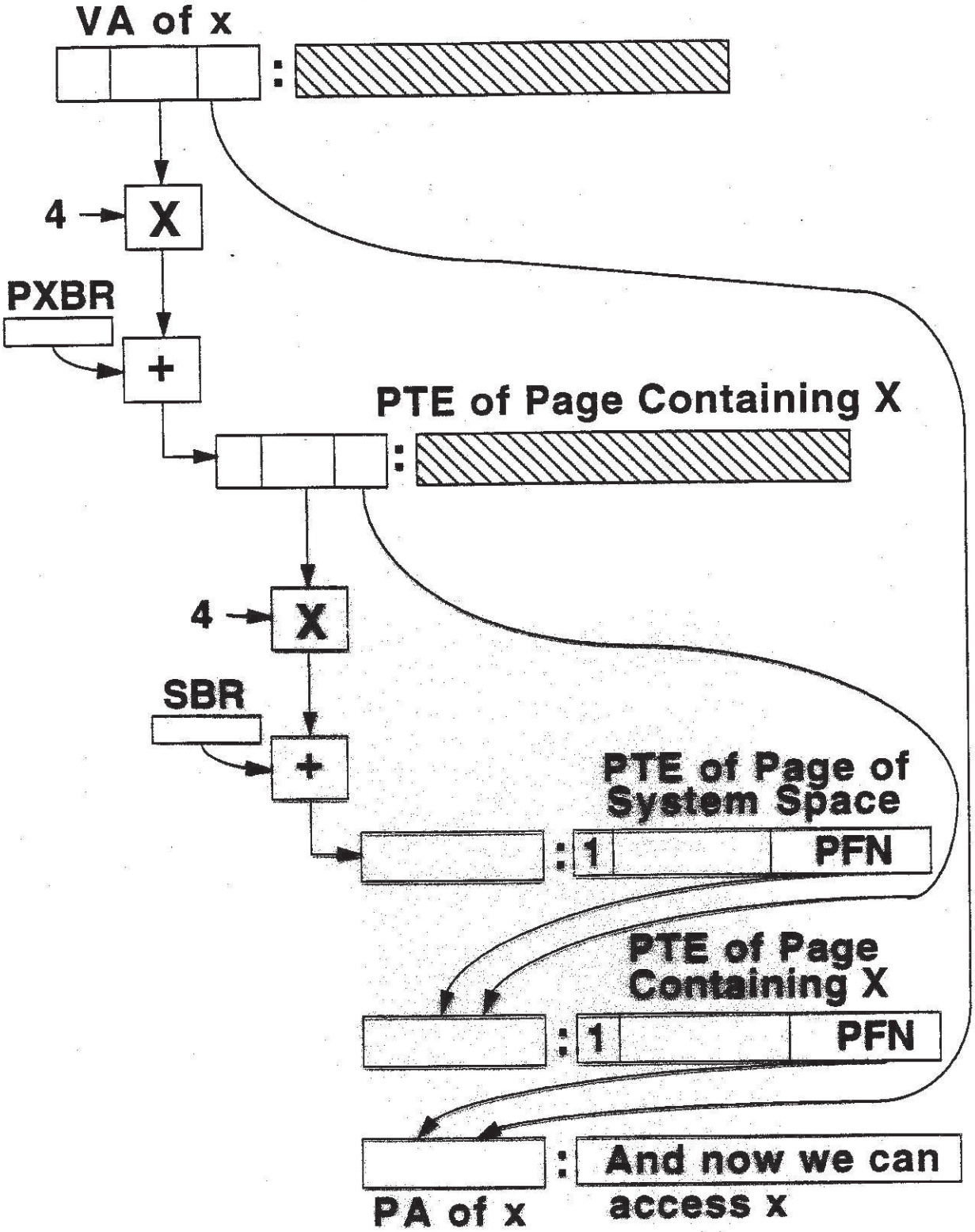
In which frame is the Page Stored

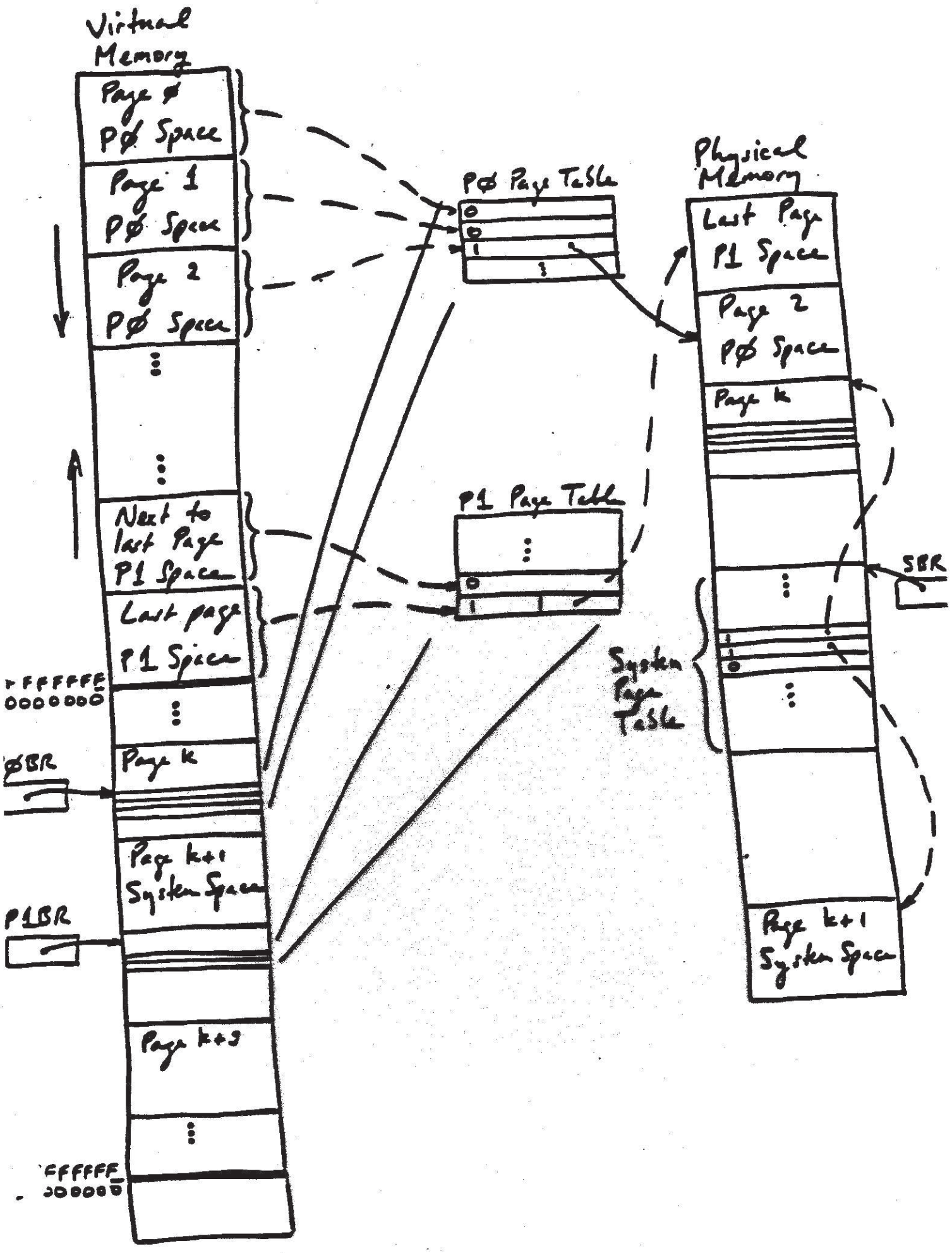
$\{NO,R,R/W\}^{\{K,E,S,U\}}$

81 Possibilities in 4 bits ?

Note:

No Ref. Bit!

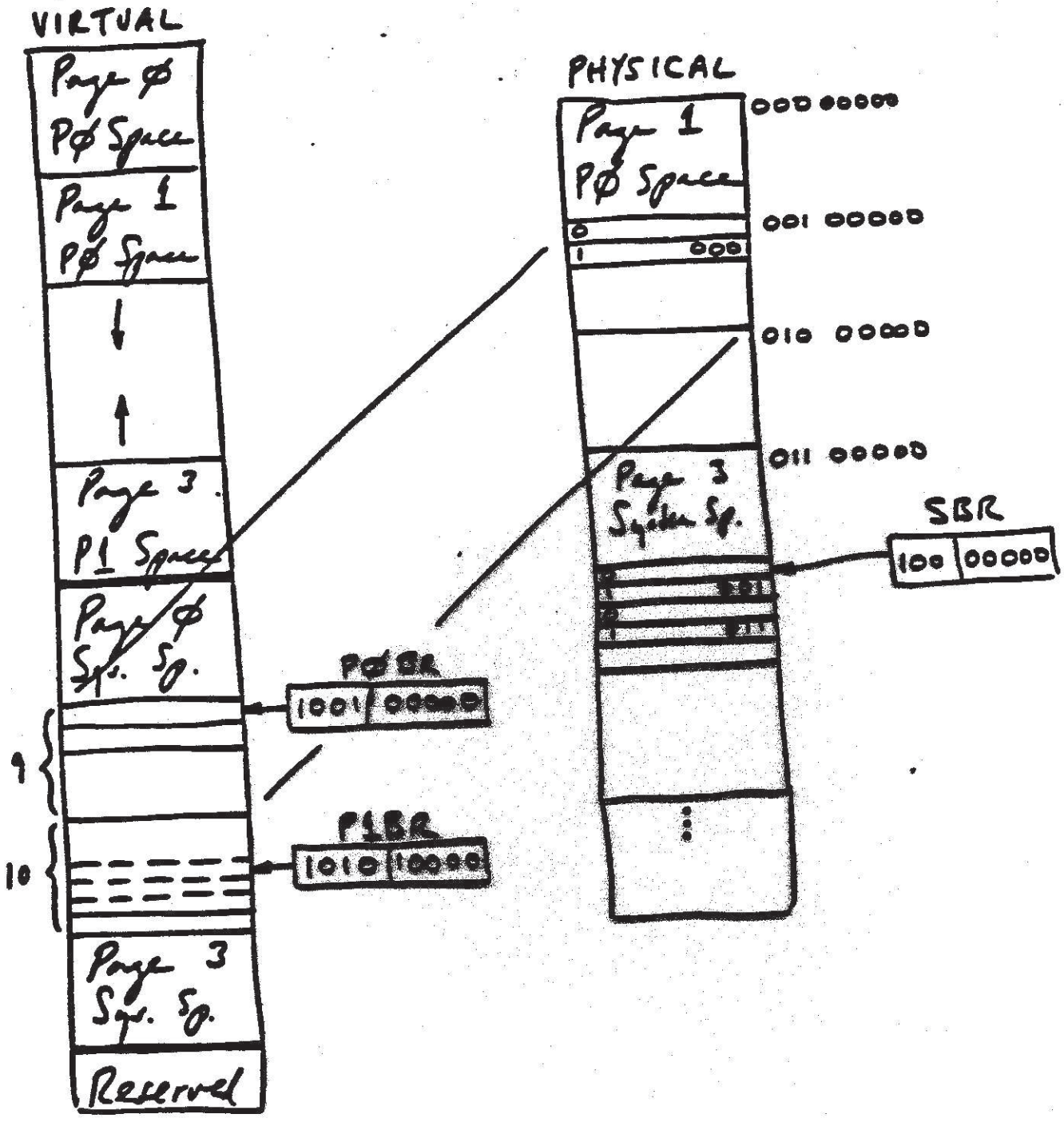

VA of x
4
X
PXBR
+
PTE of Page Containing X
4
X
SBR
+
PTE of Page of System Space
1
PFN
PTE of Page Containing X
1
PFN
And now we can access x
PA of x


Virtual Memory
Page 0 P0 Space
Page 1 P0 Space
Page 2 P0 Space
Next to last Page P1 Space
Last page P1 Space
Page k
Page k+1 System Space
Page k+3
P0BR
P1BR
P0 Page Table
P1 Page Table
Physical Memory
Last Page P1 Space
Page 2 P0 Space
Page k
Page k+1 System Space
SBR
System Page Table

VAX Hardware Memory Mgt.

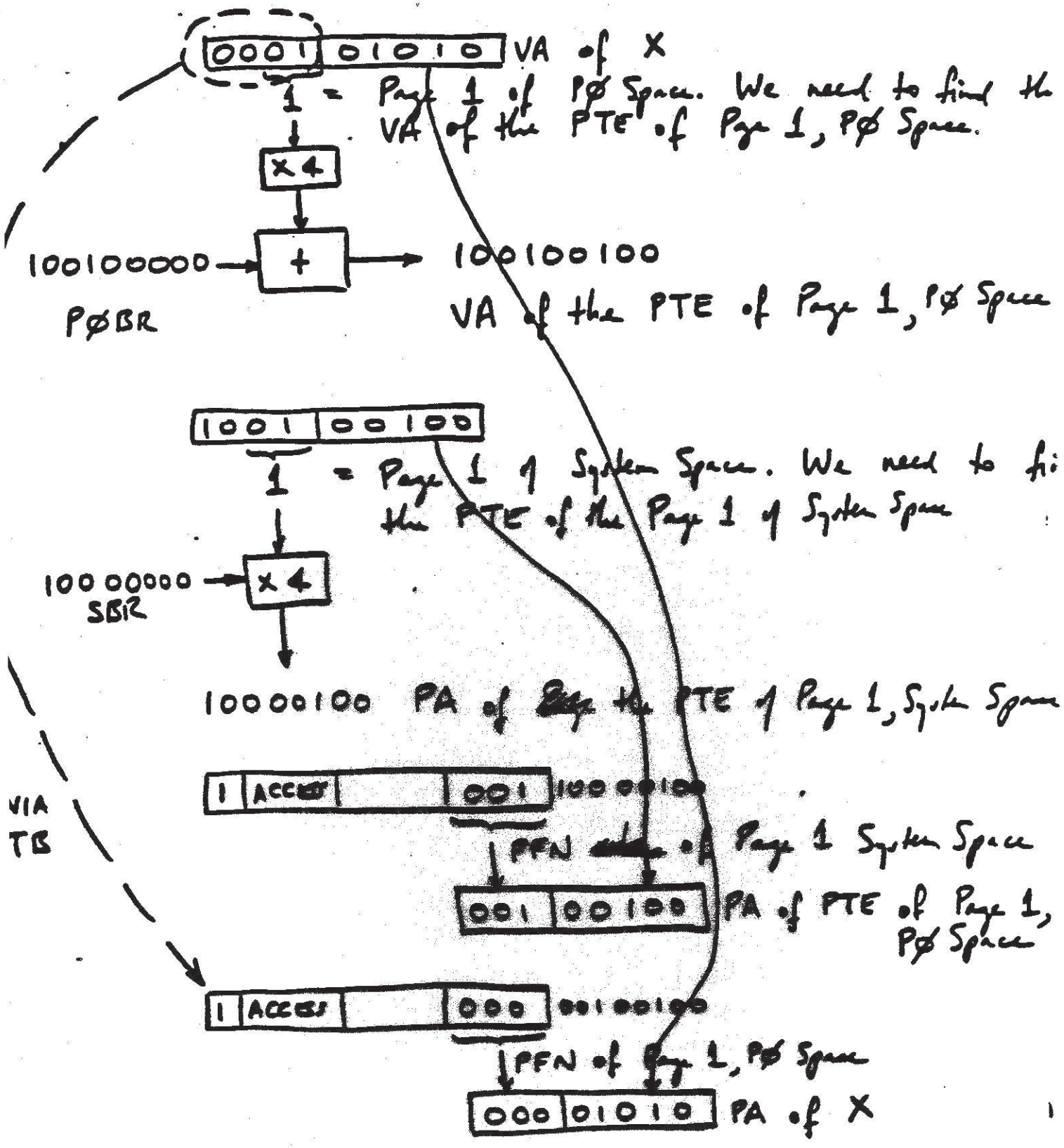
(Assuming 9 bit VA Space)

16 pages, 32 bytes each

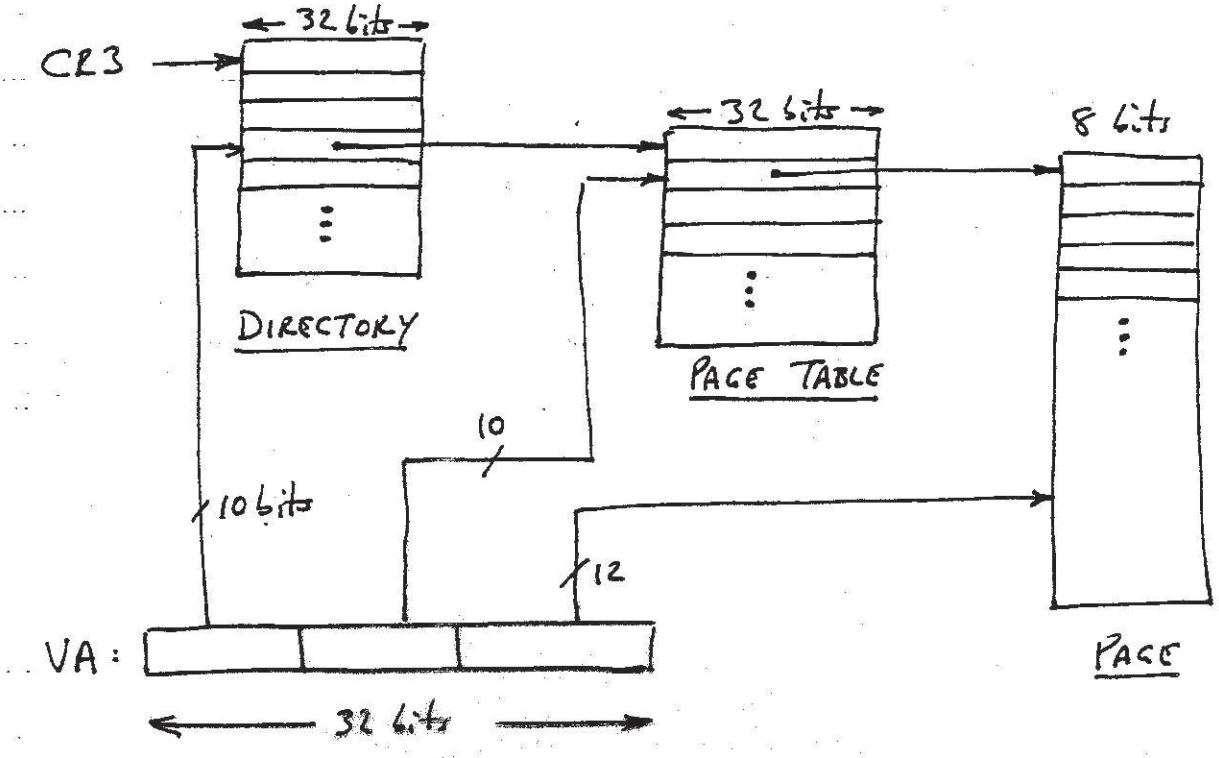


Example:

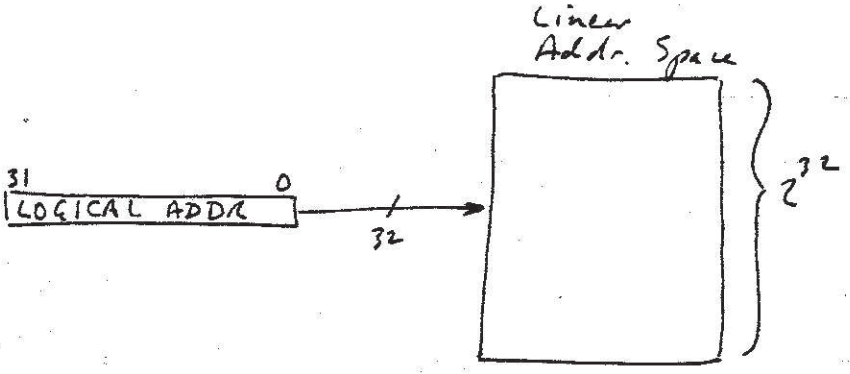
VA of a Byte X on Page 1, P0 Space



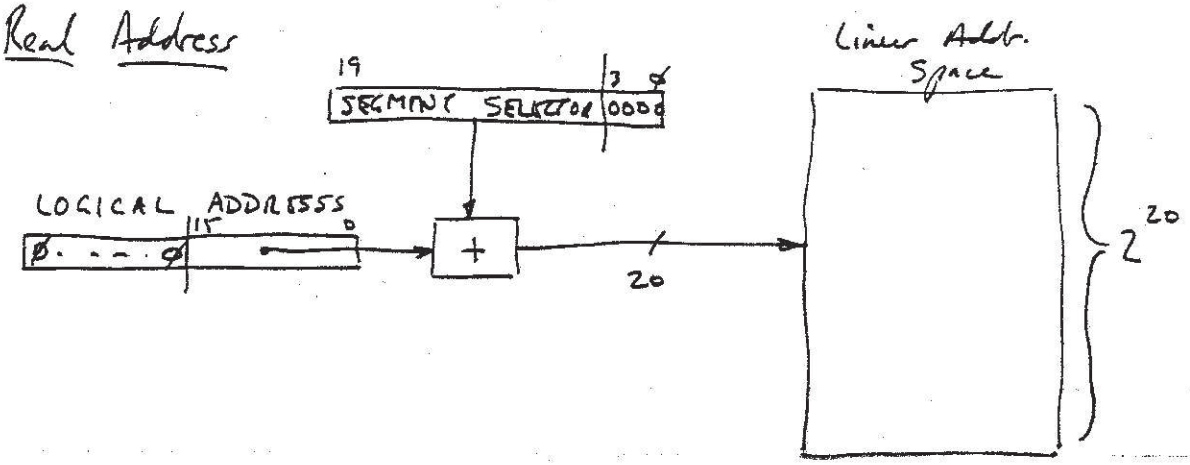
IA-32


32 bits
CR3
DIRECTORY
32 bits
PAGE TABLE
8 bits
PAGE
10
10 bits
12
VA:
32 bits

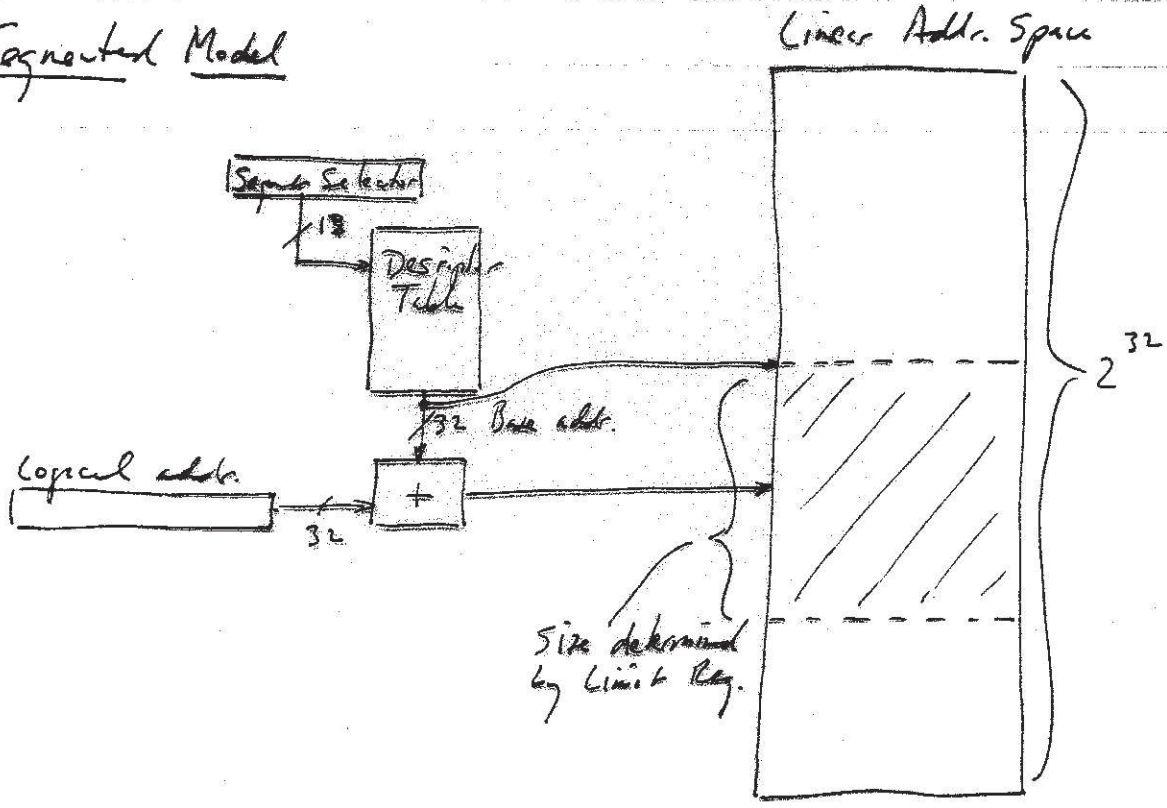
Flat Model



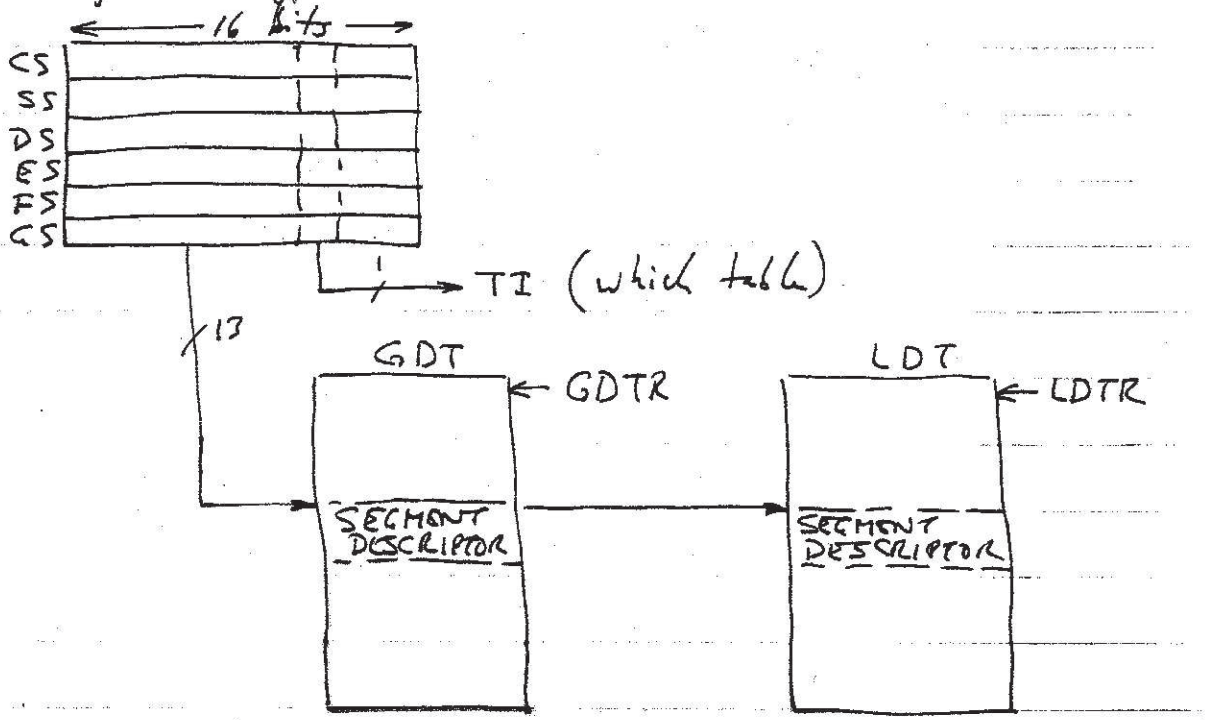
Real Address



Segmented Model

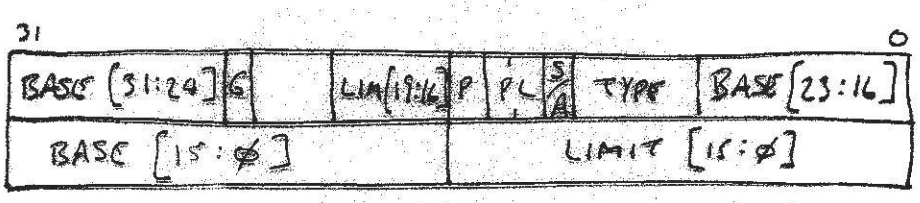


Segment Registers



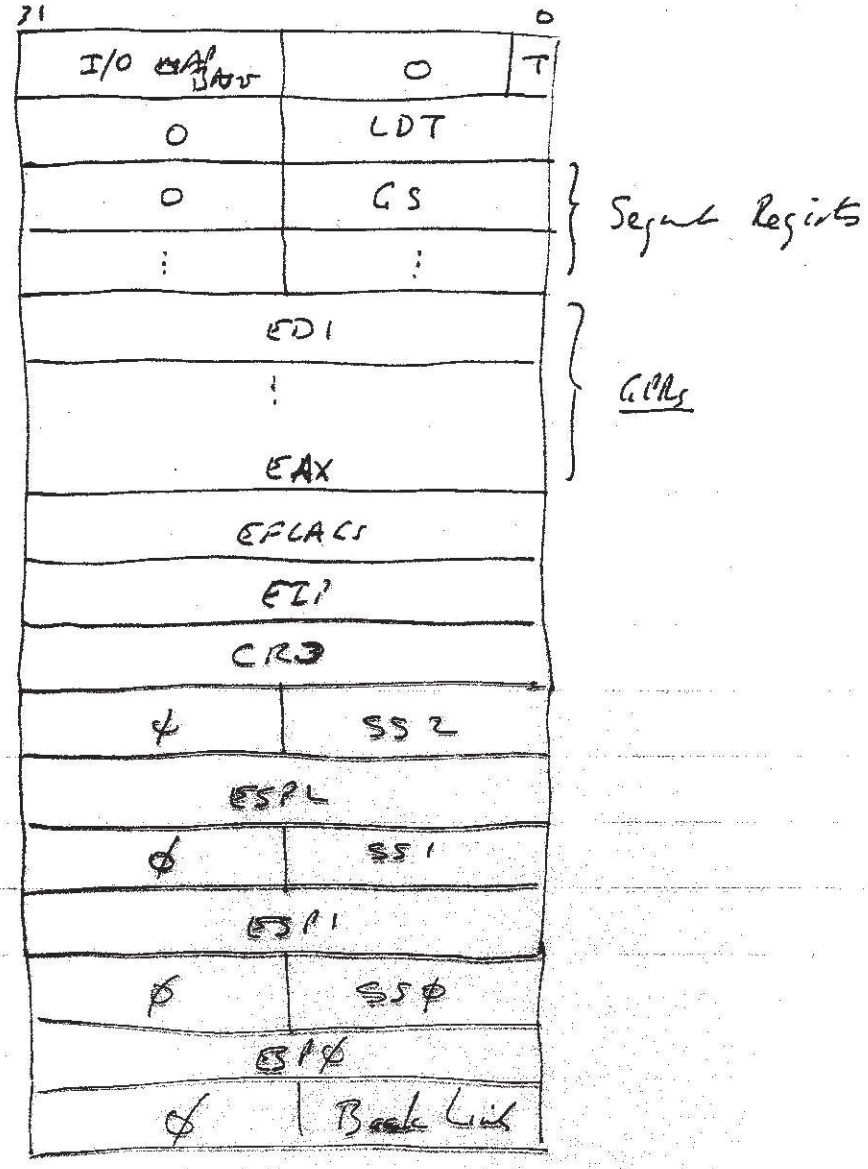
2^{13} × 8 bytes each

Segment Descriptor

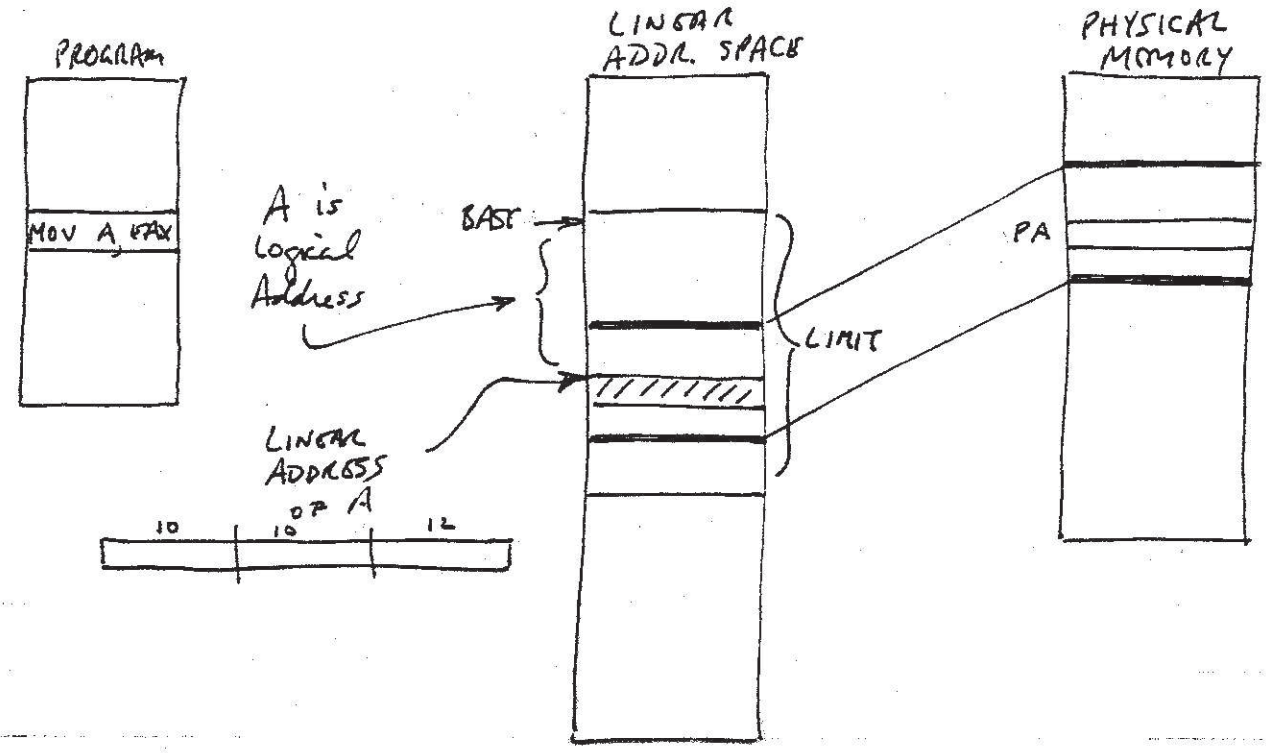


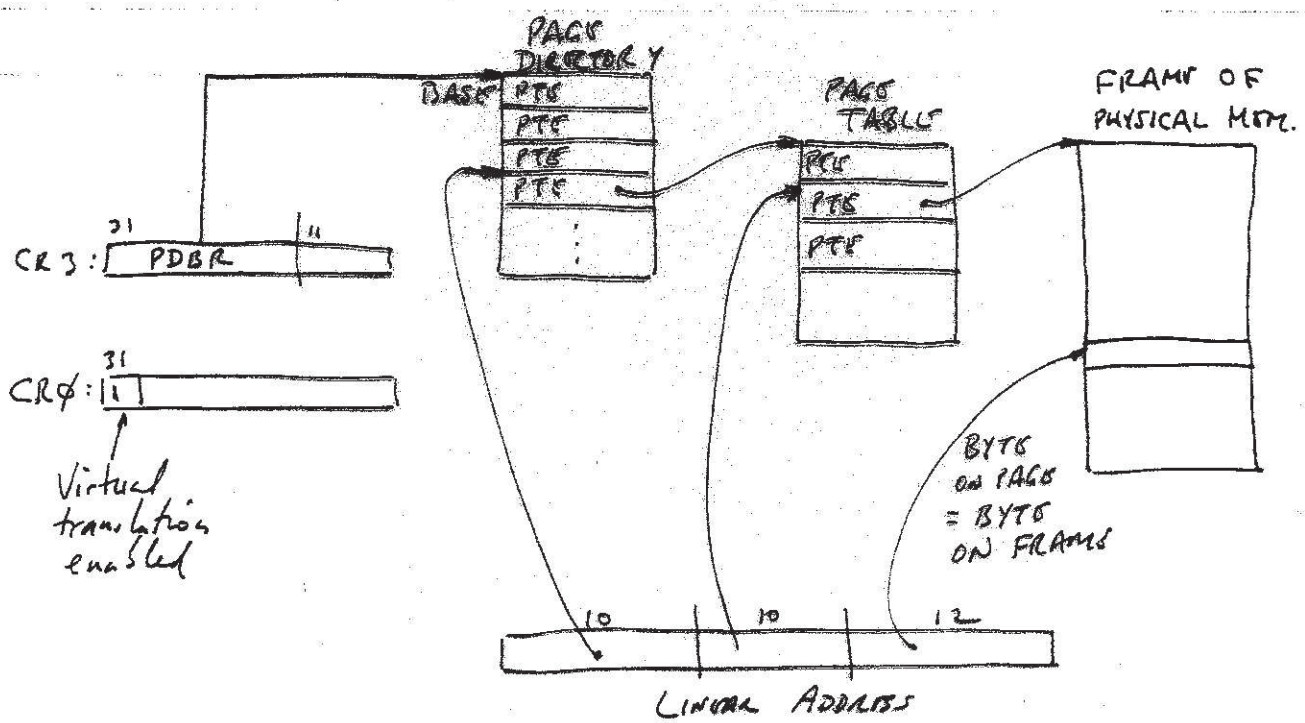
G: Granularity 1 BYTE / 4KBYTES
P: Segment Present
PL: Privilege Level
TYPE: Segment type

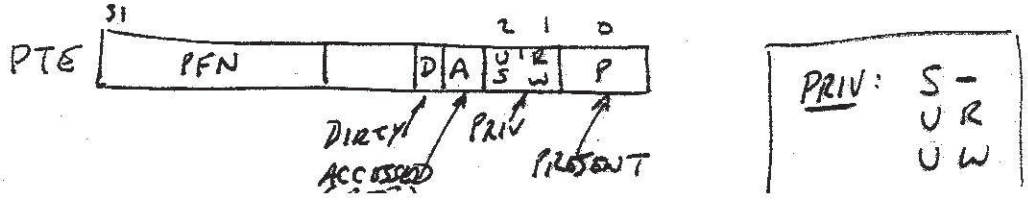
Task State Segment (TSS)



Segmentation AND Paging







PRIV: S –
U R
U W