Department of Electrical and Computer Engineering
The University of Texas at Austin

ECE 382N, Spring 2010
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"Compile-time" Course Outline
January 20, 2010

January 20: **First class meeting**. Introduction to the course, administrative details. Focus of the course: Principles and Tradeoffs. Levels of transformation, Instruction supply, data supply, processing.

January 25,27: Introduction to the CAD tools we will be using in the course.
[Note: Problem set 1a is due at the beginning of Jan 27 class]

February 1: Basic concepts in architecture and microarchitecture. Critical path, Bread and Butter Design, Compile time vs. Run time. Partitioning, Timing, Pipelining. Data Path, state machine, microsequencer, microinstruction definition, and microcode. Microprogramming (horizontal, vertical, two-level, dynamic microprogramming, bit steering). Pipelining and pipelined control.

February 2: Discussion session. Review of the use of the CAD tools on the logic design of a simple ALU.

February 3: The x86 ISA in the context of ISA tradeoffs. Some implementation issues.

February 8: ISA/Microarchitecture tradeoffs

February 9: Discussion sesssion
[Problem set 1b is due at the beginning of this class].

February 10: Evolution of the uniprocessor, including SIMD, VLIW, DAE, HPS, Data Flow. The basic Superscalar, out-of-order execution model. Effective use of long pipelines without blocking. The structure of a modern pipeline. Functions at each stage.

February 15: Evolution of the uniprocessor, continued. Data Flow

February 16: Discussion session

February 17: Run-time optimizations: Trace Cache, Runahead, etc.

February 22: Discussion sessions -- Problem sets 3,4,5.
[Problem set 2 is due at the beginning of this class.]

February 24: Multi-threading -- HEP, SMT, SSMT

March 1: Compile time optimizations: The Block-structured ISA, Predication, leading to wish branches, Braids, etc. Preview to the future: multiple levels of cache, fast track/slow track.

March 2: Discussion session.

March 3: Compile time optimaztions, continued.

March 5: Problem Set 4 due in ENS 541, at 5pm.

March 8: No class. Prepare for Initial Design Review.

March 10, 11: **Initial project design reviews in 537 ENS.**

March 15-19: Spring break, no classes.

March 22: Branch Prediction

March 24: Branch Prediction, continued.

March 29: Review, or catch up, as needed.

March 30: Discussion session, prepare for written exam.

March 31: **Written exam, in class**.

April 5: Measurement methodology and abuses.

April 6: Discussion session, as needed.

April 7: RISC, a Retrospective.

April 12: Intro to Multiprocessing.

April 13: Discussion session, as needed.

April 14: Multiple processors: Cache Coherency.

April 15,16: **Oral exams (exam2) in 541a ENS.**

April 19: Memory consistency, transactional memory

April 20: Discussion session, as needed.

April 21: Prefetching in the context of Multi-core.

April 26: Multi-core, Multi-nonsense, and the microprocessor of the year 2020.

April 27: Discussion session, as needed.

April 28: Case Studies: Pentium M, Niagara, Cell, Power 6, GPGPUs.

May 3: Guest lecture from local industry (to be determined).

May 4: Discusssion session, as needed.

May 5: Last class meeting. Review of the course.

Final project design reviews in 541a, May 6,7 by appointment.
May 9: Final project report due in 541a, 10pm.

Note: there will be no final exam in this course.