Cache Memory

WHY?

CPU

Memory

0.25

0.5

1 nsec

100 nsec
The Abstraction

Physical Address

Tag Store

To see if it is there (Also called Cache A)

"Yes" (A Hit!)

Data (Also called Cache D)

To get It

Data

Note: Hit Ratio =

\[
\frac{\text{Hits}}{\text{Hits + Misses}}
\]
**Write Through/Write Back**

```
PROC -> CACHE -> MEM
```

```
PROC -> CACHE -> MEM
```

**Issues**

- Simplicity of Design
- Bus Traffic
- Application Environment (Stack Frame)
- Allocate on Write Miss
  - Sector Cache
Characteristics

* Set Associative (Set Size)
  - Fully Associative
  - Direct Mapped

* Write Back, Write Through

* Replacement Algorithm
  - LRU
  - FIFO
  - Random

* Instructions/Data

* Supervisor/User

* Virtual/Physical
Tag Store Entry: LRU

TAG STORE ENTRY:

<table>
<thead>
<tr>
<th>TAG</th>
<th>V</th>
<th>D</th>
<th>Replace</th>
</tr>
</thead>
</table>
1. Sleep well your day
2. Consisted state

Almost was

Now some

Intend

Explain