Each cache line in memory has $p+1$ bits.
Each cache line in each cache has 1 bit.
Cache Coherency
(Snoopy Cache)

Update
Invalidate

INV
DIRTY
RSVD
Shared

PR, PW
PR, PW
PR

Goodman
ISCA 1983
→ Iannello
Illinois
ISCA 1984
Rudolph
1984
Bently
1985

WRITE ONCE

| Cache Line | DATA
|------------|------
|            | 128M
|            | SYNAPSE
|            | S. Frank

Memory

BUS

Update
Invalidate
Memory Consistency

Critical Section

A: C1 = 1
B: if (C2 = ∅) {critical section}
C: C1 = ∅

L1 = ∅
L2 = ∅

L1 = 0
L2 ≠ ∅

X: L2 = 1
Y: if (L1 = ∅) {critical section}
Z: L2 = ∅

Leslie Lamport
~1978

Sequential Consistency

Sequential Consistency
A well-meaning student told me to get rid of this slide. $cm^*$ is old. People will think you are an old man, and not take you seriously.