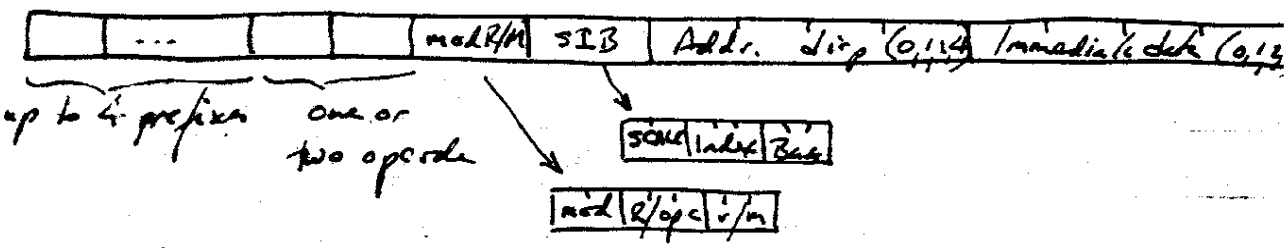
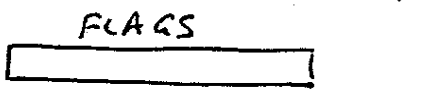
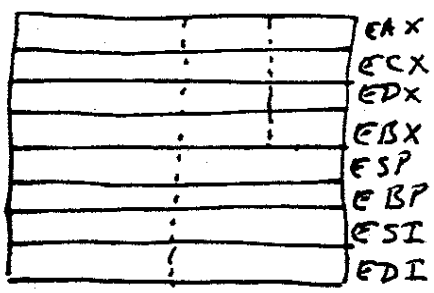
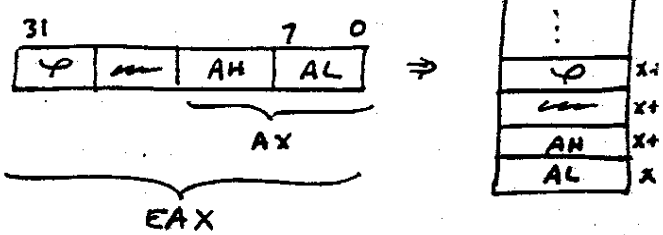
Characteristics of the ISA

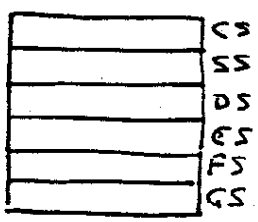
* First, the example : IA-32 :











* Variable length vs. fixed length
  - bit/byte (432)
  - uniform decode
  - sequential decode (opcode first/last)

* Condition codes vs. register operands

* Addressing modes
  - side effects (e.g., (Rx)+)

Characteristics of the ISA (Continued)

* Use of Segment registers
  - Protection vs. Virtual memory

* Predicated instructions (HPPA, CMOV)

* LD/ST vs. Memory operands
  - Early advantage to LD/ST (pre-decoupling)

* Interlocks
  - MIPS example (the other extreme)

* Zero-address, ... three address
  - Stack
  - 2 operand (extra moves)
  - 3 operand

* Compatibility
  - Today's win → tomorrow's loss
    - delayed branch
    - register windows
  - Why? - obvious

* Semantic-gap instructions
  - EDITPC, INDEX (VAX)
  - FINDFIRST (e.g., AMD 29000)
  - Context switch
  - Procedure call/ret

Characteristics of the ISA (Continued)

* Semantic-gap instructions (continued)
  - INSQUE, REMQUE
  - friends (Multiply-accumulate)

* Future (Promote march to ISA)
  - Multiple prefetch/poststore
    - FETCH 1, FETCH 2, FETCH 3
    - STORE 2, STORE 3, STORE_MEM
  - Branch prediction instructions

* Program-friendly vs. unfriendly
  - addressing modes
  - aligned accesses
  - vectored interrupts
  - ADDC