Characteristics of the ISA

1. First, the example: IA-32.

```
... modRM SIB Addr. Disp (6,14) Immediate (32)
```

2. Variable length vs. fixed length
   - bit/byte (432)
   - uniform decode
   - sequential decode (opcode first/last)

3. Condition code vs. register operands

4. Addressing modes
   - side effects (e.g., (dx) +)
Characteristics of the ISA (Continued)

* Use of Segment registers
  - Protection vs. Virtual memory

* Predicated instructions (HPPA, CMU) 

* LD/ST vs. Memory operands
  - Early advantage to LD/ST (pre-decoupling)

* Interlocks
  - MIPS example (the other extreme)

* Zero-address, ... three address
  - Stack
    - 2 operand (extra moves)
    - 3 operand

* Compatibility
  - Today's win -> tomorrow's loser
    - delayed branch
    - register windows

  - Why? - obvious

* Semantic gap instructions
  - EDITIC, INDEX (VAX)
  - FINDFIRST (85, AMD 29000)
  - Context switch
  - Procedure call/ret
  - The line is...
Characteristics of the ISA (Continued)

- Semantic-gap instructions (Continued)
  - INSQUE, REMOVE
  - triads (Multiply-accumulate)

- Future (Promote hard to ISA)
  - Multiple prefetch/post-store
    - FETCH1, FETCH2, FETCH3
    - STORE2, STORE3, STORE-MEM
  - Branch prediction instructions

- Program-friendly vs. unfriendly
  - addressing modes
  - aligned accesses
  - vectorized interop
  - ADDC