Department of Electrical and Computer Engineering
The University of Texas at Austin

EE460N, Fall 2020
Yale N. Patt, Instructor
TAs: Chester Cai, Sean Stephens, Arjun Ramesh
Course Outline
August 26, 2020

August 26: Lecture 1: Intro to the course. Levels of Transformations. Basic architectural choices. Science of Tradeoffs.

August 27,28: First Discussion Session. Bookkeeping, overview,expectations,PL0, Intro/Focus

> Programming Lab 0 is due, Sunday night, August 30, 11:59pm. (The program itself will be empty. The purpose of the assignment is to make sure we are on the same page re: using the system.)

August 31: Lecture 2: Intro/focus, continued. Tradeoffs, Latency and Bandwidth, Role of Parallelism, Role of Speculation, Overview of Quantitative Insights, Role of the Architect, Alternative Design Points.

September 2: Lecture 3: Intro to Instruction Set Architecture, with examples taken from many diverse ISAs. ISA tradeoffs. Detailed discussion of LC-3b, with Assembly language constructs. The Assembler, how it works.

September 3,4: Discussion Session. The ISA, Assembly Process, PL1.

September 7: Labor Day, no class.

September 9: Lecture 4: Microarchitecture, LC-3b data path, state machine, microsequencer, two-level microprogramming, Wilkes' Diode Matrix, Choice of ASICs, FPGAS, EMT instruction for enhanced performance

September 10,11: Discussion Session. Microarchitecture, PL1.

September 14: Lecture 5: Microarchitecture, continued. Microarchitecture Tradeoffs, Enhancing Performance. Pipelining, and its implications. Scoreboarding and its limitations.

> Problem set 1 due before class, September 16. (Emphasis: ISA, uarch of the LC-3b, the Assembly Process, Pipelining)

September 16: Lecture 6: Microarchitecture, continued. (Out of order Execution, the Tomasulo Algorithm)

September 17,18: Discussion session: Microarchitecture, PL1

> Programming Lab 1 is due, Sunday night, September 20, 11:59pm. (Write a program in LC-3b Assembly Language. Write an Assembler. Assemble the program you have written.)

September 21: Lecture 7: Microarchitecture, continued. Branch Prediction, other mechanisms for handling conditional branches. The HEP.

September 23: Lecture 8: The notion of Process, the unit of work managed by the Operating System, and its implications on Interrupts/Exceptions and on Virtual memory.

September 24,25: Discussion session: Pipelining, Scoreboard, Tomasulo, PL2.

> Programming Lab 2 is due, Sunday night, September 27, 11:59pm. (Write a program in C that simulates at the instruction cycle level the baseline LC-3b ISA. Test your simulator with the output of the assembler for the application program written in Programming Lab 1.)

September 26: Lecture 9: Physical Memory. SRAM, DRAM, NVM. Interleaving, Unaligned accesses. (Note: this lecture, normally scheduled for Monday, September 28, will be given on September 26. As all lectures, it will be recorded, and available anytime thereafter, in particular, on September 28 when it would normally have been given.

September 30, Lecture 10. Physical Memory, continued.

October 1,2: Discussion Session. Physical Memory, Prepare for first midterm.

> Problem set 2 due before class, October 5. (Emphasis: uarch of the LC-3b, the Assembly Process, Pipelining Branch Prediction, Tomasulo)

October 5, Lecture 11: Review for Exam 1.

October 7: Lecture 12: Exam 1

October 8,9: Discussion Session. Go over the exam, PL3

October 12: Lecture 13: Virtual memory, page tables, TLB, VAX model, IA32 model, Translation and Protection, contrast with segmentation.

October 14: Lecture 14: Virtual Memory, continued.

October 15,16: Discsussion session: Virtual Memory, PL3

> Programming Lab 3 is due, Sunday night October 18, 11:59pm.
> (Finish the clock-cycle level Simulator for the LC-3b.
> Test it on the application program written in Programming Lab 1.)

October 19: Lecture 15: Virtual Memory, continued.

October 21: Lecture 16: Cache memory.

October 22,23: Discussion session: Cache Memory.

October 26: Lecture 17: Cache memory, continued.

October 28: Lecture 18: Input/Output. Asynchronous/Synchronous, Arbitration, Transaction.

October 29,30: Discussion session: Cache Memory, I/O, PL4

> Problem set 3 due before class, November 2. (Physical Memory, Virtual Memory, Cache memory, Process)

NOTE: October 29 is the last day to drop a class, change to CR/NC for academic reasons.

November 2: Lecture 19: Input/Output, continued.

November 4: Lecture 20: Integer Arithmetic

November 5,6: Discussion Session: I/O, Integer Arithmetic, PL4.

> Programming Lab 4 is due, Sunday night November 8, 11:59pm.
> (Interrupts/Exceptions)

November 9: Lecture 21: Floating point arithmetic and the IEEE Standard. Instruction formats, Gradual underflow, Rounding modes, NaNs, Floating Point Exceptions.

November 11: Lecture 22: Single-thread parallelism. SIMD, Vectors, VLIW vs Wide Issue, DAE.

November 12,13:: Discussion session: Arithmetic, Prepare for Exam 2.

Problem set 4 due before class, November 16.

November 16: Lecture 23: Review.

November 18: Lecture 24: Exam 2.

November 19,20: Discussion Session: Go over Exam 2. PL5.

November 23: Lecture 25: Single-thread parallelism, continued. (HPS, Data Flow).

November 25: No class, Thanksgiving break.

Programming Lab 5 is due, Sunday night November 29, 11:59pm. (Virtual memory)

November 30: Lecture 26: Intro to Multiprocessing, Amdahl's Law, Speed-up, efficiency, Interconnection networks, Cache Coherency, Memory Consistency.

December 2: Lecture 27: Pot Pourri -- Measurement methodology, GPUs, Spatial computing, RISC, Intro Intellectual Property.

December 3,4: Discussion session. PL6, multiprocessing, Review of the course, Prepare for Final exam.

Programming Lab 6 is due, Monday afternoon, December 7, 5pm. (Pipelining)

December 7: Lecture 28: Last class, free for all!

Problem set 5. To be used as a study guide, not to be turned in.

Final exam: Probably Friday, December 11, 7-10pm.

Please note: The Registrar has the right to change the dates of the final exams. Please keep checking the Registrar's website and our announcements to be sure when the final exam will be given.