Department of Electrical and Computer Engineering The University of Texas at Austin

Yale N. Patt, Instructor TAs: Kayvan Mansoorshahi, Michael Chen Course Outline August 22, 2022

August 22: Lecture 1: Intro to the course. Levels of Transformations. Basic architectural choices. Science of Tradeoffs.

August 24: Lecture 2: Intro/focus, continued. Tradeoffs, Latency and Bandwidth, Role of Parallelism, Role of Speculation, Overview of Quantitative Insights, Role of the Architect, Alternative Design Points.

August 25,26: First Discussion Session. Bookkeeping, overview, expectations, PL0, Intro/Focus

Programming Lab 0 is due, Sunday night, August 28, 11:59pm. (The program itself will be empty. The purpose of the assignment is to make sure we are on the same page re: using the system.)

August 29: Lecture 3: Intro/focus (continued).

August 31: Lecture 4: The first programming lab, PL1, Discussion with the TAs.

September 1,2: Discussion Session. The ISA, Assembly Process, PL1.

Programming Lab 1 is due, Sunday night, September 4, 11:59pm. (Write a program in LC-3b Assembly Language. Write an Assembler. Assemble the program you have written.)

September 7: Lecture 5: Intro to Instruction Set Architecture, with examples taken from many diverse ISAs. ISA tradeoffs. Detailed discussion of LC-3b, with Assembly language constructs. The Assembler, how it works.

September 8,9: Discussion Session. PL2.

Programming Lab 2 is due Sunday night, September 11, 11:59pm. (Write a program in C that simulates at the instruction cycle level the baseline LC-3b ISA. Test your simulator with the output of the assembler for the application program written in Programming Lab 1.)

September 12: Lecture 6: ISA, continued.

September 14: Lecture 7: Microarchitecture, LC-3b data path, state machine, microsequencer, two-level microprogramming, Wilkes' Diode Matrix, Choice of ASICs, FPGAS, EMT instruction for enhanced performance

September 15,16: Discussion Session. Microarchitecture, PL3

Problem set 1 due before class, September 19. (Emphasis: ISA, microarchitecture basics, the Assembly Process)Student Information Sheet also due. See handouts section of website.

September 19: Lecture 8: Microarchitecture, continued. Microarchitecture Tradeoffs, Enhancing Performance. Pipelining, and its implications. Scoreboarding and its limitations.

September 21: Lecture 9: Microarchitecture Enhancements. (Out of order Execution, the Tomasulo Algorithm)

September 22,23: Discussion Session. (Emphasis on microarchitecture, process, PL3)

September 26: No In-Person Lecture. Lecture 10: Microarchitecture Enhancements, continued. Branch Prediction, other mechanisms for handling conditional branches. The HEP.

Programming Lab 3 is due, Tuesday night September 27, 11:59pm. (Finish the clock-cycle level Simulator for the LC-3b. Test it on the application program written in Programming Lab 1.)

September 28: Lecture 11: The notion of Process, the unit of work managed by the Operating System, and its implications on Interrupts/Exceptions and on Virtual memory.

September 29,30: Discussion session. (Review PL3, process, emphasis on PL4)

October 3: Lecture 12: Integer Arithmetic

October 5: No class

October 6,7: Discussion Session. Prepare for first midterm.

Problem set 2 due before class, October 10. (Emphasis: Arithmetic, Process, microarchitecture)

October 10: Lecture 13: Floating point arithmetic and the IEEE Standard. Instruction formats, Gradual underflow, Rounding modes, NaNs, Floating Point Exceptions.

October 12: Lecture 14: Exam 1

October 13,14: Discussion Session. Go over the exam, PL4

Programming Lab 4 is due Sunday night, October 16, 11:59pm. Add state, data path, and microsequencer to handle interrupts and exceptions.

October 17: Lecture 15: Virtual memory, page tables, TLB, VAX model, IA32 model, Translation and Protection, contrast with segmentation.

October 19: Lecture 16: Virtual Memory, continued.

October 20,21: Discussion Session. (Emphasis on Virtual Memory, PL5)

October 24: Lecture 17: Physical Memory. SRAM, DRAM, NVM. Interleaving, Unaligned accesses.

October 25: Last day an undergraduate may: Q-drop a class; withdraw; change a class to pass/fail

October 26: Lecture 18: Physical Memory, continued.

October 27,28: Discussion session: Physical Memory, PL5

Problem set 3, due before class, October 31. (Emphasis on Physical Memory, Virtual Memory.)

October 31: Lecture 19: Cache memory

November 2: Lecture 20: Cache memory, continued.

November 3,4: Discussion session: Cache Memory, PL5

Programming Lab 5 is due, Sunday night November 6, 11:59pm. (Add state, data path, and microsequencer to handle Virtual memory)

November 7: Lecture 21 Input/Output. Asynchronous/Synchronous, Arbitration, Transaction.

November 9: Lecture 22: Input/Output, continued.

November 10,11: Discussion Session: Prepare for second midterm Exam

Problem set 4, due before class, November 14. (Emphasis on Cache, I/O)

November 14: Lecture 23: Single-thread performance SIMD, Vectors, VLIW vs Wide Issue, DAE, HPS, Data Flow

November 16: Lecture 24: Exam 2.

November 17,18: Discussion Session: Go over second exam, PL6

November 21-25: No class, Thanksgiving break.

November 28: Lecture 25: Intro to Multiprocessing, Amdahl's Law, Speed-up, efficiency, Interconnection networks, Cache Coherency, Memory Consistency.

November 30: Lecture 26: (If there is time) Pot Pourri – Measurement methodology, GPUs, Spatial computing, RISC, Intro to Intellectual Property.

December 1,2: Discussion session. PL6, multiprocessing, Review of the course, Prepare for Final exam.

December 5: Lecture 27: Last class, free for all!

Programming Lab 6 is due, Monday afternoon, December 5, 5pm. (Pipelined implementation of the LC-3b)

Problem set 5. To be used as a study guide for the final exam, not to be turned in.

Final exam: Probably Friday, December 9, 7-9pm.

Please note: The Registrar has the right to change the dates of the final exams. Please keep checking the Registrar's web site and our announcements to be sure when the final exam will be given.