

CURRICULUM VITAE - Yale N. Patt

PERSONAL

Yale N. Patt
901 W. 9th Street, Suite 603, Austin, TX 78703
(or, Electrical and Computer Engineering Department, The University of Texas at Austin,
1 University Station C0803 Austin, TX 78712-0240)

EDUCATION

Northeastern University, B.S. in Electrical Engineering, June 1962
Stanford University, M.S. in Electrical Engineering, June 1963
Stanford University, Ph.D. in Electrical Engineering, June 1966

PRIMARY EMPLOYMENT (Since obtaining the PhD)

Professor of Electrical and Computer Engineering, and Ernest Cockrell, Jr. Centennial Chair in Eng'g, U of Texas at Austin	7/99-present
Professor of Electrical Eng'g & Computer Science, University of Michigan	11/88-6/99
Visiting Professor, Elec. Eng'g & Computer Science, U.C. Berkeley	9/79-8/88
Professor of Computer Science and Mathematics, S.F. State University	8/76-6/89
Associate Professor of Computer Science and E.E., N.C. State University	1/69-5/76
Captain, U.S. Army, assigned to U.S. Army Research Office	6/67-6/69
Assistant Professor of Electrical Engineering, Cornell University	9/66-6/67

HONORS AND AWARDS

IEEE/ACM Eckert-Mauchly Award, 1996, "for important contributions to instruction level parallelism and super-scalar processor design."

2000 ACM Karl V. Karlstrom Outstanding Educator Award, "for great ability, dedication, and success in developing computer science education, and for outstanding achievements as a teacher."

1995 IEEE Emanuel R. Piore Award (the IEEE Technical Field Medal for Information Processing), "for contributions to computer architecture leading to commercially viable high performance microprocessors."

1999 IEEE Wallace W. McDowell Award, "for your impact on the high performance microprocessor industry via a combination of important contributions to both engineering and education."

2005 IEEE Charles Babbage Award, "for fundamental contributions to high performance processor design."

Honorary Doctorate, University of Belgrade, 2009, "for fundamental contributions to microprocessor design."

Fellow, IEEE, for "Innovative contributions to the implementation of high performance computer architectures."

Fellow, ACM, for "many outstanding seminal contributions to high performance microarchitecture and for leadership and teaching in computer science and engineering education."

IEEE/ACM 2007 ISCA Most Influential Paper of the Year Award, for "the paper published in ISCA in 1992 that has had the most impact on the field (in terms of research, development, products or ideas) during the 15 years since it was published." For: "Alternative Implementations of Two-Level Adaptive Branch Prediction."

IEEE Third Millennium Medal, April, 2000.

IEEE Computer Society Golden Core Award, 1996.

Outstanding Lecturer of the Year, National ACM Lectureship Program, 2000-01.

Outstanding Lecturer of the Year, National ACM Lectureship Program, 1998-99.

Texas Excellence Teaching Award, presented by the Texas Exes (the University's Alumni Association), 2002.

Dad's Association Centennial Teaching Fellowship, The University of Texas at Austin, Fall semester, 2002.

Appointed Arthur F. Thurnau Professor at the University of Michigan, March, 1998, "for his excellence in teaching and his dedication to undergraduate students."

Member, Sigma Xi, Tau Beta Pi, Eta Kappa Nu Honor Societies.

National Tau Beta Pi Fellow, 1962-1963.

1997 Research Excellence Award, University of Michigan, Dept of Electrical Engineering and Computer Science.

1996 Outstanding Teacher Award, University of Michigan, College of Engineering.

1995 Teaching Excellence Award, University of Michigan, Dept of Electrical Engineering and Computer Science.

Outstanding Professor of the Year, 1991-1992, selected by the Michigan student chapter of Eta Kappa Nu.

Adaptive Insertion Policies for High-Performance Caching. *IEEE Micro*, Top Picks Special Issue, January/February, 2008. (with Moinuddin K. Qureshi, Amer Jaleel, Simon C. Steely Jr., and Joel Emer).

Diverge-Merge Processor: Generalized and Energy-Efficient Dynamic Predication, *IEEE Micro*, Top Picks Special Issue, January/February, 2007, (with Hyesoon Kim, Jose Joao, and Onur Mutlu).

Techniques for Efficient Processing in Runahead Execution Engines. *IEEE Micro*, Top Picks Special Issue, January/February, 2006, (with Onur Mutlu and Hyesoon Kim).

Wish Branches: Combining Conditional Branching and Predication for Adaptive Predicated Execution, *IEEE Micro*, Top Picks Special Issue, January/February, 2006, (with Hyesoon Kim, Onur Mutlu, and Jared Stark).

Runahead Execution: An Effective Alternative to Large Instruction Windows, *IEEE Micro*, Top Picks Special Issue, November/December, 2003. (with Onur Mutlu, Jared Stark, and Chris Wilkerson).

Best paper award in Hardware-Architecture at the 22nd Annual HICSS conference, January, 1989, "Tailoring Functional Units and Memory in a High Performance Prolog Architecture."

Best paper award in Hardware-Architecture at the 21st Annual HICSS conference, January, 1988, "HPSm2: A Refined Single Chip Microengine."

Best paper award in Hardware-Architecture at the 20th Annual HICSS conference, January, 1987, "A Clarification of the Dynamic/Static Interface."

Best paper award in Hardware-Architecture at the 19th Annual HICSS conference, January, 1986, "An HPS Implementation of VAX: Initial Design and Analysis."

KEYNOTE ADDRESSES

Keynote address, International Symposium on Systems, Architectures, MOdeling and Simulation (SAMOS IX), July 2009, Samos.

Keynote address, ACS/IEEE International Conference on Computer Systems and Applications (AICCSA-2009), May, 2009, Rabat, Morocco. Title: Future Computer Systems and Applications: Revisiting Conventional Wisdom in the context of Multi-core and Many-core.

Keynote address, 22nd International Conference on Computing Systems (ARCS 2009), March, 2009, Delft. Title: The Challenges of Multicore: Information and Misinformation.

Keynote address, 15th IEEE International High Performance Computer Architecture Symposium (HPCA-15), February, 2009, Raleigh, N.C. Title: Multi-core demands Multi-interfaces.

Keynote address, European Union HiPEAC Summer School for PhD students in Computer Architecture and Embedded Systems (ACACES), July 2008, L'Aquila, Italy. Title: The Multi-core Era: What does it mean? (and even more importantly, what does it NOT mean?).

Keynote address, International Symposium on Systems, Architectures, MOdeling and Simulation (SAMOS VIII), July 2008, Samos. Title: Can it be fixed? Some thoughts after 40 years in the business.

Keynote address, 2008 IEEE International Conference on Networking, Architecture and Storage, June 2008, Chongqing, China. Title: The Microprocessor in the Year 2018.

Keynote address, HiPC Symposium on High Performance Computer Architecture, Goa, India, December 2007. Title: The Transformation Hierarchy in the Era of Multi-Core.

Keynote address, 25th International Conference on Computer Aided Design (ICCD), Squaw Valley, October 2007. Title: Microprocessor Performance, Phase II: Harnessing the Transformation Hierarchy.

Keynote address, Second Spanish Conference on Informatics (CEDI 2007), Zaragoza, September, 2007. Title: The Microprocessor Ten Years from Now: Why it is Relevant to all Informatics.

Keynote address, 16th International Conference on Parallel Architecture and Compiling Techiques (PACT), Brasov, Romania, September 2007. Title: Harnessing the Transformation Hierarchy.

Keynote address, Workshop on Computer Architecture Education (WCAE 2007), in conjunction with ISCA, San Diego, June, 2007. Title: LC-3, x86, or ??: The First ISA for Students to Study.

Keynote address, Student Congress, Durango, Mexico, September 2006.

Keynote address, 33rd Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), Boston, June, 2006. Title: Computer Architecture Research and Future Microprocessors: Where do we go from here?

Keynote address, 2006 Spring convention of the State of New Jersey High School Science and Math Teachers, Newark, March, 2006. Title: Education: Some thoughts after 35 years in the trenches.

Keynote address, 4th Annual Dalhousie Computer Science In-House Conference, Halifax, Nova Scotia, September, 2005. Title: The Microprocessor: Its Characteristics Ten Years from Now.

Keynote address, 4th annual Encuentro Estudiantil (National ACM Congress of Mexican Computer Science Students), Puebla, March, 2005. Title: Are there any questions?

Keynote address, 3rd IEEE/ACS International Conference on Computer and System Applications (AICCSA-05), Cairo, Egypt, January, 2005. Title: The Microprocessor of the Year 2014: Do Pentium 4, Pentium M, and Power 5 provide any hints?

Keynote address, 16th Symposium on Computer Architecture and High Performance Computing, Foz du Iguazu, Brazil, October, 2004. Title: The Microprocessor of the Year 2014: Do Pentium 4, Pentium M, and Power 5 provide any hints?

Plenary address, XXIX Pan-American Engineering Symposium, Mexico City, September, 2004. Title: Future Trends in Computer Architecture.

Plenary address, 2004 International Supercomputer Conference, Heidelberg, June, 2004. Title: "The processor in 2014: What are the challenges, how do we meet them?"

Keynote address, 2004 IEEE International Symposium on Performance Analysis of Systems and Software, Austin, March, 2004. Title: Performance Analysis: A big plus, or an even bigger minus.

Keynote address, 10th annual IEEE International Symposium on High Performance Computer Architecture (HPCA-10), Madrid, Spain, February, 2004. Title: Microarchitecture: Are we finally done?

Keynote address, HiPC 2003, Hyderabad, India, December, 2003. Title: The High Performance Microprocessor in the Year 2013: What will it look like? What it won't look like?

Keynote address, International Conference on Information Technology (CIT), Bhubaneswar, India, December, 2003. Title: Current bottlenecks to continued high performance microprocessors, and what we can do to get passed them.

Keynote address, SSGRR 2003s, L'Aquila, Italy, July, 2003. Title: A Microarchitect's perspective: What computer technology will provide and won't provide by the year 2020.

Keynote address, Computer Architecture Education Workshop, International Symposium on Computer Architecture (ISCA), June, 2003. Title: Teaching and Teaching Computer Architecture: Two Very different topics (Some Opinions about each).

Keynote address, 2nd annual Encuentro Estudiantil (National ACM Congress of Mexican Computer Science Students), Guanajuato, May, 2003. Title: What is Moore's Law REALLY all about?

Keynote address, ICCD, Austin, TX, September, 2001. Title: There is still plenty of work that needs to get done.

Keynote address, 26th EuroMicro Congress, Maastricht, Netherlands, September, 2000. Title: Higher and Higher Performance Microprocessors: Are the Problems Just too Hard to Solve?

Plenary address, EuroPar-2000, Munich, Germany, August, 2000. Title: Despite the Nay-Sayers to the Contrary, Moore's Law is Alive and Well and Still Providing Opportunities.

- Keynote address, Seventh International Conference on Advanced Computing, Roorkee, India, December, 1999.
- Keynote address, International Symposium on New Trends in Computer Architecture, Gent, Belgium, December, 1999.
- Keynote address, 11th Symposium on Computer Architecture and High Performance Computing, Natal, Brazil, September, 1999.
- Keynote address, Workshop on Workload Characterization, 31st Annual Symposium on Microarchitecture, Dallas, TX, November 1998.
- Keynote address, Workshop on Simultaneous Multithreading, 4th Annual High Performance Computer Architecture Conference (HPCA-4), Las Vegas, January, 1998.
- Keynote address, Computer Architecture Education Workshop, 4th Annual High Performance Computer Architecture Conference (HPCA-4), Las Vegas, January, 1998. Title: High Tech -- The Enemy of Education?
- Keynote address, IEEE/ACM 11th Annual International Supercomputer Conference, Vienna, July, 1997.
- Keynote address, IEEE International Performance Conference on Computers and Communications, Phoenix, Arizona, February, 1997.
- Keynote address, IBM Conference on Performance Analysis and its Influence on Computer Design, Austin, March 27, 1996.
- Plenary address, 29th Annual Hawaii International Conference on System Sciences, Maui, January, 1996. Title: The Microprocessor and its Performance in the Year 2000.
- Plenary address, ACM/IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT95), Limassol, Cyprus, June, 1995.
- Keynote address, International Congress on Massively Parallel Information Systems, Ischia, Italy, May, 1994.
- Keynote address, International Federation of Information Processing (IFIP) Working Conference on Architectures and Compilation Techniques for Fine and Medium Grain Parallelism, Orlando, Florida, January, 1993. Title: The Compiler and the Microarchitecture: Partners, not Adversaries.
- Keynote address, 25th Annual IEEE/ACM International Symposium and Workshop on Microarchitecture, Portland, OR, November, 1992.
- Keynote address, Euromicro Congress 1992, Paris, September, 1992.
- Plenary address, 25th Annual Hawaii International Conference on System Sciences, Kauai, January, 1992. Title: What do we do about the Speed of Light?
- Keynote address, 5th International Congress on Computer Architecture and Performance Modeling, Torino, Italy, February, 1991. Title: "Computer Architecture and Performance Modeling, Obtaining Meaningful Information."
- Keynote address, NCR Corporation Workshop in Performance Measurement, Cambridge, OH, December, 1988. Title: "The light is better over here."
- Keynote address on "Computer Architectures for Artificial Intelligence," IEEE 1987 Symposium on Artificial Intelligence: Applications in Engineering, Minneapolis, Minnesota, January, 1987.
- Keynote address (Architecture) at the annual Livermore-Los Alamos invited Salishan Workshop on "Toward a Science of Parallel Computation," March, 1986.

DISTINGUISHED LECTURES

- Lecturer, University of Texas at Arlington Distinguished Lectures Series, December, 2008. Title: Education: Are there any questions?"
- Lecturer, Pennsylvania State University Distinguished Lectures Series, April, 2007. Title: The Fundamentals: Vehicle to the Year 2017- Tomorrow's Graduates, Tomorrow's Microprocessors
- Lecturer, The University of Arizona Distinguished Lectures Series, February, 2007. Title: The Microprocessor Ten Years from Now: What are the Challenges? What can we do about them?
- Lecturer, The European Union's 2nd Annual HiPEAC Summer School for PhD students, July, 2006, L'Aquila, Italy. Five 90 minute lectures on the subject, Advanced Microarchitecture.

The Saul Gorn Memorial Lecturer, University of Pennsylvania, April, 2006. Title: Computer Architecture Research: Is it Dead? Is it in need of Revitalization? Where do we go from here?

Lecturer, The University of Nebraska Distinguished Lecturer Series, April, 2006. Title: The Microprocessor Ten Years from Now.

Lecturer, The Northeastern University Distinguished Lecturer Series, April, 2006. Title: Future Microprocessors, where do we go from here?

The Irons Distinguished Lecturer, Rutgers University, March, 2006. Title: Future Microprocessors, where do we go from here?

Lecturer, The European Union's Inaugural HiPEAC Summer School for PhD students, July, 2005, L'Aquila, Italy. Five 90 minute lectures (Monday through Friday) on the subject Advanced Microarchitecture.

Lecturer, Distinguished Lecturer Series, SMU, April, 2005. Title: "The Microprocessor in the Year 2015: Issues, Challenges, Potential Avenues to Solutions."

Lecturer, ISTeC Distinguished Lecturer Series, Colorado State University, Ft. Collins April, 2005. Title: "Education. Are there any questions?"

Lecturer, Distinguished Lecturer Series, Computer Science Dept, Purdue University, March 2005. "Are there any questions?"

Lecturer, Distinguished Lecturer Series, Rice University, Houston, TX, November, 2004. Title: Trends in Computer Architecture.

Lecturer, Distinguished Lecturer Series, Courant Institute, New York University, October, 2004. Title: The Microprocessor of the Year 2014: Do Pentium 4, Pentium M, and Power 5 provide any hints?

Lecturer, Distinguished Lecturer Series, Carnegie Mellon University, Pittsburgh, April, 2004. Title: "The Microprocessor Ten Years from now: What are the challenges, how do we meet them?"

Lecturer, City University of Hong Kong Distinguished Lecture Series on Teaching and Learning, Hong Kong, January, 2004. Title: Ten Commandments of Good Teaching.

Lecturer, Distinguished Lecture Series, University of California, Irvine, December, 2003. Title: "Fundamentals: Moore's Law, Microarchitecture, and the Microprocessor of the year 2014."

Lecturer, Worcester Polytechnic Institute Distinguished Lecturer Series, September, 2003. Title: The High Performance Microprocessor in the Year 2013: Will the laws of Physics finally catch up with the Microprocessor development cycle?"

Lecturer, The University of Texas ECentury Distinguished Lecturer Series, March, 2003.

Robert T. Chien Memorial Lecture, University of Illinois, Urbana-Champaign, December, 2002.

Lecturer, the Harvard University Distinguished Lecture Series, October, 2002. "The Correct Way to Introduce Students to Computers."

Lecturer, The Erik Jonsson School of Engineering Distinguished Lecture Series, The University of Texas at Dallas, October, 2002.

Lecturer, University of Alberta Distinguished Lecturer Series in Electrical Engineering, October, 2002.

Lecturer, California State University at Fresno Distinguished Lecture Series in Computer Engineering, May, 2002.

The 2001-2002 Distinguished Lecturer in Computer Science, University of Wisconsin, La Crosse, April, 2002.

Lecturer, Georgia Tech Distinguished Lecturer Series in Computer Engineering, April, 2002.

The William Mong Distinguished Lecturer at the University of Hong Kong, March, 2002.

Lecturer, University of Illinois Distinguished Lecturer Series in Computer Science, February, 2002.

Lecturer, University of Pittsburgh Distinguished Lecturer Series, October, 2001.

The Birck Distinguished Lecturer, Purdue University Distinguished Lecture Series, March, 2001.

Lecturer, University of California, Riverside Distinguished Lecturer Series, January, 2001.

Lecturer, Colorado State University Distinguished Lecturer Series, April, 2000.

Lecturer, University of Delaware Distinguished Lecturer Series, March, 2000.

Lecturer, Texas A&M University Distinguished Lecturer Series, February, 2000.

Invited lecturer, HP2EUR Conference, Tromso, Norway, June, 1999.

Lecturer, Carnegie-Mellon University Distinguished Lecturer Series, April, 1998.

Lecturer, University of Southern California Distinguished Lecturer Series, February, 1998.

Lecturer, UCLA Distinguished Lecturer Series, November, 1996.

Lecturer, University of Southwestern Louisiana Distinguished Lecturer Series, November, 1996.

Lecturer, University of Texas, Austin Distinguished Lecturer Series, November, 1996.

Lecturer, Texas A&M University Shell Oil Distinguished Lecturer Series, February, 1996.

Distinguished lecturer, Taiwan Government. Series of three lectures, May 4,5, 1995. At ITRI, May 4: "HPS, The Microarchitecture for High Performance Processors." At Chiao Tung University, May 4: "The Next Challenge: a 10 IPC Processor." At National Taiwan University, May 5: "Branch Prediction: After Yeh's Algorithm, What?"

Invited lecturer, "Doctoral Network," a one-week summer school for leading PhD students in computer architecture, organized by the French National Education Administration, July, 1994.

Lecturer, Northwestern University Distinguished Lecturer Series, May, 1994.

Inaugural lecturer, the IEEE Distinguished Visitor Program for Asia and the Pacific. Lectures were presented in Bombay, Calcutta, Delhi, and Hong Kong, May 1993.

Lecturer, University of California, San Diego Distinguished Lecturer Series, April, 1992.

Lecturer, University of Maryland Distinguished Lecturer Series, November, 1991.

Distinguished Speaker, 1991 IEEE Joint Technical Committees Meeting, Rochester, New York, March 1991. Title: "Computer Architecture Choices.

Lecturer, Case-Western Reserve University Distinguished Lecturer Series, December, 1989.

Lecturer, Northeastern University Distinguished Lecturer Series, May, 1989.

Lecturer, Clemson University NCR Distinguished Lecturer Series, March, 1989.

At the invitation of the Ministry of Education of the Italian government, a series of 16 lectures on Advanced Concepts in Computer Architecture at the University of Pavia, May, 1985.

National Distinguished Visitor of the IEEE, 1989-93.

National ACM Lecturer: 1975-76, 1985-92, 1995-present.

OTHER NOTABLE TALKS

Invited speaker, 50th Anniversary Celebration of the first computer installed in Mexico, organized by the Commission on Science and Technology of the LX Legislature, Federal Government of Mexico, Camera de Diputados, Mexico City, September 3, 2008. Title: "Future Microprocessors and their implications for Computer Science Education in Mexico."

Invited speaker, "eContent Summit: Scenarios for the future," a workshop organized by the President of Croatia, Bruni, September, 2007. Title: eContent: Static vs. Dynamic; In Education, it makes a huge difference.

Featured speaker, IEEE Computer Society 60th Anniversary Celebration, Hotel Intercontinental, San Juan, Puerto Rico, June, 2006. Title: The Future of Computer * (Are we in Serious Trouble?).

Banquet address, 19th IEEE International Parallel & Distributed Processing Symposium, Denver, April, 2005. Title: A Unifying Theory of Distributed Processing.

Interview on "Newsmakers," WLSU Radio, La Crosse Wisconsin, on the future of computer technology. Aired May 6, 2002.

Interview on "Generation.e," CNBC Asia, on the topic, "The future capabilities of microprocessors," March 8, 2002.

INVITED PANELS at INTERNATIONAL CONFERENCES, SYMPOSIA

Chair, invited panel at 35th annual International Symposium on Computer Architecture, Beijing, June, 2008, on the topic, "Computer Architecture Research and ISCA, Have we lost our compass?"

Member, invited panel at 40th annual International Symposium on Microarchitecture, Chicago, December, 2007, on the topic, "Computing Beyond Von Neumann."

Member, invited panel at the 13th International High Performance Computer Architecture Symposium, Phoenix, February, 2007, on the topic, "Researching Novel Systems: To Instantiate, Emulate, Simulate, or Analyticate?"

Member, invited panel at the 39th International Symposium on Microarchitecture, Orlando, Florida, December, 2006, on the topic, "The Implications of Nanotechnology."

Member, invited panel at the 12th International High Performance Computer Architecture Symposium, Austin, February, 2006, on the topic, "Patenting the Fruits of Academic Research: What are the Implications?"

Moderator, invited panel at 16th Symposium on Computer Architecture and High Performance Computing, Foz do Iguacu, Brazil, October, 2004.

Member, invited panel at 2004 IEEE International Symposium on Performance Analysis of Systems and Software, Austin, March, 2004, on the topic, "The Future of Simulation: A Field of Dreams?"

Member, invited panel at the 10th International High Performance Computer Architecture Symposium, Madrid, February, 2004, on the topic, "Bridging the Research Gap between Academia and Industry."

Member, invited panel at the 8th International High Performance Computer Architecture Symposium, Boston, February, 2002, on the topic, "Processors, Memory, Interconnect, where will the greatest benefit come from in the next ten years."

Member, invited panel at the 34th International Symposium on Microarchitecture, Austin, TX, December, 2001, on the topic, "Intellectual Property: Microarchitecture is in the thick of it."

Member, invited panel at IEEE ICCD Symposium, Austin, September, 2001.

Member, invited panel at the 30th International Symposium on Microarchitecture, Raleigh, NC, December, 1997 on the topic, "The future of ISAs other than x86."

Member, invited panel at the 28th International Symposium on Microarchitecture, Ann Arbor, December 1995, on the topic, "Single-chip performance on the Microprocessor of the year 2000."

Moderator, one of two invited panels at the 21th International Symposium on Computer Architecture, Chicago, April 1994, on the topic, "Computer Architecture as a Discipline in the year 2000."

Moderator, one of two invited panels at the 20th International Symposium on Computer Architecture, San Diego, May 1993, on the topic, "Experimental Research: How do we Measure Success."

Member, one of two invited panels at the 19th International Symposium on Computer Architecture, Australia, May 1992, on the topic, "Processor architectures for Peta-op Performance."

Member, one of two invited panels at the 18th International Symposium on Computer Architecture, Toronto, May 1991, on the topic, "The Influence of University Research in Computer Architecture on the development of new commercial computers."

Member, one of two invited panels at the 17th International Symposium on Computer Architecture, Seattle, May 1990, on the topic, "Better than one operation per clock: VLIW, and Superscalar."

Member, one of two invited panels at the 13th International Symposium on Computer Architecture, Tokyo, June 1986, on the topic, "AI Machines and Scientific Machines, Are they compatible?"

EDITORSHIPS

Associate Editor, *Computer Architecture Letters*, 2006-

(Founding) Editor-in-Chief, *Computer Architecture Letters*, 2001-2005.

Member, Editorial Board, *Proceedings of the IEEE*, 1996-2000.

Associate Editor of the *IEEE Transactions on Computers*, 1992-1996.

Member, Editorial Board, *IEEE Computer*, 1989-1992.

Guest Editor of a Special Issue of *IEEE Computer* (December, 1997) on the topic, Strategic Directions for Computer Architecture Research.

Guest Editor of a Special Issue of *Proceedings of the IEEE* (December, 1995) on the topic, Microprocessors.

Guest Editor of a Special Issue of *IEEE Computer* (March, 1994) on the topic, The I/O Subsystem, A Candidate for Improvement.

Guest Editor of a Special Issue of *IEEE Computer* (January, 1991) on the topic, Experimental Research in Computer Architecture and Performance Measurement.

Guest Editor of a Special Issue of *IEEE Computer* (January, 1989) on the topic, Design and Engineering Tradeoffs in the Implementation of Various Commercially Successful Computers.

EXTERNAL EXAMINING BOARDS

External Examiner, Graduate program in Electrical Engineering and Computer Engineering, University of Cincinnati, October, 2005.

External Examiner, Computer Engineering Research, National Foundation for Science and Technology, Lisbon, Portugal, January, 2005.

External Examiner, Electrical and Computer Engineering Department, Northwestern University, May, 2001.

External Examiner, Computer Science Department, UNLV, March, 2001.

External Examiner, Texas A&M PhD program in Electrical and Computer Engineering, March, 2000.

External Examiner, Computer Engineering Research, National Foundation for Science and Technology, Lisbon, Portugal, December, 1999.

External Examiner, City University of Hong Kong, Computer Science Department, 1996-2003.

Member, Dean's External Advisory Committee, School of Electrical Engineering and Computer Science, Polytechnic University of New York, 1992-1994.

PROFESSIONAL SERVICE

Member of the Governing Board of the IEEE Computer Society, 1989-1993.

Vice President for Press Activities of the IEEE Computer Society, 1992.

General Co-Chairman, 12th International Symposium on High Performance Computer Architecture, Austin, TX, February, 2006.

General Chairman, 29th International IEEE/ACM Symposium on Computer Architecture (ISCA), Anchorage, May, 2002.

General Chairman, 34th International IEEE/ACM Workshop and Symposium on Microarchitecture, Austin, TX, November, 2001.

General Chairman, 21st International IEEE/ACM Workshop on Microarchitecture and Microprogramming, San Diego, CA, November, 1988.

General Chairman, First International Symposium on High Performance Computer Architecture, Raleigh, NC, January, 1995.

Program Co-Chairman, 15th International IEEE/ACM Symposium on Computer Architecture (ISCA), June, 1988.

Program Co-Chairman (Computer Architecture), IEEE/ACM International Conference on Supercomputing, Melbourne, July, 1998.

Member of the Advisory Committee, ACM Distinguished Lectureship Program, 1998-2003; Director, 2001-2002.

Chairman, Joint ACM-IEEE Computer Society Eckert-Mauchly Award Committee, 1992, 1999. Member of the committee, 1988-1992, 1998-2000.

Member, IEEE Computer Society Harry Goode Award Committee, 2001- , Chair, 2004-2006.

Member, IEEE Computer Society Wallace W. McDowell Award Committee, 2001- , Chair, 2004-2006.

Chairman of a Task Force appointed by the President-elect of the IEEE Computer Society to investigate problems dealing with the education of computer engineers and computer scientists, starting with high school preparation, continuing with educational programs in the Colleges, and finally dealing with continuing education beyond graduation, July, 1991.

Member of the Strategic Planning Committee of the IEEE Computer Society, 1991.

Member, IEEE Computer Society Taylor Booth Award Committee, 1993-1996.

Member, Educational Activities Board, IEEE Computer Society, 1988-1994.

Invited participant (one of 20), NSF Workshop on Grand Challenges in Computer Architecture for the Support of High Performance Computing, Purdue University, December 1991. A report of that workshop appeared as an invited paper (with 20 co-authors) in the Journal of Parallel and Distributed Computing. High Performance Architectures for Numerical and Symbolic Computations, University of California, Berkeley, February 13-15, 1985.

Member, Steering Committee of the 19th, 21st, 22nd, 23rd, 24th, 25th, 26th, 28th, 29th, 30th and 31st, 33rd, 35th and 36th International Symposia on Computer Architecture, May, 1989, April, 1994, June, 1995, May, 1996, June, 1997, June, 1998, May, 1999, May, 2001, May, 2002, June, 2003, June, 2004, June, 2006, June, 2008, and June, 2009.

Member, Steering Committee of the 25th, 26th, 27th, 28th, 29th, 30th, 31st, 32nd, 33rd, 34th, 35th, 36th, 37th, 38th, 39th, 40th, and 41st International Symposium on Microarchitecture, December, 1992, December, 1993, December, 1994, December, 1995, December, 1996, December, 1997, December, 1998, November, 1999, December, 2000, December, 2001, November, 2002, December, 2003, December, 2004, November, 2005, December, 2006, December, 2007, November, 2008.

Member, Steering Committee of the 2nd, 3rd, 4th, 5th, 6th, 7th, 8th, 9th, 10th, 11th, 12th, 13th, 14th, and 15th IEEE International Symposium on High Performance Computer Architecture, San Jose, February, 1996, San Antonio, February, 1997, San Francisco, February, 1998, Orlando, January, 1999, Toulouse, January, 2000, Monterrey, Mexico, January, 2001, Boston, January, 2002, Anaheim, January, 2003, Madrid, February, 2004, San Francisco, February, 2005, Austin, February, 2006, Phoenix, February, 2007, Salt Lake City, February 2008, February 2009.

Member, Technical Advisory Board, IEEE Technical Committee on Computer Architecture, 1995-present.

Organizer/co-ordinator, minitrack on the subject: "Real Machines: Design Choices, Engineering Trade-offs," at the 20th Hawaii International Conference on Systems Science, January, 1989.

Organizer/co-ordinator, minitrack on the subject: "Experimental Research in Computer Architecture," at the 21st Hawaii International Conference on Systems Science, January, 1990.

Organizer/co-ordinator, second consecutive minitrack on the subject: "Experimental Research in Computer Architecture," at the 22nd Hawaii International Conference on Systems Science, January, 1991.

Organizer/co-ordinator, minitrack on the subject: "I/O Architecture: Issues and Bottlenecks," at the 23rd Hawaii International Conference on Systems Science, January, 1992.

Organizer/co-ordinator, second consecutive minitrack on the subject: "I/O Architecture: Issues and Bottlenecks," at the 24th Hawaii International Conference on Systems Science, January, 1993.

Lecturer, IEEE Computer Society's Tutorial Program on the subject, "Computer Architecture Choices."

Lecturer, IEEE Computer Society's one-day tutorial for High School Math and Science teachers, 1991-94.

External reviewer, Research Programs Review at the Lawrence Livermore National Laboratory, December, 1984.

Member, organizing committee for the First Northern California Universities Supercomputer Workshop, Lawrence Livermore National Laboratory, February, 1984.

Member, Program Committee for more than 50 conferences and symposia, including most recently the 31th International Workshop on Microarchitecture and Microprogramming (Dallas, December 1998), the 1998 3rd International conference on Parallel Architectures and Compiling Techniques (Paris, October, 1998), the 5th International High Performance Computer Architecture Conference (Orlando, January, 1999), 32th International Symposium on Microarchitecture (Haifa, November, 1999), HPCA-7 (Monterrey, January, 2001), ISCA-2001 (Goteborg, June,

2001), 8th International Conference on High Performance Computing (Hyderabad, December, 2001), and ICS (New York City, June, 2002), ISCA-2004 (Munich, June 2004), Micro-37 (San Francisco, Dec 2004), HiPEAC (Barcelona, Nov 2005), Micro-38 (Barcelona, Nov 2005), ISCA (Boston, 2006), Micro-39 (Orlando, 2006), HPCA-13 (Phoenix, 2007), Micro-40 (Chicago, 2007), HPCA-14 (Salt Lake City, 2008), ISCA (Beijing, 2008), SBAC-PAD (Brazil, 2008), Micro-41 (Como, 2008), HPCA-15 (Raleigh, 2009)

Reviewer, NSF proposals, ACM and IEEE journals and conferences.

Accreditation visitor, ABET (computer engineering) 1990-1994.

Accreditation visitor, CSAB (computer science), 1986-1992.

Chairman, Curriculum Assistance Committee of the IEEE Computer Society, 1978-1981. In this capacity I organized and conducted workshops dealing with the Model Curriculum in Computer science and Engineering in 1979 (San Francisco), 1980 (Chicago) and 1981 (Washington, D.C.).

General Chairman, 5th Annual Southeastern Symposium on System Theory, Co-hosted by N.C. State, UNC-Chapel Hill, Duke, March, 1973.

Member, Steering Committee, COINS-3, 1969.

Program Chairman, 1975 Southeastern Regional ACM Meeting, April, 1975.

Session Chairman, more than 50 conferences, including: COINS-3 (January, 1969), Hawaii International Conference on Systems Sciences (January, 1970), 6th Annual Southeastern Systems Theory Symposium (1974), 4th International Multi-valued Logic Symposium (1974), 7th Annual Southeastern Systems Theory Symposium (1975), Fall Compcon (September, 1981), Spring Compcon (February, 1983), Spring Compcon (February, 1984), Micro-17 (October, 1984), Spring Compcon (February, 1985), Micro-18 (December, 1985), HICSS-19 (January, 1986), Spring Compcon (March, 1986), 13th ICAC (June, 1986), Micro-19 (October, 1986), Micro-20 (December, 1987), Compcon 88 (March, 1988), Micro-21 (December, 1988), Compcon 89 (February, 1989), International Supercomputing Conference (June, 1989), HICSS-1991 (January, 1991), Micro-24 (November, 1991), ISCA-13 (June, 1986), HICSS-1992 (January, 1992), ISCA-19 (May, 1992), Micro-25 (November, 1992), IFIP Workshop on Architecture and Compiling (January, 1993), HICSS-1993 (January, 1993), Micro-26 (December, 1993), IPPS (April, 1994), Micro-27 (December, 1994), HPCA-1 (January, 1995), ISCA (June, 1995), PACT (June, 1995), Micro-28 (December, 1995), ICS (July, 1997), Micro-30 (December, 1997), HPCA-5 (January, 1999), PACT (October, 1999), ISCA (June, 2004), ISCA (June, 2006), HPCA (February, 2008).

TUTORIALS (Sponsored by the professional computer societies, IEEE_CS and ACM)

Instructor, one day tutorial on current hot topics in Computer Architecture, as follows: IEEE Tutorial Week West, October 1, 1984, IEEE Tutorial Week West, June 7, 1985, IEEE Compcon 86, March 1, 1986, Compcon 88, February 29, 1988, Compcon 89, February 27, 1989, Compcon 90, February 26, 1990, Compcon 91, February 25, 1991, Compcon 92, February 24, 1992, Compcon 93, February 22, 1993, Compcon 94, February 28, 1994, Compcon 95, March 5, 1995, Supercomputing 95, December 4, 1995, Compcon 96, February 25, 1996, Compcon 97, February 23, 1997, Supercomputing 2001, November 11, 2001.

Instructor, half-day tutorial on architectural mechanisms for exploiting concurrency, as follows: 17th IEEE/ACM International Symposium on Computer Architecture, May 28, 1990, 18th IEEE/ACM International Symposium on Computer Architecture, May 27, 1991, 19th IEEE/ACM International Symposium on Computer Architecture, May 17, 1992, International Conference on Parallel Processing, August 17, 1992, 21st IEEE/ACM International Symposium on Computer Architecture, April 19, 1994, 1994 International Conference on Parallel Architectures and Compiler Technology, August 23, 1994, 22nd IEEE/ACM International Symposium on Computer Architecture, June 21, 1995, the 1995 International Conference on Parallel Architectures and Compiler Techniques, June 27, 1995, the 23rd IEEE/ACM International Symposium on Computer Architecture, May 21, 1996, IEEE Hot Chips Symposium, August 18, 1996, and ICCD, October 7, 1996.

Instructor, one-day tutorial to non-Computer-Architects on the state-of-the-art in Computer Architecture, as follows: 26th Annual HICSS Conference, January 5, 1993, 27th Annual HICSS Conference, January 4, 1994, 28th Annual HICSS Conference, January 3, 1995, 29th Annual HICSS Conference, January 2, 1996.

Instructor, one-day tutorial on Microarchitecture: Concepts, Tradeoffs, the Future, PACT 2007, Brasov, Romania, September, 2007.

BOOKS

Introduction to Computing Systems: from bits and gates to C and beyond, McGraw-Hill, 2001 (ISBN No. 0-07-237690-2), co-authored with Professor Sanjay Jeram Patel. 2nd edition, McGraw-Hill, 2004 (ISBN No. 0-07-246750-9, ISBN 0-07-121503-4(ISE)).

MAGAZINE/NEWSLETTER ARTICLES

Adaptive Insertion Policies for High-Performance Caching. *IEEE Micro*, Top Picks Special Issue, January/February, 2008. [earlier version in *Proceedings, 34th annual IEEE/ACM International Symposium on Computer Architecture*, San Diego, CA, June 2008 (with Moinuddin K. Qureshi, Amer Jaleel, Simon C. Steely Jr., and Joel Emer).

Diverge-Merge Processor: Generalized and Energy-Efficient Dynamic Predication, *IEEE Micro*, Top Picks Special Issue, January/February, 2007. [earlier version in *Proceedings, 39th annual IEEE/ACM International Symposium on Microarchitecture*, Orlando, Florida, December, 2006] (with Hyesoon Kim, Jose Joao, and Onur Mutlu)..XP Techniques for Efficient Processing in Runahead Execution Engines. *IEEE Micro*, Top Picks Special Issue, January/February, 2006. [earlier version in *Proceedings, 32nd annual IEEE/ACM International Symposium on Computer Architecture*, Madison, Wisconsin, June, 2005] (with Onur Mutlu and Hyesoon Kim).

Wish Branches: Combining Conditional Branching and Predication for Adaptive Predicated Execution, *IEEE Micro*, Top Picks Special Issue, January/February, 2006. [earlier version in *Proceedings, 38th annual IEEE/ACM International Symposium on Microarchitecture*, Barcelona, November, 2005] (with Hyesoon Kim, Onur Mutlu, and Jared Stark).

Runahead Execution: An Effective Alternative to Large Instruction Windows, *IEEE Micro*, Top Picks Special Issue, November/December, 2003. [earlier version in *Proceedings, 9th annual IEEE High Performance Computer Architecture Symposium*. Anaheim, CA, February, 2003] (with Onur Mutlu, Jared Stark, and Chris Wilkerson).

"New Requirements, Bottlenecks, and Good Fortune, Agents of Evolution of the Microprocessor," *Proceedings of the IEEE*, November, 2001.

"The First Computing Course for CS, CE, and EE Majors at Michigan," *The Interface* (a Newsletter published jointly by ASEE and the IEEE Education Society), November 1998, pp. 1-3.

"Identifying Obstacles in the Path to *More*," *IEEE Computer*, December 1997, Vol. 30, No. 12, p. 32.

"One billion transistors, one uniprocessor, one chip," *IEEE Computer*, September, 1997.

"First, Let's Get the Uniprocessor Right," *Microprocessor Report*, (Invited article for 25th Anniversary of the Microprocessor Special Issue), August 5, 1996, pp. 23-24.

"The Microprocessor for Scientific Computing in the Year 2000," *IEEE Computational Science & Engineering*, Summer 1996, pp. 42-43.

"Education in Computer Science and Computer Engineering Starts with Computer Architecture," *Computer Architecture Technical Committee Newsletter*, June 1996.

"Scanning the Special Issue on Microprocessors," *Proceedings of the IEEE*, December 1995, Vol. 83, No. 12.

"The I/O Subsystem - A Candidate for Improvement," *IEEE Computer*, March 1994, Vol. 27, No. 3, pp. 15-16.

"Disk Arrays: High-Performance, High-Reliability Storage Subsystems," *IEEE Computer*, March 1994, Vol. 27, No. 3, pp. 30-36.

"Experimental Research in Computer Architecture," *IEEE Computer*, January 1991, Vol. 24, No. 1, pp. 14-16.

"Real Machines: Design Choices/Engineering Trade-Offs," *IEEE Computer*, January 1989, Vol. 22, No. 1, pp. 8-10.

RESEARCH PUBLICATIONS

Archival Journals:

- Virtual Program Counter (VPC) Prediction: Very Low-Cost Indirect Branch Prediction using Conditional Branch Prediction Hardware, *IEEE Transactions on Computers*, accepted for publication, September 2008 (with Hyesoon Kim, Jose Joao, Onur Mutlu, Chang Joo Lee, and Robert Cohn).
- Dynamic Predication of Indirect Jumps, *IEEE Computer Architecture Letters*, Vol. 7, June, 2008 (with Jose A. Joao, Onur Mutlu, and Hyesoon Kim).
- Address-Value Delta (AVD) Prediction: A Hardware Technique for Efficiently Parallelizing Dependent Cache Misses, *IEEE Transactions on Computers*, vol. 55, no. 12, December, 2006, (with Onur Mutlu and Hyesoon Kim).
- An Analysis of the Performance Impact of Wrong-Path Memory References on Out-of-Order and Runahead Execution Processors, *IEEE Transactions on Computers*, vol. 54, no. 12, December, 2005, (with Onur Mutlu, Hyesoon Kim, and David Armstrong).
- Using the First-Level Caches as Filters to Reduce the Pollution Caused by Speculative Memory References, *International Journal of Parallel Programming*, 2005, (with Onur Mutlu, Hyesoon Kim, and David N. Armstrong).
- On Reusing the Results of Pre-Executed Instructions in a Runahead Execution Processor, *Computer Architecture Letters*, vol 4, no. 1, Jan. 2005 (with O. Mutlu, H. Kim, and J. Stark).
- Soft Updates: A Solution to the Metadata Update Problem in File Systems, *ACM Transactions on Computer Systems*, vol. 18, no. 2, May 2000, pp 127-153 (with Greg Ganger, Marshall Kirk McKusick, and Craig A.N. Soules).
- Evaluation of Design Options for the Trace Cache Fetch Mechanism, *IEEE Transactions on Computers*, February, 1999, (with Sanjay Patel and Daniel Friendly).
- Increasing the Instruction Fetch Rate via Block-structured Instruction Set Architectures, *International Journal of Parallel Programming*, vol.26, no.4, August, 1998 (with E. Hao, P-Y Chang, M. Evers).
- Using System Level Models to Evaluate I/O Subsystem Designs, *IEEE Transactions on Computers*, vol 47, no. 6 (June, 1998) (with Gregory Ganger).
- Improving Branch Prediction Accuracy by Reducing Pattern History Table Interference, *International Journal of Parallel Programming*, 1997, vol 25, num 5 (with P-Y Chang and Marius Evers).
- The Effects of Mispredicted-Path Execution on Branch Prediction Structures, *International Journal of Parallel Programming*, 1997, vol 25, num 5, pp. 363-384 (with Stephan Jourdan, Tse-Hao Hsing and Jared Stark).
- Using Predicated Execution to Improve the Performance of a Dynamically Scheduled Machine with Speculative Execution, *International Journal of Parallel Programming*, vol.24, 1996 (with P-Y Chang, E. Hao, and P. Chang).
- Branch Classification: A New Mechanism for Improving Branch Predictor Performance, *International Journal of Parallel Programming*, vol.24, 1996 (with Po-Yung Chang, Eric Hao, and Tse-Yu Yeh).
- Enhancing Instruction Scheduling With a Block-Structured ISA, *International Journal of Parallel Programming*, vol. 23, no. 3, 1995 (with Stephen Melvin).
- Report of the Purdue Workshop on Grand Challenges in Computer Architecture for the Support of High Performance Computing, *Journal of Parallel and Distributed Computing*, vol.16, pp. 199-211, 1992 (with 19 co-authors).
- An Experimental Single-Chip Data Flow CPU, *IEEE Journal of Solid State Circuits*, January, 1992 (with G.Uvieghara, W. Hwu, Y. Nakagome, D. Jeong, D. Lee, D. Hodges).
- Alternative Implementations of Prolog, the Microarchitecture Perspective, *IEEE Transactions on Systems, Man, and Cybernetics*, vol. 19, no. 4, pp. 693-698, July/August, 1989.
- Checkpoint Repair for High Performance Out-of-Order Execution Machines, *IEEE Transactions on Computers*, December, 1987, (with Wen-mei Hwu).

- Retrofitting the VAX-11/780 Microarchitecture for IEEE Floating Point Arithmetic - Implementation Issues, Measurements, and Analysis, *IEEE Transactions on Computers* v. c-34, no. 8, August, 1985 (with David Aspinwall).
- Independent necessary conditions for functional completeness in m-valued logic, *Notre Dame Journal of Formal Logic*, v. 18, no. 2, April, 1977.
- Some clarifications of the concept of a Garden of Eden configuration, *Journal of Computer and System Sciences*, v. 10, no. 1, February, 1975 (with S. Amoroso and G. Cooper).
- Optimal and near optimal universal logic modules with interconnected external terminals, *IEEE Transactions on Computers*, October, 1973.
- Minimum search tree structures for data partitioned into pages, *IEEE Transactions on Computers*, September, 1972.
- Decision procedures for surjectivity and injectivity of parallel maps for tessellation structures, *Journal of Computer and Systems Sciences*, October, 1972 (with S. Amoroso).
- Variable length file structures having minimum average search time, *Communications of the ACM*, v. 12, no. 2, February, 1969.

Refereed Conferences and Symposia:

- Flexible Reference Counting-Based Hardware Acceleration for Garbage Collection, *Proceedings, 36th International Symposium on Computer Architecture*, Austin, Texas, June 2009, (with Jose Joao and Onur Mutlu).
- An Asymmetric Multi-core Architecture for Accelerating Critical Sections, *Proceedings of ASPLOS XIV*, Washington D.C., March 2009 (with M. Aater Suleman, Onur Mutlu, and Moinuddin Qureshi).
- Techniques for Bandwidth-Efficient Prefetching of Linked Data Structures in Hybrid Prefetching Systems, *Proceedings of the 15th Annual IEEE High Performance Computer Architecture Symposium (HPCA-15)*, Raleigh, NC, February, 2009. (with Eiman Ibrahim and Onur Mutlu).
- Prefetch-Aware DRAM Controller, *Proceedings, 41st annual IEEE/ACM International Symposium on Microarchitecture*, Como, Italy, November, 2008 (with Chang Joo Lee, Onur Mutlu, and Veynu Narasiman).
- Achieving Out-of-Order Performance with Almost In-Order Complexity, *Proceedings, 35th International Symposium on Computer Architecture*, Beijing, China, June 2008, (with Francis Tseng).
- Feedback-Driven Threading: Power-Efficient and High-Performance Execution of Multi-threaded Workloads on CMP, *Proceedings of ASPLOS XIII*, Seattle, March 2008 (with M. Aater Suleman and Moinuddin Qureshi).
- Improving the Performance of Object-Oriented Languages with Dynamic Predication of Indirect Jumps, *Proceedings of ASPLOS XIII*, Seattle, March 2008 (with Jose A. Joao, Onur Mutlu, and Hyesoon Kim).
- A Performance-aware Speculation Control Technique using Wrong Path Usefulness Prediction, *Proceedings of the 14th Annual IEEE High Performance Computer Architecture Symposium (HPCA-14)*, Salt Lake City, February 2008 (with Chang Joo Lee, Hyesoon Kim, and Onur Mutlu).
- Adaptive Insertion Policies for High Performance Caching, *Proceedings, 34th International Symposium on Computer Architecture*, San Diego, CA, June 2007 (with Moinuddin Qureshi, Aamer Jaleel, Simon Steely, Jr. and Joel Emer).
- VPC Prediction: Reducing the Cost of Indirect Branches via Hardware-Based Dynamic Devirtualization, *Proceedings, 34th International Symposium on Computer Architecture*, San Diego, CA, June 2007 (with Hyesoon Kim, Jose Joao, and Onur Mutlu).
- Profiling-assisted Compiler Support for Dynamic Predication in Diverge-Merge Processors, *5th International Symposium on Code Generation and Optimization (CGO-5)*, San Jose, March 2007 (with Hyesoon Kim, Jose Joao, and Onur Mutlu).
- Line Distillation: Increasing Cache Capacity by Filtering Unused Words in Cache Lines, *Proceedings of the 13th Annual IEEE High Performance Computer Architecture Symposium (HPCA-13)*, Phoenix, February, 2007 (with Moinuddin Qureshi and Muhammed Aater Suleman).

- Feedback Directed Prefetching: Improving the Performance and Bandwidth-Efficiency of Hardware Prefetchers, *Proceedings of the 13th Annual IEEE High Performance Computer Architecture Symposium (HPCA-13)*, Phoenix, February, 2007 (with Santhosh Srinath, Onur Mutlu, and Hyesoon Kim).
- Diverge-Merge Processor(DMP):Dynamic Predicated Execution of Complex Control-Flow Graphs Based on Frequently Executed Paths *Proceedings, 39th annual IEEE/ACM International Symposium on Microarchitecture*, Orlando, December, 2006 (with Hyesoon Kim, Jose A. Joao, and Onur Mutlu).
- Utility-Based Cache Partitioning: A Low-Overhead, High-Performance, Runtime Mechanism to Partition Shared Caches, *Proceedings, 39th annual IEEE/ACM International Symposium on Microarchitecture*, Orlando, December, 2006 (with Moinuddin Qureshi).
- A Case for MLP-Aware Cache Replacement, *Proceedings, 33rd International Symposium on Computer Architecture*, Boston, June, 2006 (with Moinuddin Qureshi, Daniel Lynch, and Onur Mutlu).
- 2D-Profiling: Detecting Input-Dependent Branches with a Single Input Data Set, *4th International Symposium on Code Generation and Optimization (CGO-4)*, New York City, March, 2006 (with Hyesoon Kim, Mohammed Aater Suleman, and Onur Mutlu).
- Wish Branches: Combining Conditional Branching and Predication for Adaptive Predicated Execution, *Proceedings, 38th annual IEEE/ACM International Symposium on Microarchitecture*, Barcelona, November, 2005 (with Hyesoon Kim, Onur Mutlu, and Jared Stark).
- Address-Value Delta (AVD) Prediction: Increasing the Effectiveness of Runahead Execution by Exploiting Regular Memory Allocation Patterns, *Proceedings, 38th annual IEEE/ACM International Symposium on Microarchitecture*, Barcelona, November, 2005 (with Onur Mutlu and Hyesoon Kim).
- The V-Way Cache: Demand Based Associativity via Global Replacement, *Proceedings, 32nd International Symposium on Computer Architecture*, Madison, Wisconsin, June, 2005 (with Moinuddin Qureshi and David Thompson).
- Techniques for Efficient Processing in Runahead Execution Engines. *Proceedings, 32nd International Symposium on Computer Architecture*, Madison, Wisconsin, June, 2005 (with Onur Mutlu and Hyesoon Kim).
- Microarchitecture-Based-Introspection: A Technique for Transient-Fault= Tolerance in Microprocessors, *The IEEE International Conference on Dependable Systems and Networks (DSN 2005)*, Yokohama, Japan, June 2005 (with Moinuddin Qureshi and Onur Mutlu).
- Early Detection of Branch Mispredictions using Wrong Path Execution Information, *Proceedings, 37th annual IEEE/ACM International Symposium on Microarchitecture*, Portland, OR, December, 2004 (with Onur Mutlu, Hyesoon Kim, and David Armstrong).
- Cache Filtering Techniques to Reduce the Negative Impact of Useless Speculative Memory References on Processor Performance, *Proceedings of the 16th Symposium on Computer Architecture and High Performance Computing*, Foz do Iguacu, Brazil, October, 2004, (with Onur Mutlu, Hyesoon Kim, and David Armstrong).
- Partitioned First-level Cache design for Clustered Microarchitectures, *Proceedings, 17th annual ACM International Conference on Supercomputing*, San Francisco, June, 2003 (with P. Racunas).
- Runahead Execution: An Alternative to Very Large Instruction Windows for Out-of-order Processors, *Proceedings, 9th Annual IEEE International Symposium on High Performance Computer Architecture*, Anaheim, CA, February, 2003 (with Onur Mutlu, Jared Stark, Chris Wilkerson).
- Microarchitectural Support for Precomputation Microthreads, *Proceedings of the 35th International Symposium on Microarchitecture*, Istanbul, November, 2002 (with R. Chappell, F. Tseng, and A. Yoav).
- Handling of Packet Dependencies: A Critical Issue for Highly Parallel Network Processors, *Proceedings of the International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES 2002)*, Grenoble, France, October, 2002 (with S. Melvin).
- Difficult-Path Branch Prediction Using Subordinate Microthreads, *Proceedings, 29th International Symposium on Computer Architecture*, Anchorage, May, 2002 (with R. Chappell).
- Pipelined and Redundant Binary Adders for Modern Processors, *Proceedings, 8th Annual IEEE International Symposium on High Performance Computer Architecture*, Boston, MA, February, 2002 (with M. Brown).

- Select-Free Instruction Scheduling Logic, *Proceedings, 34th International Symposium on Microarchitecture*, Austin, TX, December, 2001 (with M. Brown and J. Stark).
- On Pipelining Dynamic Instruction Scheduling Logic, *Proceedings, 33rd International Symposium on Microarchitecture*, Monterey, CA, December, 2000 (with J. Stark and M. Brown).
- Simultaneous Subordinate Microthreading (SSMT), *Proceedings, 26th International Symposium on Computer Architecture*, Atlanta, GA, May, 1999 (with R. Chappell, J. Stark, S.W.P. Kim, and S. Reinhardt).
- Putting the Fill Unit to Work: Dynamic Optimizations for Trace Cache Microprocessors, *Proceedings, 31st International Symposium on Microarchitecture*, Dallas, TX, November, 1998 (with Daniel Friendly and Sanjay Patel).
- Variable Length Path Branch Prediction, *Proceedings, ASPLOS VIII*, San Jose, CA, October, 1998 (with Jared Stark and Marius Evers).
- An analysis of correlation and predictability: What makes two-level branch predictors work, *Proceedings, 25th International Symposium on Computer Architecture*, Barcelona, June, 1998 (with Marius Evers, Sanjay J Patel, and Robert S Chappell).
- Improving Trace Cache Effectiveness with Branch Promotion and Trace Packing, *Proceedings, 25th International Symposium on Computer Architecture*, Barcelona, June, 1998 (with Sanjay J Patel and Marius Evers).
- Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism, *Proceedings, 30th International Symposium on Microarchitecture*, Raleigh, NC, December, 1997 (with Daniel Friendly and Sanjay Patel).
- Reducing the Performance Impact of Instruction Cache Misses by Writing Instructions into the Reservation Stations Out-of-order, *Proceedings, 30th International Symposium on Microarchitecture*, Raleigh, NC, December, 1997 (with Jared Stark and Paul Racunas).
- Using Non-Volatile Storage to Improve the Reliability of RAID5 Disk Arrays, *Proceedings, International Symposium on Fault Tolerant Computer Systems*, Seattle, June, 1997 (with Robert Hou).
- Target Prediction for Indirect Jumps, *Proceedings of the 24th International Symposium on Computer Architecture*, Denver, June 1997 (with P-Y. Chang).
- The Agree Predictor: A Mechanism for Reducing Negative Branch History Interference, *Proceedings of the 24th International Symposium on Computer Architecture*, Denver, June 1997 (R. Chappell, E. Sprangle, and M. Alsup).
- Increasing the Instruction Fetch Rate via Block-Structured Instruction Set Architectures, *Proceedings, 29th International Symposium on Microarchitecture*, Paris, France, December, 1996 (with Eric Hao, Po-Yung Chang, and Marius Evers).
- Improving Branch Prediction Accuracy by Reducing Pattern History Table Interference, *Proceedings, International Conference on Parallel Architectures and Compilation Techniques*, Boston, October 1996 (with P-Y Chang and M. Evers)
- The Effects of Mispredicted-Path Execution on Branch Prediction Structures, *Proceedings, International Conference on Parallel Architectures and Compilation Techniques*, Boston, October 1996 (with S Jourdan, T-H Hsing and J Stark).
- Using Hybrid Branch Predictors to Improve Branch Prediction Accuracy in the Presence of Context Switches, *Proceedings of the 23rd International Symposium on Computer Architecture*, Philadelphia, May, 1996 (with Marius Evers, Po-Yung Chang, and Tse-Yu Yeh).
- Alternative Implementations of Hybrid Branch Predictors, *Proceedings of the 28th International Symposium on Microarchitecture*, Ann Arbor, Michigan, November, 1995 (with Po-Yung Chang and Eric Hao).
- Track Piggybacking: An Improved Rebuild Algorithm for RAID's Disk Arrays, *Proceedings of International Conference on Parallel Processing*, August, 1995 (with Robert Hou).
- Using Predicated Execution to Improve the Performance of a Dynamically Scheduled Machine with Speculative Execution, *Proceedings, International Conference on Parallel Architectures and Compilation Techniques*, Limassol, Cyprus, June 1995 (with P-Y Chang, E. Hao, and P. Chang).
- On-Line Extraction of SCSI Disk Drive Parameters *Proceedings of the 1995 ACM SIGMETRICS Conference*, May, 1995 (with Gregory Ganger, Bruce Worthington, and John Wilkes).

- Branch Classification: A New Mechanism for Improving Branch Predictor Performance, *Proceedings of the 27th International Symposium on Microarchitecture*, San Jose, California, November, 1994 (with Po-Yung Chang, Eric Hao, and Tse-Yu Yeh).
- Facilitating Superscalar Processing via a Combined Static/Dynamic Register Renaming Scheme, *Proceedings of the 27th International Symposium on Microarchitecture*, San Jose, California, November, 1994 (with Eric Sprangle).
- The Effect of Speculatively Updating Branch History on Branch Prediction Accuracy, Revisited, *Proceedings of the 27th International Symposium on Microarchitecture*, San Jose, California, November, 1994 (with Eric Hao).
- Metadata Update Performance in File Systems, *Proceedings of the First Operating Systems Design and Implementation Symposium*, Monterey, November 1994 (with Gregory Ganger).
- Scheduling Algorithms for Modern Disk Drives *Proceedings of the 1994 ACM SIGMETRICS Conference*, Nashville, TN, May, 1994 (with Gregory Ganger and Bruce Worthington).
- Branch History Table Indexing to Prevent Pipeline Bubbles in Wide-Issue Superscalar Processors, *Proceedings of the 26th International Symposium and workshop on Microarchitecture*, Austin, TX, December 1993 (with Tse-Yu Yeh).
- A Comparative Performance Evaluation of Various State maintenance Mechanisms, *Proceedings of the 26th International Symposium and workshop on Microarchitecture*, Austin, TX, December 1993 (with Michael Butler).
- Trading Disk Capacity for Performance *Proceedings of the 2nd International Symposium on High Performance Distributed Computing*, Spokane, WA, July, 1993 (with Robert Hou)
- Increasing Instruction Fetch Rate via Multiple Branch Prediction and a Branch Address Cache. *Proceedings of the 7th ACM International Conference on Supercomputing*. Tokyo, Japan, July, 1993. (with Tse-Yu Yeh and Deborah Marr)
- A Comparison of Dynamic Branch Predictors that use Two Levels of Branch History. *Proceedings, 20th International Symposium on Computer Architecture*, San Diego, CA, May, 1993. (with Tse-Yu Yeh)
- The Process Flow Model: Examining I/O Performance from the System's Point of View, *Proceedings of the 1993 ACM SIGMETRICS Conference*, Santa Clara, CA, May, 1993 (with Gregory Ganger)
- Comparing Rebuild Algorithms for Mirrored and RAID5 Disk Arrays *Proceedings, SigMOD Conference '93* Washington, DC, May, 1993 (with Robert Hou)
- Disk Subsystem Load Balancing: Disk Striping vs. Conventional Data Placement *Proceedings, 26th Hawaii International Conference on Systems Sciences* Maui, January, 1993. (with Gregory R. Ganger, Bruce L. Worthington, and Robert Y. Hou)
- Balancing I/O Response Time and Disk Rebuild Time in a RAID 5 Disk Array *Proceedings, 26th Hawaii International Conference on Systems Sciences* Maui, January, 1993. (with Robert Y. Hou and Jai Menon)
- An Investigation of the Performance of Various Dynamic Scheduling Techniques, *Proceedings, 25th International Symposium and workshop on Microarchitecture*, Portland OR, November, 1992. (with Michael Butler)
- A Comprehensive Instruction Fetch Mechanism for a Processor Supporting Speculative Execution, *Proceedings, 25th International Symposium and workshop on Microarchitecture*, Portland OR, November, 1992. (with Tse-Yu Yeh)
- Alternative Implementations of Two-Level Adaptive Training Branch Prediction, *Proceedings, 19th International Symposium on Computer Architecture*, Queensland, Australia, May, 1992. (with Tse-Yu Yeh)
- Toward the Specification of an ISA for High Performance Computing Engines -- Part I: The Hardware Perspective. *Proceedings, 25th Hawaii International Conference on Systems Sciences* Kauai, January, 1992. (with Michael Butler and David Dyer)
- Issues and Problems in the I/O Subsystem, Part I -- The Magnetic Disk, *Proceedings, 25th Hawaii International Conference on Systems Sciences* Kauai, January, 1992. (with Robert Hou, Gregory Ganger and Charles Gimarc)
- Two-Level Adaptive Branch Prediction, *Proceedings, 24th International Symposium and workshop on Microarchitecture*, Albuquerque, November, 1991. (with Tse-Yu Yeh)

- The Effect of Real Data Cache Behavior on the Performance of a Microarchitecture that Supports Dynamic Scheduling, *Proceedings, 24th International Symposium and workshop on Microarchitecture*, Albuquerque, November, 1991. (with Michael Butler)
- Single Instruction Stream Parallelism is Greater than Two, *Proceedings of the 18th International Symposium on Computer Architecture*, May, 1991, (with M. Butler, T-Y Yeh, M. Alsup, H. Scales, and M. Shebanow).
- Exploiting Fine-Grained Parallelism through Combined Hardware and Software Techniques, *Proceedings of the 18th International Symposium on Computer Architecture*, May, 1991, (with Stephen Melvin).
- An Area-efficient Register Alias Table for Implementing HPS, *Proceedings of the International Conference on Parallel Processing*, August, 1990, (with Michael Butler).
- An Experimental Single-Chip Data Flow CPU *Proceedings of the 1990 Symposium on VLSI Circuits* Honolulu, June, 1990 (with G. Uvieghara, W. Hwu, et.al.).
- Methodologies for Experimental Research in Computer Architecture and Performance Measurement, *Proceedings of the 23rd Annual Hawaii International Conference on System Sciences*, Kona, HI, January, 1990.
- Unification Parallelism: How much can we exploit, *Proceedings of the North American Conference on Logic Programming*, Cleveland, OH, October, 1989 (with A. Singhal).
- Alternative Microarchitecture Structures for Implementing the VAX Architecture, *Proceedings of the 22nd International Workshop on Microarchitecture and Microprogramming*, Dublin, August, 1989.
- Performance Benefits of Large Execution Atomic Units in Dynamically Scheduled Machines, *Proceedings of the 3rd International Conference on Supercomputing*, Crete, June, 1989 (with S. Melvin).
- A High Performance Prolog Processor with Multiple Function Units, *Proceedings of the 16th International Symposium on Computer Architecture*, Jerusalem, May, 1989 (with A. Singhal).
- Tailoring Functional Units and Memory in a High Performance Prolog Architecture, *Proceedings of the 22nd Hawaii International Conference on Systems Sciences*, January, 1989 (with A. Singhal).
- Extending a Prolog Architecture for High Performance Numeric Computations, *Proceedings of the 22nd Hawaii International Conference on Systems Sciences*, January, 1989 (with R. Yung and A. Despain).
- An Extended Prolog Architecture for Integrated Symbolic and Numeric Execution, *Proceedings of the International Computer Science Conference*, December 1988 (with Robert Yung, Alvin M. Despain).
- Implementing a Prolog Machine with Multiple Functional Units, *Proceedings of the 21st Workshop on Microarchitecture and Microprogramming*, November, 1988 (with A. Singhal).
- Hardware Support for Large Atomic Units in Dynamically Scheduled Machines, *Proceedings of the 21st Workshop on Microarchitecture and Microprogramming*, November, 1988 (with S. Melvin and M. Shebanow).
- Hierarchical Registers for Scientific Computers, *Proceedings of the ACM International Conference on Supercomputing*, Saint Malo, France, July, 1988 (with J. Swensen).
- The Use of Microcode Instrumentation for Development, Debugging, and Tuning of Operating System Kernels, *Proceedings of the 1988 ACM SIGMETRICS Conference*, Santa Fe, NM, May, 1988 (with S. Melvin).
- HPSm2: A Refined Single Chip Microengine, *Proceedings of the 21st Annual Hawaii International Conference on Systems Sciences*, Kona, HI, January, 1988 (with W.Hwu).
- The DSI and Below: The Architecture/Hardware Component of a Computer Science Curriculum, *Proceedings of the 21st Annual Hawaii International Conference on Systems Sciences*, Kona, HI, January, 1988.
- SPAM: A Microcode-Based Tool for Tracing Operating System Performance, *Proceedings, 20th Annual Workshop on Microprogramming*, Colorado Springs, CO, December, 1987 (with S. Melvin).
- Exploiting Horizontal and Vertical Concurrency via the HPSm Microprocessor, *Proceedings, 20th Annual Workshop on Microprogramming*, Colorado Springs, CO, December, 1987 (with W. Hwu).
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