Errata for *Fundamentals of Logic Design, 5th ed, hardcover (1st printing)*

Look on the back of the title page of the textbook (the copyright page) and you will find a line that reads either 3 4 5 6 7 06 05 04 or 2 3 4 5 6 7 06 05 04 03 or 1 2 3 4 5 6 7 06 05 04 03. If the line begins with 1, you have the first printing of the text, and you should use this errata list. Note that the list is divided into two parts. Be sure to check both parts of the list before reporting any errors.

**Reward:** Dr. Roth (ENS 510) will pay a $5 reward to the first person who finds any additional technical error in the text. He will pay a $2 reward to the first person who finds any additional minor error (spelling, grammar, etc.). Please verify your error with a T.A. and then send it to roth@ece.utexas.edu.

"s.b." means "should be"

- p. 20, line –6: 1011 s.b. 1010
- p. 28, part (e), last column of table: \( C(A + B)' \) s.b. \( C(A + B') \)
- p. 43, Eq. (2-15): \( AC'E' \) s.b. \( AC'E' \)
- p. 49, Prob. 2.10: \( = X + Y' \) s.b. \( = X \)
- p. 58, line 2: \( (3-32) \) s.b. \( (3-33) \)
- p. 60, line –4: \( (3-15) \) s.b. \( (3-6) \)
- p. 67, Example 2, 8th line: \( (3-12) \) s.b. \( (3-3) \)
- p. 104, Prob. 4.11: \( c_i \) and \( b_i \) s.b. \( c_{i+1} \) and \( b_{i+1} \)
- p. 108, Prob. 4.33, line 3: delete "one full adder,"; three half... s.b. four half...
- Delete last sentence of hint.
- p. 145, Prob. 5-9(a): \( M \) s.b. \( m \)
- Prob. 5.15(b) and (f): \( f(d,e,f) \) s.b. \( g(d,e,f) \)
- p. 148, Prob. 5.35(a): \( B'C \) s.b. \( A'B' \); minterm 5 s.b. minterm 2
- Prob. 5.35: second (a) s.b. (b)
- p. 172, Prob. 6.20: \( BC'E'F \) s.b. \( BDE'F \)
- p. 197, Prob. 7.6: \( C'D' \) s.b. \( C'D \)
- p. 199, Prob. 7.24(b): delete the 4th plus sign
- p. 200, Prob. 7.33: equation for \( f_2 \): \( 6 \) s.b. \( 7 \)
- p. 217, Prob. 8.8: add "(no connection)" to the left of \( E \)
- p. 221, Prob. 8.J: line 2, insert after \( AB: (00, 01 \) or 10)
- p. 236, Fig. 9-14: leftmost input line on NAND gate 8 should go to \( A \), not \( A' \)
- p. 241, Fig. 9-23, \( A_1 \) column: move \( X \) from \( m_{10} \) position to \( m_{12} \) position
- p. 245, 3rd line after "Programmable Array Logic": 9-23 s.b. 9-24
- p. 247, last line before Section 9.7: \( X'YC \) s.b. \( X'Y'C_{in} \)
- p. 247, Last line inputs s.b. outputs
- p. 250, 2nd line below Fig. 9-33: H function generator s.b. H multiplexer
- 2nd line above Fig. 9-34: \( a'b'c'd' \) s.b. \( a'b'c'd \)
- p. 253, Prob. 9.6: enable s.b. control
- p. 256, Prob. 9.29: Figure 9-29 s.b. Figure 9-16
- Prob. 9.26(c) s.b. Specify the connection pattern for the PLA. (remove rest of problem)
- p. 275, Fig. 10-13: add before line 1: library BITLIB;
  use BITLIB.bit_pack.all;

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p. 281, Fig. 10-19: after **library** IEEE; add **use** IEEE.std_logic_1164.all;
p. 283, Fig. 10-22, code in box: insert **not** after <= (on all three lines)
p. 293, 7(b): move dashed lines left to line up with rising edge of Clock
p. 303, line 1: **effect** s.b. affect; 2nd line of 2nd paragraph: 5 ns s.b. 7 ns
p. 310, Prob. 11.1, 3rd line, insert before "X becomes": "after 10 ns"
p. 312, figure at bottom left: Clear s.b. ClrN
p. 314, Prob. 11.17(a): when K becomes 1 for the first time, it should remain 1 until after the first falling clock edge.
p. 323, part(d): **falling** s.b. rising
p. 327, Fig. 12-4, input to Register H: **LdG** s.b. **LdH**
p. 329, Figure 12-7(b): add an arrow from the Q₁ waveform to the Q₀ waveform (starting at the last vertical dashed line)
p. 341, Fig. 12-24: P s.b. Clock
p. 354, Prob. 12.23(c): three s.b. four
p. 360, label on last line of timing diagram s.b. Z₂, not Z₁
p. 367, line 14: The false ... s.b. If circuit delays are negligible, the false ...
p. 368, next to the last sentence should read: The next input is \( X = 1 \), so \( A'B' = 01 \), and the state will change after the next rising clock edge.
p. 371, line –3: Table 4-6 s.b. Table 4-4
p. 385, Prob. 13.11: add to D₁ equation: \( +XQ_1' \), add to D₂ equation: \( +X'Q_2 \)
   Prob. 13.11(b): rising and falling s.b. falling and rising
   Prob. 13.11(b), semicolon after \( Q_2 \) s.b. a comma
p. 391, SG 6, 14.5: delete the first two test sequences for X, Z₁, and Z₂
p. 424, Prob. 14.33(c): 14-18(b) s.b. 14-20(b) (two places)
p. 426, part (d): S₂ \( \neq \) S₃ s.b. S₂ \( \neq \) S₃
p. 432, all four maps: \( Q_1Q_2 \) s.b. \( Q_2Q_3 \)
p. 435, Fig. 15-1(b), arrow from H to A: 1/1 s.b. 1/0
p. 436, 4th line after Definition 15.1: length 5, length 6 s.b. length 4, length 5
p. 441, Fig. 15-6(b), loop from S₂ to S₂: 1/1 s.b. 1/0
p. 444, Fig. 15.9(b), Jₜ map: the lower \( B = 0 \) s.b. \( B = 1 \)
p. 445, Fig. 15.10, 2nd map: \( X_2A'B \) s.b. \( X'_2A'B \)
p. 451, Fig. 15-15(b), map for B⁺: 1 in upper right square s.b. 0
p. 454, line 2: 9-34(b) s.b. 9-36(b)
p. 455, Prob. 15.1: in states E, F, and G, outputs for \( X = 1 \) s.b. 0
p. 459, Prob. 15.10(b), 3rd line: length three s.b. length two
p. 461, Prob. 15.18, table: Previous Output s.b. Present Output
p. 476, 8th line of Section 16.4: 13-18 s.b. 13-19
p. 479, sentences starting on the 4th line below Fig. 16-11 should read: If the next input is \( X = 1 \), rows --0- and -1-- are selected, so \( Z = 0 \) and \( D_1D_2D_3 = 110 \). After the active clock edge, \( Q_1Q_2Q_3 = 110 \).
p. 512, Fig. 17-12, line 11: delete >
p. 521, line 11: array s.b. in boldface, vector s.b. vector; line 16: "000>" s.b. "000"
p. 526, line 12: G s.b. C
p. 528, Prob. 17.7, delete comma after: if LDA = '1'

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Formatting, spelling, and grammatical errors:

Unit 2, numerous places: the primes are too close to the variables

p. 23, Prob. 1.3: delete (a)

p. 94, line 20: $m_1$ s.b. $m_1$ M, s.b. $M_1$ [change l (letter ell) to 1 (one)]

p. 104, Prob. 4-15(c): loud speaker s.b. speaker; Prob. 4-16, 1st line: by s.b. by a
p. 120, Section 5.1, line 4: sum-of-product s.b. sum of product
p. 123, caption of Fig. 5-3: Thee s.b. Three
p. 195, caption for Fig. 7-22(b): and s.b. an
p. 212, line –12: a shown s.b. as shown
p. 242, line 14: insert "of" after "number"

p. 254, Prob. 9.11(a), 2nd line: programable s.b. programmable
p. 261, part (d): is 6-bit s.b. is a 6-bit
p. 263, 12th line above Fig. 10-2: indicated s.b. indicate
p. 275, Fig. 10-13, line 3: entity s.b. in boldface
p. 278, lines 16 and 26: in, out, or s.b. in boldface
p. 279, Fig. 10-15, 2nd line of code: BITLB s.b. BITLIB ... 7th line of code: add ; after bit
p. 285, Prob. 10.12, line 3: last "or" s.b. in boldface
p. 289, line 2: start new line with (c)

p. 299, Fig. 11-8, top of map: 00 01 s.b. 0 1
p. 307, Fig. 11-24, right flip-flop: add small arrow at Ck input
p. 308, 4th line above Fig. 11-27: flip-flop s.b. flip-flop
p. 330, Figure 12.9 s.b. Figure 12-9
p. 331, Fig. 12-10(a): Input s.b. Input
p. 351, Prob. 12.13 (figure of shift register): Clk s.b. Clock
p. 354, Prob. 12.23(b): add ) at end

p. 370, Fig 13-13: $x_i, y_i, c_i, c_{i+1}$, and $s_i$ s.b. $x_i, y_i, c_i, c_{i+1}$, and $s_i$
line –3: Table 4-6 s.b. Table 4-4
p. 400, line –11: active/edge clock s.b. active clock edge
p. 423, Prob. 14.31, move vertical line in table downward
p. 438, line 8: $a = d$ s.b. $a = d$

p. 444, line 13: the a $K_A$ s.b. the $K_A$

p. 502, Prob. 2(b): add ( before Remember
p. 509, Fig. 17-6, lines 3, 7, 13, and 15: "out", "begin", "after", and "or" s.b. in boldface
p. 513, 2nd line above Fig. 17-13: remove hyphen from equiva-lent
p. 518, Fig. 17-18, lines 5, 7, 8, 9: "of", "begin" and "process" s.b. in boldface
p. 520, line –11: delete the last "the"

p. 543, line 27: add ) after $M = 1$

p. 549, 5th line above Fig. 18-12: great s.b. greater
p. 563, #6 under Objectives: Delete comma after "using a PLA"

pp. 617 and 619: header at top of page s.b. "VHDL Language Summary"

p. 627, prob. 3.9: insert comma after second $A = 1$

p. 661, Answers 17.1, 3rd line from bottom: "if" s.b. in boldface
p. 663, line –4: insert ; after end process
p. 669, 2(f): add period after 18 states

p. 681, Asynchronous sequential circuit: Replace "See Sequential circuit, asynchronous" with ", 309"
p. 683, under Flip-flop: edge-triggered D s.b. D
pp. 519, 589, 593, 665: all VHDL keywords should be in boldface

**Error on CD (first printing):** solution to Prob. 14.21 is wrong. The correct solution has been installed on the computers in ENS 335, 329, and the LRC labs.