Errata for *Fundamentals of Logic Design,* 5th ed, hardcover (2nd printing)

Look on the back of the title page of the textbook (the copyright page) and you will find a line that reads either 3 4 5 6 7 06 05 04 or 2 3 4 5 6 7 06 05 04 03 or 1 2 3 4 5 6 7 06 05 04 03. If the line begins with 2, you have the second printing of the text, and you should use this errata list. Note that the list is divided into two parts. Be sure to check both parts of the list before reporting any errors.

Reward: Dr. Roth (ENS 510) will pay a $5 reward to the first person who finds any additional technical error in the text. He will pay a $2 reward to the first person who finds any additional minor error (spelling, grammar, etc.). Please verify your error with a T.A. and then send it to roth@ece.utexas.edu .

"s.b." means "should be"

p. 20, line –6: 1011 s.b. 1010

p. 43, Eq. (2-15): $AC'E$ s.b. $AC'E'$

p. 49, Prob. 2.10: $= X + Y$ s.b. $= X$

p. 58, line 2: (3-32) s.b. (3-33)

p. 60, line –4: (3-15) s.b. (3-6)

p. 104, Prob. 4.11: c_i and b_i s.b. c_{i+1} and b_{i+1}

p. 197, Prob. 7.6: $C'D'$ s.b. $C'D$

p. 221, Prob. 8.J: line 2, insert after AB: (00, 01 or 10)

p. 236, Fig. 9-14: leftmost input line on NAND gate 8 should go to A, not A'

p. 241, Fig. 9-23, A_1 column: move X from m_{10} position to m_{12} position

p. 247, Last line inputs s.b. outputs

p. 250, 2nd line below Fig. 9-33: H function generator s.b. H multiplexer
2nd line above Fig. 9-34: $a'b'c'd'$ s.b. $a'b'c'd$

p. 275, Fig. 10-13: add before line 1:

```
library BITLIB;
use BITLIB.bit_pack.all;
```

p. 293, 7(b): move dashed lines left to line up with rising edge of Clock

p. 303, line 1: effect s.b. affect ; 2nd line of 2nd paragraph: 5 ns s.b. 7 ns

p. 310, Prob. 11.1, 3rd line, insert before "X becomes": "after 10 ns"

p. 312, figure at bottom left: Clear s.b. ClrN

p. 323, part(d): falling s.b. rising

p. 329, Figure 12-7(b): add an arrow from the Q_1 waveform to the Q_0 waveform (starting at the last vertical dashed line)

p. 341, Fig. 12-24: P s.b. Clock

p. 360, label on last line of timing diagram s.b. Z_2, not Z_1

p. 368, next to the last sentence should read: The next input is $X = 1$, so $A^+B^+ = 01$, and the state will change after the next rising clock edge.

p. 371, line –3: Table 4-6 s.b. Table 4-4

p. 426, part (d): S2 ≠ S3 s.b. S2 ≠ S3

p. 435, Fig. 15-1(b), arrow from H to A: 1/1 s.b. 1/0

p. 436, 4th line after Definition 15.1: length 5, length 6 s.b. length 4, length 5

p. 441, Fig. 15-6(b), loop from S_2 to S_2: 1/1 s.b. 1/0

p. 445, Fig. 15.10, 2nd map: $X_2A'B$ s.b. $X_2'A'B$

p. 451, Fig. 15-15(b), map for B^+: 1 in upper right square s.b. 0

p. 454, line 2: 9-34(b) s.b. 9-36(b)

p. 476, 8th line of Section 16.4: 13-18 s.b. 13-19

p. 479, sentences starting on the 4th line below Fig. 16-11 should read: If the next input is $X = 1$, rows --0- and -1-- are selected, so $Z = 0$ and $D_1D_2D_3 = 110$. After the active clock edge, $Q_1Q_2Q_3 = 110$.

p. 512, Fig. 17-12, line 11: delete >

p. 521, line 11: array s.b. in boldface; vec**to**r s.b. vector; line 16: "000>" s.b. "000"

p. 526, line 12: G s.b. C

p. 528, Prob. 17.7, delete comma after: if LDA = '1'

p. 532, line –2: 17.20 s.b. 17.19

p. 556, Prob. 18.5, last line: eight to five s.b. ten to six; five s.b. six

p. 569, Fig. 19-7(a), arrow labeled 0/Z1: delete arrowhead on right side

p. 633, Prob. 7.6: $C'D'$ s.b. $C'D$

p. 640, 9.10(a): AND gate input connected to A_3 OR gate: $WX'Z'$ s.b. $WX'Y'$

p. 646, Prob. 11.1: y should go to 1 again at 100 ns

p. 648, 11.9(a): K should go to 1 half-way between the 4th and 5th clock pulses

p. 655, Prob.13.6(c), arrow from S_0 to S_2: 0,1/1 s.b. 0,1/0; in state table, 2nd $X = 0$ s.b. $X = 1$

p. 661, Prob. 15.7(b): $Q_1'Q_2' + XQ_1'$ s.b. $Q_1'Q_3' + X'Q_1'$

p. 663, last line of 2(d): Q 1 1; s.b. Q + 1;
2(h), add another row to table: 0 0 0 | Q_3 Q_2 Q_1 Q_0

Formatting, spelling, and grammatical errors:

p. 23, Prob. 1.3: delete (a)

p. 94, line 20: m_l s.b. m_1 M_l s.b. M_1 [change l (letter ell) to 1 (one)]

p. 120, Section 5.1, line 4: sum-of-product s.b. sum of product

p. 123, caption of Fig. 5-3: Thee s.b. Three

p. 195, caption for Fig. 7-22(b): and s.b. an

p. 242, line 14: insert "of" after "number"

p. 261, part (d): is 6-bit s.b. is a 6-bit

p. 263, 12th line above Fig. 10-2: indicated s.b. indicate

p. 279, Fig. 10-15, 2nd line of code: BITLB s.b. BITLIB ... 7th line of code: add ; after bit

p. 307, Fig. 11-24, right flip-flop: add small arrow at Ck input

p. 308, 4th line above Fig. 11-27: flip-flip s.b.. flip-flop

p. 331, Fig. 12-10(a): Intput s.b. Input

p. 400, line –11: active/edge clock s.b. active clock edge

p. 438, line 8: $a = d$ s.b. $a \equiv d$

p. 444, line 13: the a K_A s.b. the K_A

p. 502, Prob. 2(b): add (before Remember

p. 513, 2nd line above Fig. 17-13: remove hyphen from equiva-lent

p. 520, line –11: delete the last "the"

p. 549, 5th line above Fig. 18-12: great s.b. greater

p. 599, Fig. 20-11, line 6: dividend_ **in** s.b. dividend_in (no space or boldface)

pp. 617 and 619: header at top of page s.b. "VHDL Language Summary"

p. 627, prob. 3.9: insert comma after second A = 1

p. 663, line –4: insert ; after **end process**

p. 669, 2(f): add period after 18 states
p. 681, Asynchronous sequential circuit: Replace "See Sequential circuit, asynchronous" with ", 309"
p. 683, under Flip-flop: edge-triggered D s.b. D
pp. 275, 278, 509, 518, 519, 589, 593, 665: all VHDL keywords should be in boldface