Errata for Fundamentals of Logic Design, 6th edition, 1st & 2nd printing

Look on the back of the title page of the textbook (the copyright page) and you will find a line that reads either 2 3 4 5 6 7 12 11 10, or 1 2 3 4 5 6 7 12 11 10 09. If the line begins with 1, you have the 1st printing of the text, and you should use this errata list. If the line begins with 2, you have the 2nd printing, and only the errors marked with a * apply. Note that the list is divided into two parts. Be sure to check both parts of the list before reporting any errors.

Dr. Roth will pay $5 to the first student who reports a new technical error in this text. He will pay $2 for minor errors like punctuation, spelling, incorrect figure or page references, etc. Please report the error to a TA for verification before contacting Dr. Roth.

* p. 9, line 14, add at end: 3/8
* p. 16, line 19: delete "for a word length of n bits."

p. 135, Figure 5-13: \( = a d + c \overline{d} \) should be \( = a'd + c'd \)
p. 211, Prob. 7-21(e): \( \Pi D(16, \) should be \( \Pi D(17, \)
p. 233, Prob. 8-6(a) -- second sentence should read: Initially \( A = B = C = 0 \) and \( D = 1; \) C changes to 1 at time 2 ns.

p. 279, Prob. 9-41(b): 4-variable should be 3-variable
p. 286, line –11: value of \( D \) should be value of \( C \)
p. 286, line –16: \( (A, B, D) \) should be \( (A, B, C) \)
p. 289, line –12: delete "or equal to"

* p. 305, last line, also p. 684, lines –8 and –17: Synopsis should be Synopsys
p. 313, Prob. 10.22(d): 0100, 0101 should be 0011, 0100
* p. 356, Fig. 12-3(a): triangle above \( \text{D8} \) input should be above the Clock input
p. 382, table in Prob. 12.25: ClN should be ClrN

pp. 458-459, Probs. 14-16(a), 14-18(a), 14-20(a): Assume that in the reset state all previous inputs were 0.

p. 465, Prob. 14.46, label on arrow from state \( S_2 \) back to \( S_2 \): \( X_2 \) should be \( X_1 \)
* p. 476, Fig. 15-1(b), label on arrow from \( H \) to \( A \): 1/1 should be 1/0
* p. 482, Fig. 15-6(b), label on arrow from \( S_2 \) back to \( S_2 \): 1/1 should be 1/0
* p. 485, Fig. 15-9(b), \( J_B \) map: the lower \( B = 0 \) should be \( B = 1 \)
* p. 486, Fig. 15-10, 2nd map: \( X_2' A'B \) should be \( X_2' A'B \)
* p. 493, Fig. 15-15(b), map for \( B^+ \), upper right square: 1 should be 0
* p. 501, problem 15.12, line 3: insert 0010 after 0011
* p. 502, table at the top: for the input pattern 0010, the output should be 1

8/20/10
* p. 559, line 2 of Fig. 17-8: change the last comma to a semi-colon
  line 13: bit-vector should be bit_vector
* p. 568, code lines 1, 4 and 5: SM1_2 should be SM17_2
* p. 569, code lines 3, 6 and 7: SM17_1 should be SM16_4
p. 585, Prob. 17.28(b), add:
  Assume that changes in xin occur 1/4 clock period after the rising edge of clk.
* p. 597, 6th line above Fig. 18-3: register should be registers
p. 659, line 10: State (S) should be State, St
p. 659, line 11: St should be Sh
p. 711, add the following to the answer to Prob. 10.8:
  Addout <= '0' & E + Bus;
  Sum <= Addout(3 downto 0);
  Cout <= Addout(4);
* p. 749, for Characteristic equations: 309 should be 326, 336
p. 749, add under Counters: Johnson, 362

Minor errors (spelling, punctuation, etc.):
* p. 25: last line: weighte should be weighted
* p. 222, line above Fig. 8-3: strainghtforward should be straightforward
p. 245: page number is at the bottom instead of at the top
* p. 292, Fig. 10-8, 2nd line in VHDL code box: bit should not be bold (2 places)
* p. 353, last line circuits should be circuit
* p. 362, line above Section 12.3: feed back should be feedback
* p. 383, Problem 12.26(c): modification the should be modification to the
* p. 477, line –9: Theorem15.1 should be Theorem 15.1
p. 560, Fig. 17-10 caption: clear should be Clear
p. 571, line 9: SM16_5 should be SM16_6
* p. 657, line 8: Notrigger should be NOtrigger