

A 2.7mW 2MHz Continuous-Time $\Sigma\Delta$ Modulator with a Hybrid Active-Passive Loop Filter

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Abstract - We present a 5th-order continuous-time $\Sigma\Delta$ modulator with a hybrid active-passive loop filter consisting of only three amplifiers. The passive integrators save power, and introduce no distortion. The active integrators provide gain and minimize internal noise contributions. A single-bit switched-capacitor DAC is employed as the main feedback DAC for high clock jitter immunity. An additional current steering DAC stabilizes the loop with the advantage of simplicity. To verify the proposed techniques, a prototype continuous-time $\Sigma\Delta$ modulator with 2MHz signal bandwidth is designed in a 0.25 μ m CMOS technology targeting for GPS or WCDMA applications. The experimental results show that the prototype $\Sigma\Delta$ modulator achieves 68dB dynamic range over 2MHz bandwidth with a 150MHz clock, consuming 1.8mA from a 1.5V supply.

I. INTRODUCTION

Battery powered portable applications demand analog-to-digital (A/D) converters with low power consumption for a long battery life. $\Sigma\Delta$ A/D converters offer economical solutions with up to multi MHz signal bandwidth, and have been traditionally realized with switched-capacitor (SC) techniques. In recent years, $\Sigma\Delta$ modulators with continuous-time (CT) loop filters attracted much attention due to the low power consumption [1,7]. By placing the sampling network after the high gain noise shaping loop filter, sampling nonidealities are significantly suppressed. Additionally, the CT loop filter acts as an anti-alias filter, attenuating out-of-band high frequency interferences. CT $\Sigma\Delta$ modulators are usually more power efficient than SC implementations, because there is no settling time requirement for CT circuits.

Loop filters in CT $\Sigma\Delta$ modulators are usually implemented with active integrators [1,7], such as active-RC or g_m -C integrators. It proved possible that the loop filter can be implemented with all passive integrators, as demonstrated by a 0.25mW 13b 20kHz bandwidth passive $\Sigma\Delta$ modulator [2], in which the only active component is the quantizer. Passive integrators consume no power, and introduce no distortion. However, no signal gain is provided by passive components. The very small voltage swing at the input of the quantizer makes the design of the quantizer a challenging task. Unlike a conventional $\Sigma\Delta$ modulator with active integrators, nonidealities (such as thermal noise and quantizer offset) of the loop filter and the quantizer in a passive $\Sigma\Delta$ modulator can not be suppressed by the passive loop filter that attenuates instead of amplifies the signal. Thus, internal electronic noise of the loop filter and quantizer will be referred back to the

input of the modulator with a high amplitude that is inversely proportional to the loop filter gain, degrading the SNR performance. The above considerations almost preclude the use of high order loop filters due to the significant signal attenuation at high frequencies. One technique to solve the problem is to increase the loop gain by adding active integrators [3]. However, the modulator in [3] demands a current input signal, not convenient for many applications. Moreover, due to the loading effect of the SC feedback DAC, which is equivalent to a resistance of $1/(T_s C_{DAC})$ at low frequencies, the gains of the active integrators are low, degrading noise shaping effects.

In this paper, a low power 5th-order CT $\Sigma\Delta$ modulator is designed, combining the merits of both active and passive implementations. The modulator operates at 150MHz clock frequency, achieving 68dB dynamic range over a 2MHz signal bandwidth with 2.7mW power consumption.

II. CONTINUOUS-TIME $\Sigma\Delta$ MODULATOR WITH A HYBRID ACTIVE-PASSIVE LOOP FILTER

A. The $\Sigma\Delta$ Modulator Architecture

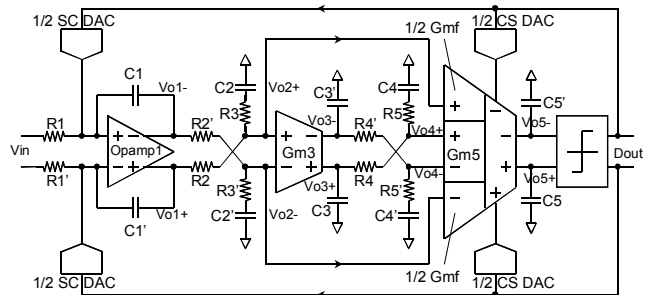


Fig. 1. The architecture of the proposed $\Sigma\Delta$ modulator.

The architecture of the $\Sigma\Delta$ modulator is shown in Fig. 1, with three active integrators (as the 1st, 3rd, and 5th stages) and two passive ones (as the 2nd and 4th stages). In each of the passive integrators, a local feedforward path is formed with extra resistors (such as R3 and R3' in Fig. 2) to stabilize the modulator loop. Switched-capacitor and current-steering DACs are employed for both good clock jitter immunity and design simplicity. The last g_m -C integrator also works as a signal summation stage.

For high linearity, the 1st-stage integrator is implemented as an active-RC integrator, which effectively suppresses thermal noise from the 2nd- and later stages of integrators. The

other two active integrators have relatively relaxed linearity requirement, therefore they are realized as g_m -C integrators for low power consumption. Additionally, the 3rd-stage g_m -C integrator buffers the 2nd-stage passive RC integrator to avoid loading the 2nd-stage passive integrator with the 4th-stage passive integrator. In addition, the active integrators help to maintain high enough signal levels at intermediate nodes. Otherwise the high frequency components of the signal could be significantly attenuated by the passive network.

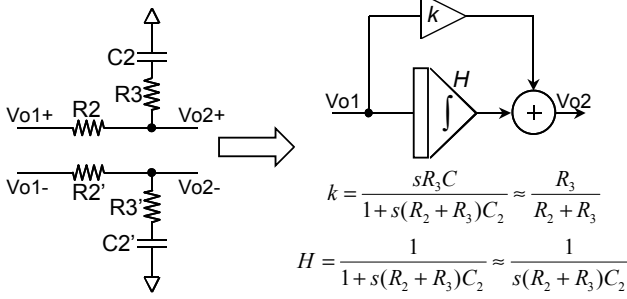


Fig. 2. The equivalent signal path of a passive RC integrator.

To stabilize the $\Sigma\Delta$ modulator, four distributed feedback or weighted feedforward paths are necessary, in addition to the main feedback DAC. The passive network implemented with R2, R3 and C2 adds one zero in the transfer function, and provides a local feedforward path, as illustrated in Fig. 2. R4, R5 and C4 in Fig. 1 also implement another local feedforward path. The passive RC network in Fig. 2 is equivalent to a feedforward path in parallel with an integrator, which has a unity gain angular frequency of $1/(R_2+R_3)C_2$. At high frequencies, the value of $\omega(R_2+R_3)C_2$ is far greater than 1, therefore the passive integrator behaves similarly as an ideal integrator. In conventional all-active loop filter implementations, active transconductors are generally employed to realize feedforward coefficients [7], consuming additional power. Whereas the passive feedforward path in Fig. 2 does not consume any extra power. The remaining two zeros for stabilizing the whole loop are provided by the transconductor G_{mf} and a current steering feedback DAC. Therefore, the overall $\Sigma\Delta$ architecture employs three weighted feedforward paths and one feedback path, in addition to the main SC feedback DAC.

The values of resistors, capacitors, and transconductances can be derived in the following steps. First, a sample 5th-order discrete-time $\Sigma\Delta$ modulator is designed with a z-domain loop filter function $H_D(z)$, optimized for SQNR at a given OSR. Next, $H_D(z)$ is transformed to s-domain as $H_C(s)$ with impulse-invariant transform. Then $H_C(s)$ is mapped to the transfer function of hybrid active-passive loop filter in Fig. 1, with a transfer function of,

$$H_{APLF}(s) = H_{DAC1}(H_1H_2H_3H_4H_5 + H_1H_2H_3k_1) + H_{DAC2}H_3k_2 \quad (1)$$

where H_1 to H_5 are given by,

$$H_1 = \frac{1}{sC_1} \quad (2a)$$

$$H_2 = \frac{\frac{R_3}{R_2 + R_3} + \frac{1}{s(R_2 + R_3)C_2}}{1 + \frac{1}{s(R_2 + R_3)C_2}} \quad (2b)$$

$$H_3 = \frac{G_{m3}}{sC_4} \quad (2c)$$

$$H_4 = \frac{\frac{R_5}{R_4 + R_5} + \frac{1}{s(R_4 + R_5)C_4}}{1 + \frac{1}{s(R_4 + R_5)C_4}} \quad (2d)$$

$$H_5 = \frac{G_{m5}}{sC_5} \quad (2e)$$

Coefficients k_1 and k_2 are parameters to be determined. H_{DAC1} and H_{DAC2} in Eq. (1) are the transfer functions of the SC DAC and the current-steering DAC. For CT $\Sigma\Delta$ modulators, both the DAC waveform shaping and the time delay determine H_{DAC1} or H_{DAC2} [4]. The transfer functions of the SC (H_{SCDAC}) and current-steering (H_{CSDAC}) DACs are respectively given by the following equations,

$$H_{SCDAC} = \frac{T_s / \tau}{s + T_s / \tau} \cdot e^{-s/2} \quad (3)$$

$$H_{CSDAC} = \frac{2 \cdot (e^{-s/2} - e^{-s})}{s} \quad (4)$$

The τ in Eq. (3) is the SC RC time constant. Half clock cycle delay is introduced in the feedback DACs to accommodate the time delay of the quantizer and digital circuitry [5]. Eqs. (1), (2a-e), (3) and (4) characterize the proposed hybrid active-passive loop filter, which can be mapped to the pre-designed $H_C(s)$. Subsequently, the values of resistors, capacitors and coefficients k_1 and k_2 can be determined for the active-passive $\Sigma\Delta$ modulator with an equivalent noise transfer function $H_D(z)$.

One disadvantage of a CT $\Sigma\Delta$ modulator is the high sensitivity of the loop filter transfer function to process variations, because some of the filter coefficients are determined by absolute RC product values, which may vary up to 30%. As RC products vary from the nominal values, the performance of the $\Sigma\Delta$ modulator degrades, and the loop may even become unstable. As shown in Fig. 3, when the RC time constant increases, the maximum SQNR gradually degrades, and the $\Sigma\Delta$ modulator remains stable. However, if the RC time constant decreases to less than 0.85, the modulator becomes unstable, similar to what was reported in [1]. The RC time constant sensitivity of a CT active-passive $\Sigma\Delta$ modulator is close to that of a conventional CT $\Sigma\Delta$ modulator.

Many techniques have been proposed to solve the RC time constant sensitivity problem in CT $\Sigma\Delta$ modulators [1] [6]. In this design, we intentionally set the RC time constant value to 1.1 times of its nominal value [1], resulting in a nominal SQNR of 75dB. Even if the RC time constant varies $\pm 20\%$, the entire $\Sigma\Delta$ modulator still keeps stable and the SQNR varies from 70dB to 80dB. To compensate for larger RC time constant variations ($> \pm 20\%$), discretely tunable capacitors can be employed. Capacitors {C2-C5} can be tuned from 50% to 200% of their nominal values, at a step of approximately

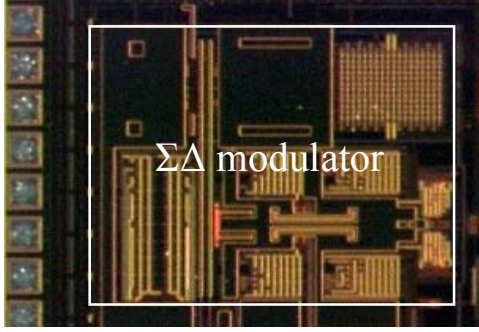


Fig. 8. The microphotograph of the prototype chip.

III. EXPERIMENTAL RESULTS

The prototype chip was designed and fabricated in a 0.25 μ m CMOS technology for GPS or WCDMA receiver applications. The microphotograph is shown in Fig. 8, with an active area of 0.42mm². The prototype is characterized experimentally with a 150MHz clock and a 100kHz input signal. The power spectral density is plotted in Fig. 9. Two-tone intermodulation test result is shown in Fig. 10, with an IM3 of 69dB. The peak SNR and SNDR over a 2MHz signal bandwidth are 63.9dB and 63.4dB, respectively. The SNDR vs. input signal level is plotted in Fig. 11, showing that a dynamic range of around 68dB has been achieved. The power consumption is 2.7mW from a 1.5V supply. Table I summarizes the measured performance of the prototype modulator.

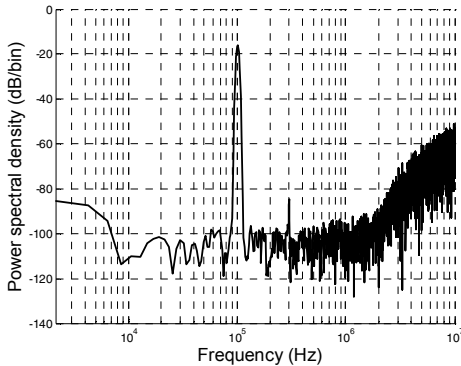


Fig. 9. The measured output spectrum (input signal frequency = 100 kHz)

Table I, Summary of the measured performance

Technology	0.25 μ m 1P5M CMOS
Supply Voltage	1.5V
Power Consumption	2.7mW
Active Area	0.42mm ²
Peak SNR/SNDR	63.9dB/63.4dB
Dynamic Range	68dB
Clock frequency	150MHz
Signal bandwidth	2MHz

IV. CONCLUSION

A 2MHz signal bandwidth continuous-time $\Sigma\Delta$ modulator with a hybrid active-passive loop filter has been presented. This design features wide signal bandwidth and low power consumption. A prototype $\Sigma\Delta$ modulator was fabricated in a 0.25 μ m CMOS technology, achieving a peak SNDR of 63.4dB and a dynamic range of 68dB.

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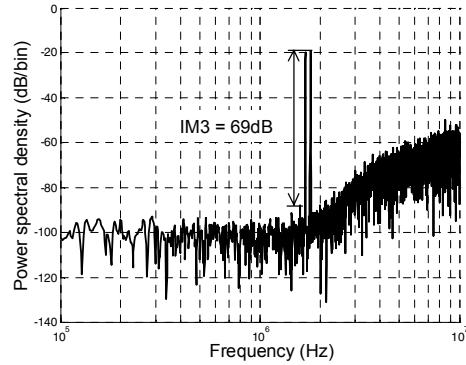


Fig. 10. Two-tone intermodulation test (input frequencies: 1.7MHz and 1.8MHz).

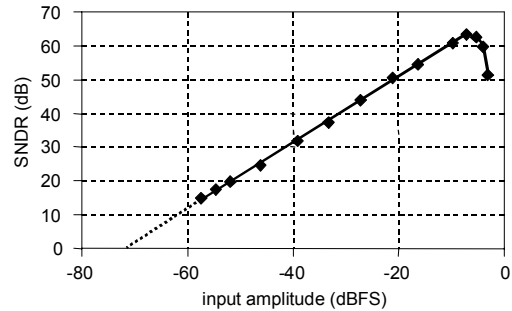


Fig. 11. Measured SNDR vs. input signal amplitude.

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