A 2.7mW 2MHz Continuous-Time \( \Sigma \Delta \) Modulator with a Hybrid Active-Passive Loop Filter

Tongyu Song, Zhiheng Cao, and Shouli Yan
Department of Electrical and Computer Engineering
The University of Texas at Austin
Austin, TX 78712

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Outline

• Introduction
• Architecture Design
• Circuit Implementation
• Experimental Results
• Conclusion
Introduction

- Wireless receiver applications demand
  - Low power consumption for long battery life
  - Large dynamic range for simple architecture
  - Low supply voltage compatible with advanced CMOS technologies
- Target specifications (for WCDMA)
  - 2 MHz signal bandwidth
  - 11-bit dynamic range
  - Minimum power dissipation
  - Low supply voltage
Discrete-Time or Continuous-Time (CT) ΣΔ Modulator?

- Continuous-time (CT) ΣΔ modulator
  - Low power dissipation
  - Inherent anti-aliasing
  - Suppressed sampling non-idealities
  - Simple interface with preceding stage
  - Non-zero excess loop delay
  - High clock jitter sensitivity
  - RC time-constant variation

- Design decision
  - CT ΣΔ implementation is chosen
Passive or Active Loop Filter?

- **Passive $\Sigma\Delta$ modulator** [Chen, JSSC 97]
  - ✓ No amplifier in the loop filter $\rightarrow$ low power filter
  - ✓ Gain provided by comparator $\rightarrow$ no linearity requirement
  - ✗ High input referred thermal noise $\rightarrow$ low SNR
  - ✗ Small internal voltage swing, not suitable for high order modulator $\rightarrow$ low SNR
Passive or Active Loop Filter? (Cont’d)

- **Active CT $\Sigma\Delta$ modulator implementation** [van der Zwan, JSSC 97]
  - Integrators as active-RC or gm-C integrators
  - Feedforward paths as gm stages

![Active CT $\Sigma\Delta$ modulator architecture](image)
Passive or Active Loop Filter? (Cont’d)

- Pros and cons of active CT $\Sigma \Delta$ modulator
  - High loop gain $\rightarrow$ low input referred noise
  - High order noise shaping possible $\rightarrow$ high SNR
  - Active integrators consume power

![Active CT $\Sigma \Delta$ modulator implementation](image)
Passive or Active Loop Filter? (Cont’d)

• The best should be a combination of both active and passive implementations [Das, ISSCC 2005]
• Therefore, a hybrid active-passive loop filter is chosen
  – Active integrators $\rightarrow$ high loop gain, efficient noise shaping and low input referred noise
  – Passive integrators $\rightarrow$ low power dissipation
Proposed Continuous-Time (CT) $\Sigma\Delta$ Modulator Architecture

- A 5th-order noise shaping is achieved with 3 active integrators and 2 passive integrators.
- Single-bit internal quantization is chosen for simple implementation.
- Two feedback DACs, DAC1 and DAC2, are employed.
Non-Zero Excess Loop Delay Compensation

\( \Phi_1: \) clock of the comparator
\( \Phi_2: \) clock of the feedback DACs
\( D: \) comparator digital output
\( T_{dc}: \) comparator delay
\( \tau_{DAC}: \) intentional DAC delay

(a) Loop filter impulse response without DAC2
(b) Impulse response of DAC2 and the 5th integrator
(c) DAC2 output waveform

Combining (a) and (b) to achieve ideal loop filter response with zero loop delay
Passive Network

- Passive implementation of integration & feedforward zero
- No DC power dissipation
- No signal distortion
- Voltage gain lower than that of active implementation

\[
k = \frac{sR_3C}{1+ s(R_2 + R_3)C_2} \approx \frac{R_3}{R_2 + R_3}
\]

\[
H = \frac{1}{1+ s(R_2 + R_3)C_2} \approx \frac{1}{s(R_2 + R_3)C_2}
\]
For a single-bit $\Sigma\Delta$ modulator with NRZ DAC, the maximum SNR due to clock jitter is

$$SNR_{\text{max}} = 10\log \left( \frac{\text{OSR}}{8} \left( \frac{T_s}{\sigma_{\text{clk}}} \right)^2 \right)$$
Feedback DAC Implementations

<table>
<thead>
<tr>
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<th>Switched-Capacitor DAC</th>
<th>Current Steering DAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jitter sensitivity</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Silicon area</td>
<td>Large</td>
<td>Small</td>
</tr>
</tbody>
</table>

- Design choice
  - DAC1: switched-capacitor DAC for low jitter sensitivity
  - DAC2: current steering DAC for low power & small area
Overall $\Sigma\Delta$ Modulator Circuit Implementation

- Integrators
  - 1\textsuperscript{st} stage: active RC
  - 2\textsuperscript{nd} and 4\textsuperscript{th} stages: passive RC
  - 3\textsuperscript{rd} and 5\textsuperscript{th}: gm-C

- Feedback DACs
  - DAC1: switched capacitor DAC
  - DAC2: current steering DAC
Loop Filter Design

The overall loop gain of the noise shaping loop filter:

\[ H_{APLF}(s) = H_{DAC1}(H_1 H_2 H_3 H_4 H_5 + H_1 H_2 H_5 k_1) + H_{DAC2} H_5 k_2 \]
Loop Filter Design (Cont’d)

Active RC integrator:
\[ H_1 = \frac{1}{sC_1} \]
\[ H_1 = \frac{R_3}{R_2 + R_3} + \frac{1}{s(R_2 + R_3)C_2} \]

Passive RC network:
\[ H_2 = \frac{1}{1 + \frac{1}{s(R_2 + R_3)C_2}} \]
\[ H_2 = \frac{R_3}{R_2 + R_3} + \frac{1}{s(R_2 + R_3)C_2} \]

Gm-C integrator:
\[ H_3 = \frac{G_{m3}}{sC_4} \]

Passive RC network:
\[ H_4 = \frac{R_5}{R_4 + R_5} + \frac{1}{s(R_4 + R_5)C_4} \]
\[ H_4 = \frac{R_5}{R_4 + R_5} + \frac{1}{s(R_4 + R_5)C_4} \]
Loop Filter Design (Cont’d)

Gm-C integrator:  

$$H_5 = \frac{G_{m5}}{sC_5}$$

DAC1:  

$$H_{DAC1} = \frac{V_{REF}}{R_{SW}} \frac{1}{s + 1/\tau} \left( e^{-sT_S/2} - e^{-T_S/(2\tau)} e^{-sT_S} \right)$$

DAC2:  

$$H_{DAC2} = \frac{I_{REF}}{g_{m5}} \frac{e^{-sT_S/2} - e^{-sT_S}}{s}$$
RC Time Constant Sensitivity

- $\Sigma \Delta$ modulator performance vs. RC time constant variation [Yan, JSSC 2004]
  - When the time constant is smaller than a certain value, the loop becomes unstable.
  - When the time constant is too large, SQNR degrades.
  - The nominal time constant is set at around 1.1 in the design.
The First Stage Integrator

- Active RC integrator for excellent linearity
- Switched-capacitor feedback DAC for low jitter sensitivity
- opamp1 as a telescopic opamp.

Maximum SNR due to clock jitter:

\[
SNR_{\text{max}} = 10 \log \left[ \frac{OSR \left( \frac{T_s}{\sigma_{clk}} \right)^2 \cdot \left( \frac{1}{2} \frac{T_s}{\tau} \right)^2}{8} \right]
\]
OPAMP1 Schematic

- Telescopic (instead of folded cascode) amplifier for small quiescent current
- Output common mode sensed by the 3rd stage integrator
The Third Stage Integrator

- Gm-C integrator for low power dissipation
- Vcmo1 senses the output common mode voltage of the first stage integrator
The Fifth Stage Integrator with Current Summation
Chip Microphotograph

- Process: 0.25 μm 1P5M CMOS
- Active area: 0.42 mm²
Experimental Results

PSD with 100 kHz sine input signal  two-tone intermodulation test

IM3 = 69dB
Measured SNDR vs. Input Signal Level

Dynamic Range (DR) = 68dB
# Performance Summary

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<table>
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<tbody>
<tr>
<td>**Signal frequency/</td>
<td>2 MHz / 150 MHz</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td></td>
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<tr>
<td><strong>Dynamic range</strong></td>
<td>68 dB</td>
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<tr>
<td><strong>Peak SNR/SNDR</strong></td>
<td>63.9 dB / 63.4 dB</td>
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<tr>
<td><strong>Power consumption</strong></td>
<td>1.8 mA × 1.5 V</td>
</tr>
<tr>
<td><strong>Silicon area</strong></td>
<td>0.42 mm²</td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>TSMC 1P5M 0.25 μmCMOS</td>
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Conclusion

- A 5th-order CT ΣΔ modulator with only 3 amplifiers was designed with an active-passive loop filter.
- Improved excess loop delay compensation.
- Robust to RC time-constant variation.
- Low clock jitter sensitivity.
- Prototype chip
  - 0.25μm CMOS, 0.42 mm² active area
  - with 2MHz signal bandwidth
  - achieving 68dB dynamic range, 69dB IM3
  - consuming 1.8mA from 1.5V supply
- The proposed ΣΔ modulator is suitable for low power portable applications.
Acknowledgement

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