3.5 A Continuous-Time ΣΔ Modulator with 88dB Dynamic Range and 1.1MHz Signal Bandwidth

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A baseband continuous-time multi-bit ΣΔ modulator achieves 88dB dynamic range over a 1.1MHz signal bandwidth consuming 62mW from a 3.3V supply. Excess loop delay encountered in conventional continuous-time modulators is eliminated by the proposed architecture. Clock-jitter sensitivity is considerably reduced compared with prior designs.

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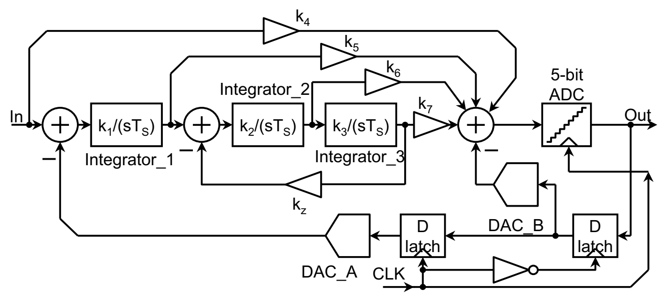
Outline

- Advantages/disadvantages of CT (continuous-time) ΣΔ modulators
- Multi-bit CT ΣΔ architecture
- Circuit design and implementation
- Experimental results
- Summary

Multi-bit CT ΣΔ Modulator Architecture



Proposed 5-bit 3rd-order CT ΣΔ modulator architecture

Advantages and Disadvantages of CT ΣΔ Modulators

- Advantages
  - Potentials for high speed and lower power consumption
  - Relaxed sampling network requirements
  - Intrinsic anti-alias filtering
- Disadvantages
  - Sensitive to loop delay and clock jitter
  - Loop filter RC time constant variations
  - Discrete time to continuous time mapping

Multi-bit CT ΣΔ Modulator Architecture

- Multi-bit quantizer and DAC are chosen to achieve higher resolution.
- NRZ (non-return-to-zero) multi-bit DAC effectively reduces clock jitter sensitivity.
- Loop filter architecture eliminates the performance degradation due to non-zero loop delay.
- A feedforward path, k4, could effectively reduce the internal signal swing.

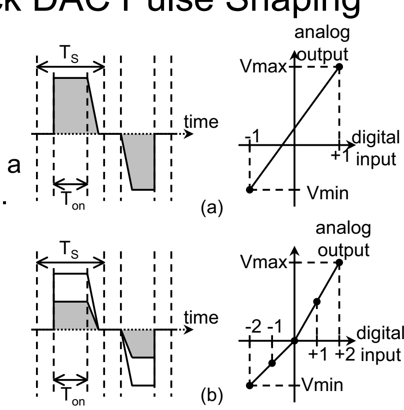
Prior Work of CT ΣΔ Modulators

- 1-bit or 1.5-bit quantization
- Delayed RZ (return-to-zero) DAC pulse shaping
- Performance sensitive to clock jitter
- Either low bandwidth [zwan00] or low resolution [veldhoven02]

[zwan00] E. J. van der Zwan, *et al.*, "A 10.7MHz IF-to-baseband ΣΔ A/D conversion system for AM/FM radio receivers," *ISSCC 2000*, pp. 340-341,469.
[veldhoven02] R. van Veldhoven, *et al.*, "A 3.3mW ΣΔ modulator for UMTS in 0.18µm CMOS with 70dB dynamic range in 2MHz bandwidth," *ISSCC 2002*, pp. 222-223,461.

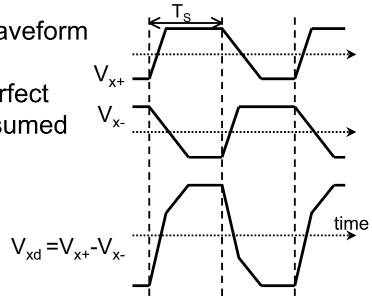
Feedback DAC Pulse Shaping

- RZ pulse overcomes inter-symbol interference in a single-bit DAC.
- However, a multi-bit RZ DAC is not linear.



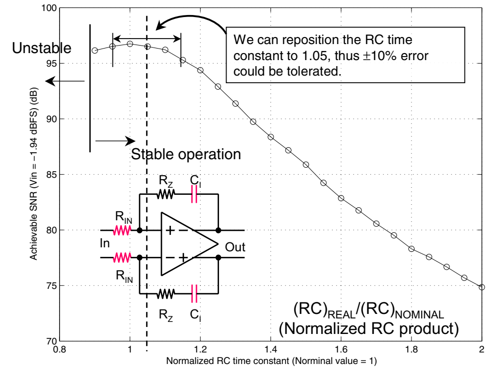
Feedback DAC Pulse Shaping

- A differential waveform is intrinsically symmetric if perfect matching is assumed [jensen95].



[jensen95] J. F. Jensen, *et al.*, "A 3.2-GHz second-order delta-sigma modulator implemented in InP HBT technology," *IEEE J. Solid-State Circuits*, vol. 30, no. 10, pp. 1119-1127, Oct. 1995.

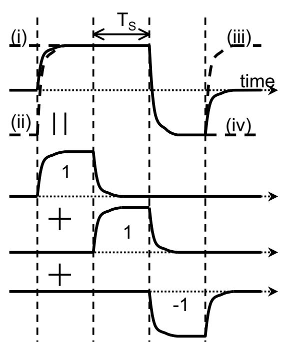
Loop Filter RC Time Constant Tuning



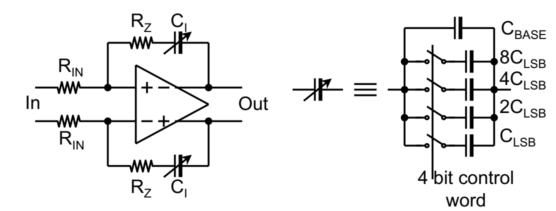
Simulated SNR vs. RC time constant

Feedback DAC Pulse Shaping

- If the DAC waveform settles within one clock period, an NRZ waveform can be viewed as *linear* addition of ±unit pulses with different unit delays.
- This principle applies to multi-level DAC as well.
- ISI (Inter-symbol-interference) between two adjacent symbols still exists, but does not hurt linearity.



Loop Filter RC Time Constant Tuning



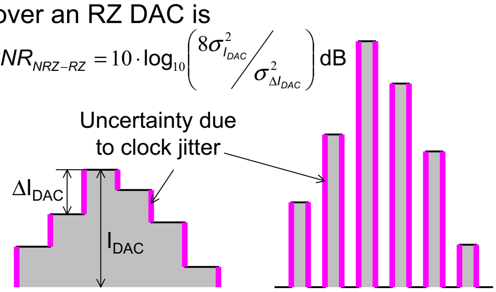
- Discrete capacitor tuning [durham92] to overcome large (> ±10%) RC product variation

[durham92] A. M. Durham, W. Redman-White, and J. B. Hughes, "High-linearity continuous-time filter in 5-V VLSI CMOS," *IEEE J. Solid-State Circuits*, vol. 27, no. 9, pp. 1270-1276, Sept. 1992

Feedback DAC Pulse Shaping

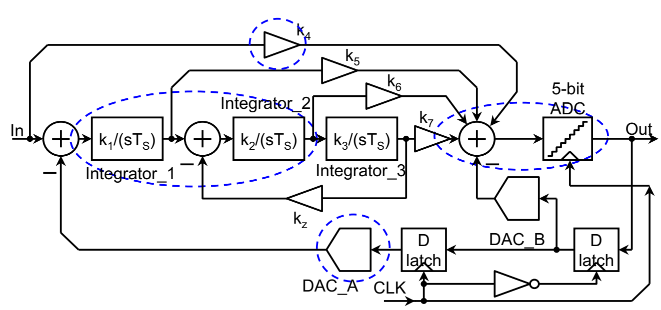
- The SNR improvement of an NRZ DAC over an RZ DAC is

$$SNR_{NRZ-RZ} = 10 \cdot \log_{10}\left(\frac{8\sigma^2_{I_{DAC}}}{\sigma^2_{\Delta I_{DAC}}}\right) \text{dB}$$

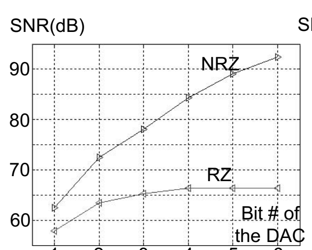


NRZ Pulse Shaping RZ Pulse Shaping

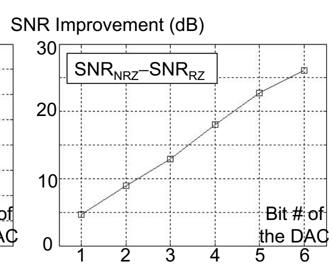
Multi-bit CT ΣΔ Modulator Architecture



Feedback DAC Pulse Shaping



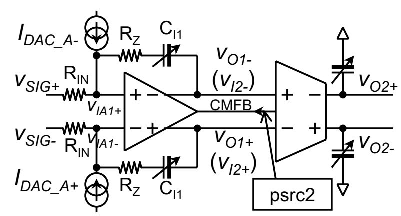
SNR of NRZ and RZ DAC pulse shaping vs. DAC bit number



SNR improvement vs. DAC bit number

Simulated SNR for clock jitter (RMS value) = 20 ps

1st- and 2nd- Stage Integrators



- 1st-stage integrator is an active-RC integrator
- 2nd-stage integrator uses gm-C structure

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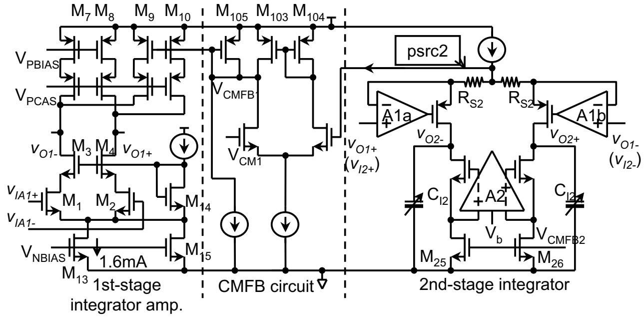
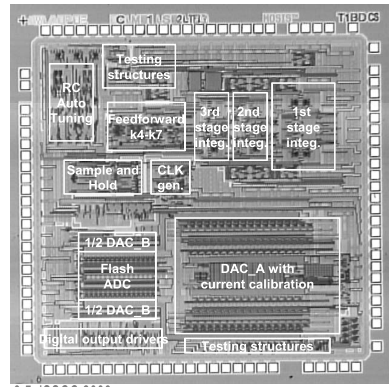
1st- and 2nd- Stage Integrators



Detailed schematics of the 1st-stage integrator amplifier and 2nd-stage integrator

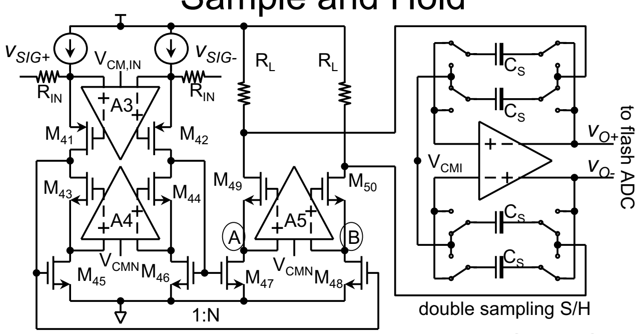
Chip Microphotograph



Technology: 0.5 μm 2P3M CMOS

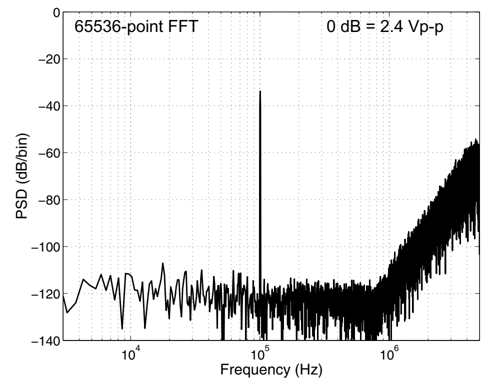
Silicon Area: 2.4x2.4 mm² (excluding frame and pads)

Current Summation and Sample and Hold

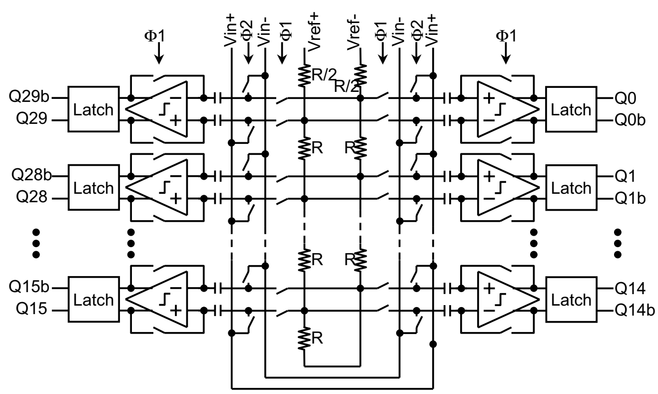


Currents from feedforward paths add at nodes (A) and (B)

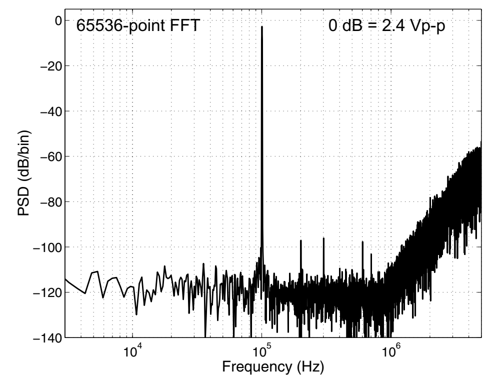
PSD with –33dB$_{FS}$ 100 kHz Input



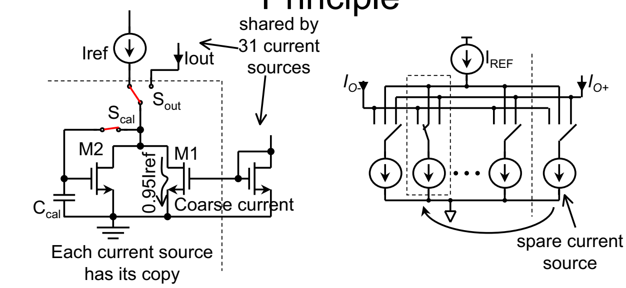
5-bit Internal Flash A/D Converter



PSD with –2.4dB$_{FS}$ 100 kHz Input



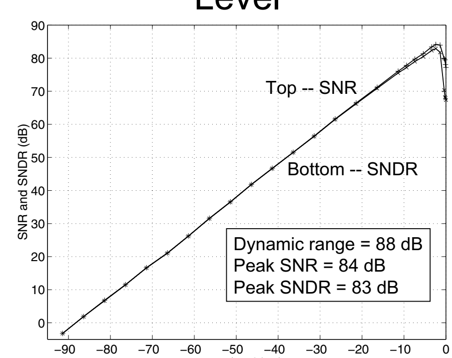
DAC_A Current Calibration Principle



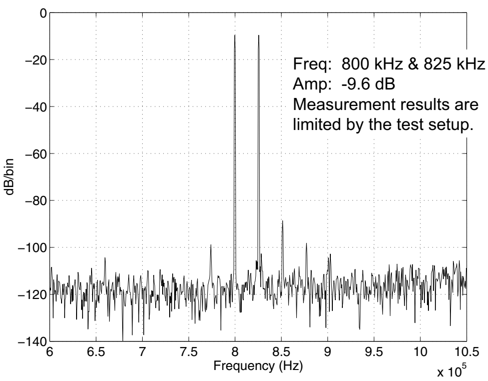
Current calibration principle [groene89]

[groene89] D. W. J. groeneveld, *et al*, "A self-calibration technique for monolithic high-resolution D/A converters," *IEEE J. Solid-State Circuits*, vol. 24, no. 6, pp. 1517-1522, Dec. 1989

SNR and SNDR vs. Input Signal Level



Two-Tone Inter-Modulation Test



Performance Summary

Signal bandwidth	1.1MHz
Sample frequency	35.2MHz
Oversampling ratio	16
Dynamic range	88dB
SNR	84dB
SNDR	83dB
SFDR	93dB
Power consumption	62mW
Supply voltage	3.3V
Process	0.5µm 2P3M CMOS
Area	$2.4x2.4mm^2$

Summary

- Multi-bit quantizer and DAC are chosen for high resolution.
- NRZ (non-return-to-zero) multi-bit DAC effectively reduces clock jitter sensitivity.
- Loop filter architecture accommodates non-zero loop delay.
- Current calibration of DAC_A improves linearity.
- 1.1 MHz input bandwidth and 88dB dynamic range have been achieved.