Testing Domino Circuits in SOI Technology

Eric MacDonald

Advanced PowerPC Development
11400 Burnet Road
IBM, Austin, TX 78712
<emac@us.ibm.com>

Nur A. Touba

Computer Engineering Research Center
Dept. of Electrical and Computer Engineering
University of Texas, Austin, TX 78712-1084
<touba@ece.utexas.edu>

Abstract

The proliferation of both Partially Depleted Silicon-On-Insulator (PD-SOI) technology and domino circuit styles has allowed for increases in circuit performance beyond that of scaling traditional bulk CMOS static circuits. However, interactions between dynamic circuit styles and PD-SOI complicate testing. This paper describes the issues of testing domino circuits fabricated in SOI technology and new tests are proposed to address the interactions. A fault modeling analysis is described which demonstrates that the overall fault coverage can be improved beyond that of traditional testing of domino circuits in bulk technology.

1. Introduction

Partially-Depleted Silicon-On-Insulator technology has become a leading candidate for replacing traditional bulk CMOS as the dominant processing vehicle for high performance / low power VLSI designs. Based on the significant reduction in junction capacitance of the individual transistor, SOI provides a reduction in delay or a corresponding reduction in dynamic power consumption. Furthermore, the isolation of the transistor body in SOI leads to several other advantages including the elimination of latch-up and a reduction of the soft error rate [Krishnan98] [Chuang98] [Shahidi98]. At the same time, dynamic circuit styles have become increasingly more pervasive in high performance circuits. In dynamic circuits, the reductions in input capacitance and decreases in intrinsic delay can lead to a significant increase in performance. Combining the advantages of SOI with those of dynamic circuit styles allows designers to leverage the two performance enhancements in tandem.

However, dynamic circuits are not considered as robust as traditional static circuits due to an increased sensitivity to leakage. SOI technology, on the other hand, introduces new sources of leakage, which did not previously exist in traditional bulk CMOS technology. These leakages result from the parasitic bipolar transistor inherent in SOI CMOS transistors and can cause the unintentional discharge of dynamic nodes. With proper consideration taken, SOI dynamic circuits can be guaranteed to operate correctly in the fault-free case. However, specific defects, which would not be detectable in bulk technology, can now become manifest in SOI if the bipolar leakage is triggered. New test sequences are necessary to ensure that the interactions between dynamic circuits and SOI technology do not induce failures during field operation in the customer's application. This paper presents such a technique and shows through fault modeling that the test coverage is actually improved beyond that possible with traditional tests on circuits fabricated in bulk technology.

This paper begins by describing the reason for the increase of the leakage sensitivity in domino circuits. Section 3 explains parasitic bipolar leakage in SOI and how it relates to possible failures in circuits with dynamic nodes. New test techniques are then proposed to provide the worst-case environment for these SOI-related leakages and a fault study describes the defects that the new technique detects. Finally, simulations are presented highlighting the need for this new technique.

2. Leakage Sensitivity of Domino Circuits

Dynamic circuits are used in most of the high performance microprocessors in production today. Domino logic, for example, is often used in the word line drivers of on-chip arrays such as caches, tags and register files or where wide OR gate logic (8, 16, or 32 inputs) is required and static circuits are insufficient in terms of delay and area constraints. The primary advantage of domino logic results from implementing the gate's function with only an NFET pulldown network as represented with transistors *N2* and *N3* in the simple domino AND gate depicted in Fig. 1. A clock is used to activate a PFET pullup transistor (*P1*) during a pre-charge phase. This results in the gate driving a logic

1081-7735/00 $10.00 © 2000 IEEE

low value on the output regardless of the values on the other inputs. The evaluate stage occurs when the clock is asserted causing the pullup transistor to cease conduction, while activating the foot device (*N1*). This allows the NFET network to conditionally discharge the intermediate node (*Dynamic Node* in Fig. 1) that controls the output through an inverter (*P2* and *N4*). If the pulldown network does not evaluate, then the intermediate node is left un-driven for the remainder of the clock phase - dynamically storing a logic high value.

Figure 1. Simple domino AND gate

The advantages of domino circuits include improvements in both performance and die area. The increase in performance is related to the significant decrease in capacitance as seen at the inputs and the elimination of contention between the PFET and NFET networks as compared to static circuits. The decrease in input capacitance is the result of each input connecting only to a single NFET, while the mutually-exclusive conduction of the NFET and PFET networks allows for faster switching. Furthermore, by eliminating the dual PFET pull-up network, a significant reduction in area can be achieved. Where traditional static circuits require two transistors per input, domino circuits require one NFET transistor per input with the addition of three other transistors per gate – one PFET for pre-charge and a PFET / NFET pair providing an output inverter. This decrease in area not only reduces the die size and associated costs but also reduces the length of the global routing across larger sub-circuits – improving the performance further.

Domino circuits are more sensitive to leakage events due to the dynamic nature of the intermediate node, which can be inadvertently discharged resulting in an incorrect evaluation of the gate [Srivastava 91]. In bulk technology, the sources of leakage include sub-threshold current, charge sharing, alpha particles and noise at input. A keeper transistor (*P3*) can be included as illustrated in Fig. 2 to replenish charge lost to these leakages. However, the keeper results in some reduction in performance due to the parasitic capacitance introduced by the drain of *P3* and the additional current that the NFET network must fight during evaluation. For these reasons, keeper devices are generally designed with minimum dimensions. Additionally, testing for the existence of the keeper is notoriously difficult. A defect that disables the keeper functionality may not result in a failure if a leakage mechanism is not activated during test. This may later result in a field failure.

Figure 2. Domino AND gate with keeper transistor

3. Interaction of SOI and Domino Circuits

In almost every respect, SOI technology is identical to traditional bulk CMOS technology. The most striking difference is that the transistors are fabricated on a buried oxide layer. This provides a dramatic reduction in junction capacitance and results in a substantial increase in performance or a corresponding reduction in dynamic power consumption. By building the transistor on a buried oxide, each transistor is isolated electrically from the other transistors in the circuit. Whereas in bulk, the NFET devices share a common P well and PFET devices share an N well, each transistor body in SOI is now floating. As a consequence of the floating body in the SOI transistor, the body voltage can be raised in the static sense to a diode drop above the source node. For NFET transistors in which both the source and drain of a device are held at a voltage level approaching V_{dd}, the body voltage can (through diode leakage) approach V_{dd} as well. This is in stark contrast to bulk technology where the body is statically tied to either V_{dd} or ground through a well tie and this difference leads to several significant departures from traditional bulk transistor behavior.

Parasitic Bipolar Leakage (PBL) has been described in device and circuit literature [Wei96] [Pelella95] [Assaderaghi96]. In the case of an NFET transistor where the gate is held low, no charge beyond the sub-threshold leakage should pass between the source and the drain nodes. However, if the source and drain nodes

are held at a voltage approaching V_{dd} for a long period of time, the body node will eventually reach a voltage approaching V_{dd} as a result of junction leakage. If, subsequently, the source node is dropped to ground, a large forward bias will be seen across the source to body junction. This in turn leads to the injection of electrons into the body and this resulting current is analogous to emitter / base current in a bipolar transistor. Of the charge introduced into the body some fraction is consumed in electron-hole recombination, lowering the body voltage and terminating the leakage event. However, the remainder of the injected charge diffuses to the drain in the form of leakage. This current continues until the body voltage is lowered to within a diode drop of the source node. The leakage event can last in the order of a nS with peak currents in the order of 10's of uAs per micron of width of the offending transistor.

The resulting leakage is generally harmless in the context of static circuits, where a strong PFET network is always available to maintain the correct output. However, in domino circuits where the dynamic node is at times left floating (during the evaluate phase), this new form of leakage can discharge the node and lead to incorrect results. Transistor *N3* of Figs. 1 and 2 is susceptible to this SOI-specific leakage. For other domino configurations, where the drains of several transistors are connected to the dynamic node, the leakage can be seen on more than one transistor simultaneously. A domino OR gate is an example circuit where parallel transistors can be triggered together and for wide (more inputs) OR gates the problem can become even more significant.

By introducing a keeper device that can supply the charge withdrawn from the node by PBL, dynamic circuits fabricated in SOI can be designed to operate reliably in the fault-free case. However, faults that would otherwise be undetectable in domino circuits fabricated in bulk technology can now become manifest in SOI due to this new leakage source. Resistive shorts between the dynamic node and ground may not be detectable if the keeper transistor is capable of maintaining the dynamic voltage above the switching threshold of the output inverter. In SOI however, bipolar leakage can now contribute to the charge loss at the dynamic node and corrupt the output. Additionally, defects that render the keeper device ineffective are difficult to detect in bulk circuits with traditional test techniques. PBL provides a vehicle for exercising the keeper device without the introduction of extraneous test transistors, which degrade functional performance and increase circuit area.

4. Proposed PBL Test

Given that parasitic bipolar leakage in SOI can aggravate existing, previously undetectable faults, a new test sequence is required to exercise domino circuits under the worst-case leakage scenario. An SOI-specific test should be included to trigger the leakage event and then verify that the data at the output of the domino circuit is not corrupted. A test for the example domino AND gate is illustrated in Fig. 3 in both waveform and vector table format. In this case, the *A* input is held high long enough to charge the intermediate node between transistors *N2* and *N3* and then is deasserted for the remainder of the test. This allows the source to approach V_{dd} and begins the process of pre-conditioning the body node of *N3*. A preconditioning period must be sufficiently long to allow the body voltage of *N3* to rise to approximately V_{dd} through leakage currents in the source / body and drain / body junctions. Transistors *N1* and *N2* are then activated in the evaluate phase of the final test cycle. This results in forcing the source node of *N3* to the ground potential, which in turn, causes a forward bias across the source to body junction and initiates the bipolar leakage through transistor *N3* - potentially discharging the dynamic node if a defect is present.

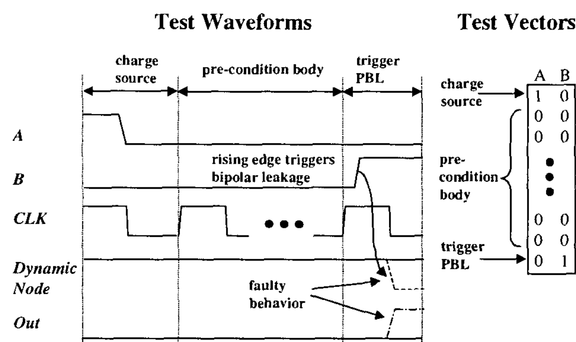

Figure 3. Proposed test sequence for domino AND gate

The environmental conditions (voltage and temperature) that the test should be executed under are process and design dependent. The worst-case scenario for the bipolar leakage in domino circuits is that which would maximize the bipolar leakage while reducing the drive capability of the keeper. Higher temperatures will reduce the ability of the keeper to replenish lost charge but will also reduce the beta of the parasitic bipolar transistor, thus reducing the leakage. Higher temperature may result in increasing other contributing leakages to provide an overall worst-case testing

environment. Similarly, a higher supply voltage increases the bipolar leakage, but also strengthens the keeper device. Simulations are required to identify the voltage and temperature that provide the worst-case scenario. In the next section, simulations are presented that help understand the tradeoffs between different voltages / temperatures.

5. Simulations

To understand the necessity of the PBL test, we simulated three circuits. Circuit 1 includes a fault-free domino circuit as shown in Fig. 2. In this case, the size of the keeper was selected to manage the bipolar leakage under all environmental / process corners. Consequently, this circuit would presumably never fail the proposed test sequence. Circuit 2 is the same circuit with the addition of a resistive short between the dynamic node and ground as depicted in Fig. 4.

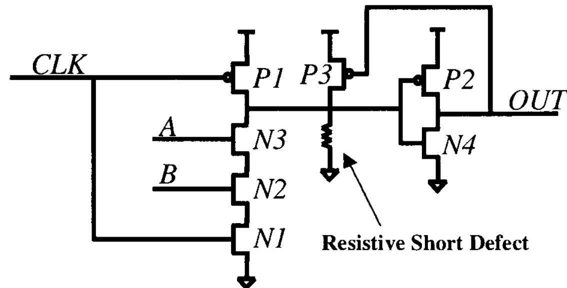

Figure 4. Circuit 2 - resistive short defect

In this case, the resistor and the keeper together make up effectively a voltage divider with the dynamic node as the output of the divider. Lower resistance values then tend to pull the dynamic node voltage lower. If the voltage drops below the switching threshold of the output inverter, the circuit will always evaluate to a logic high level regardless of the input values for both bulk and SOI. These defects can be detected with traditional tests even if they do not trigger PBL. However if the resistance value is high, then the defect is potentially undetectable without an additional aggravating mechanism. These higher resistance defects if undetected can cause reliability problems during the lifetime of the circuit.

The final circuit, circuit 3 shown in Fig. 5, was simulated with an open drain on the keeper, effectively removing the keeper functionality from the circuit. Without a leakage mechanism, traditional test vectors can not be guaranteed to detect this defect. A bleeder NFET can be included as a test vehicle to verify the keeper functionality, however this adds additional parasitic capacitance to the dynamic node and reduces performance [Adams98]. By triggering the bipolar leakage through the top transistor in the NFET network, a new controllable mechanism can be exploited to exercise the keeper and verify its existence, improving overall fault coverage.

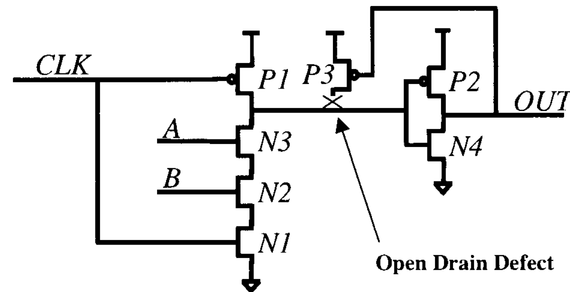

Figure 5. Circuit 3 - open drain defect on the keeper

The SOISPICE-5.0 circuit simulator created by SOI group at the University of Florida was used to simulate each of the three circuits using the test sequence described in the previous section. Circuit 1 evaluated correctly as expected. The keeper device replenished the charge lost due to the bipolar leakage and the dynamic node voltage was never reduced below the value of the switching threshold of the output inverter. Consequently, the output never incorrectly evaluates to a logic high value. Fig. 6 illustrates the waveforms. The dynamic node dips 300 mVs but never drops below the critical switching threshold. Eventually, the voltage is restored to V_{dd} due the charge introduced by the keeper.

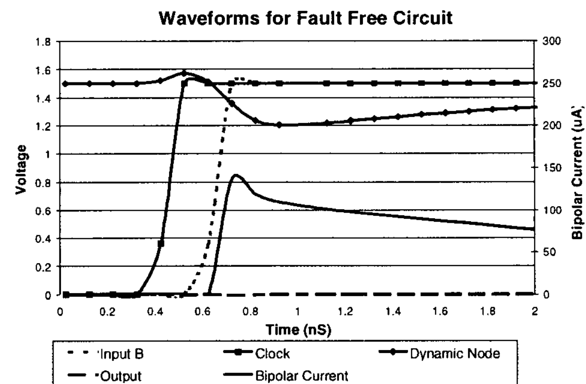

Figure 6. Waveforms of circuit 1 (Fault-Free)

Circuit 2 was simulated with both a conventional functional test that does not trigger PBL and the proposed test as stimulus. The waveforms for the

proposed test are illustrated in Fig. 7. As the Clock input is asserted, the large pre-charge PFET is turned off. This leaves only the small keeper transistors to hold the value on the dynamic node, which drops by 200 mVs. At this point, the domino circuit will still function, but is more sensitive to leakage. When the *B* input asserts, the source of the *N3* is driven to ground and a large pulse of bipolar leakage flows through *N3*, pulling the dynamic node down further and causing the gate to falsely evaluate to a logic high value.

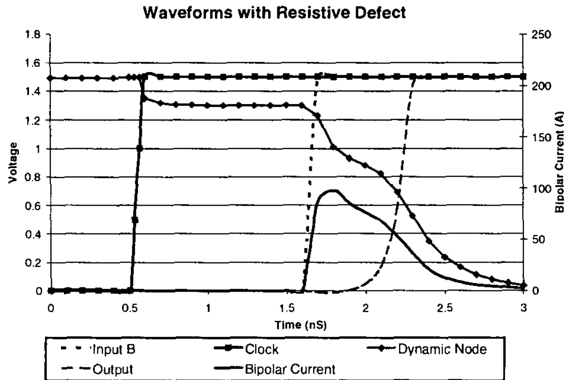

Figure 7. Waveforms of circuit 2 (resistive defect)

To identify the worst case temperature and voltage conditions for PBL, both parameters were varied and Figs. 8 and 9 show the resistance detected for temperature and voltage, respectively. In the case of Fig. 8, the sensitivity of the test increases significantly as the temperature is increased. This can be explained by the reduction in drive capability of the keeper. Prior to the PBL event, the dynamic node will drop to an equilibrium value determined by the voltage division of the keeper and the defect. At higher temperatures the effective resistance of the keeper will increase relative to the resistive defect and the dynamic node voltage will be reduced. This results in the circuit becoming more sensitive to noise. If the voltage is reduced below the switching threshold of the output inverter, traditional tests will detect the defect. Otherwise, the defect will not become manifest. In the case of the proposed PBL test, the leakage will reduce the voltage further providing an opportunity to detect the resistance. From Fig. 8, it becomes clear that the PBL test should be implemented at the highest specified temperature to gain the most sensitivity to resistive defects. Furthermore, the proposed test provides a significant increase in the ability at test to detect resistive defects when compared to traditional tests that do not trigger PBL.

The test sensitivity was measured across the specified supply voltage range and is depicted in Fig. 9. The

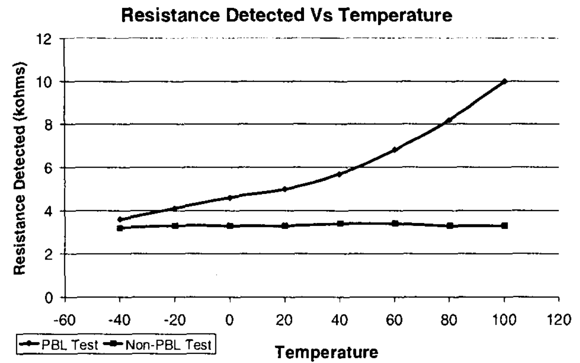

Figure 8. Resistance detected vs. temperature

ability to detect larger resistance values increases monotonically with V_{dd} for the PBL test, while the conventional functional test loses sensitivity at higher voltages. For the PBL case, this is explained by the increase in the body voltage prior to the PBL event due to the higher supply voltage. This results in a stronger forward bias across the source / body junction when the

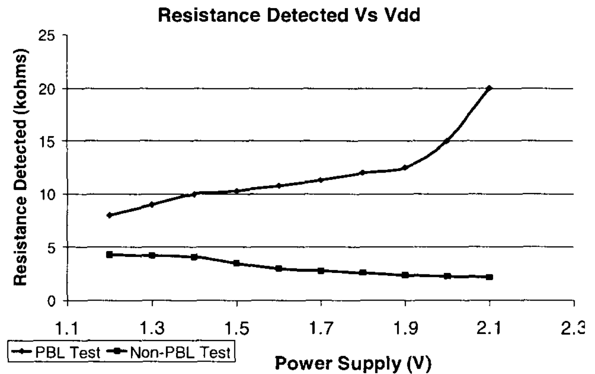

Figure 9. Resistance detected vs. supply voltage

source is brought to the ground potential producing a corresponding exponential increase in leakage. However, the keeper's drive capability is only increasing with a quadratic relationship to the supply voltage. Hence, the test will become more sensitive at higher voltages due to the mismatch between the leakage and the current of the keeper. In the case of the traditional functional test, no PBL event occurs and the sensitivity of the test is based only on the difference in the current drawn from the resistor – increasing linearly with V_{dd} - and the keeper increasing quadratically. Consequently, the sensitivity is decreased as the supply voltage is increased. Based on these results, PBL should be triggered at the highest specified voltage.

Circuit 3 was simulated demonstrating that without the keeper to replenish the charge lost to bipolar leakage, the circuit would fail under the high voltage/ temperature conditions. No traditional test can detect a missing keeper without the presence of some form of leakage. In bulk domino circuits, the only controllable way of testing the keeper is with the inclusion of a small NFET bleeder transistor, which would play the role of a leakage source during test operation, but otherwise would be inert during functional operation and quiescent current tests. However, this is generally not implemented in practice because of the associated performance and area penalty. In SOI, PBL can now be exploited to improve the test coverage for faults associated with the keeper. Circuit 3 only represented one possible fault (open drain), however, any fault that affects the drive capability of the keeper could be potentially detected with the PBL test. Other keeper-related faults would include an open source, a stuck-at 1 on the gate or a resistive fault (missing or partial vias) on the drain.

6. Conclusion

This paper has described a fault study of domino circuits fabricated in Partially-Depleted SOI and has demonstrated the need for an SOI-specific test that will trigger parasitic bipolar leakage. Although parasitic bipolar leakage can be accommodated for at design and fault-free circuits can be guaranteed to work under all specified conditions, it has been shown that certain defects, which were potentially undetectable in bulk technology, can now cause functional failures in domino circuits fabricated in SOI.

The PBL test eliminates these test escapes by providing worst-case leakage conditions and also increases overall fault coverage for domino circuits beyond that of conventional testing of traditional bulk technology. By exploiting the parasitic bipolar leakage, the sensitivity at test to resistive shorts on the dynamic node can be increased significantly and the presence of a keeper device can be verified without the need for extraneous test transistors. The test was simulated for two types of defects demonstrating the need for the technique and it was shown that high voltage and high temperature were the worst-case environmental conditions in which to implement the test.

SOI will continue to garner attention as the best candidate for the next generation of VLSI technology and domino circuit styles will become increasingly more popular in high performance IC's. The combination of the two then is inevitable. The interactions between SOI and dynamic circuits are well understood and the associated problems can be avoided for fault-free circuits. However, for manufactured circuits where defects are unavoidable, new test techniques, such as the one proposed, will be required.

Acknowledgements

The authors would like to thank Dr. Jerry Fossum for the availability of the SOISPICE 5.0 SOI transistor models used in this study.

References

[Adams98] R. D. Adams, "Fault Modeling and Design of Dynamic Logic", Ph.D. Dissertation, Dartmouth College, 1998.

[Assaderaghi96] F. Assaderaghi, G. Shahidi, L. Wagner, M. Hsieh, M. Pelella, S. Chu, R. Dennard, B. Davari, "Accurate Measurement of Pass-Transistor Leakage Current in SOI MOSFETs", *IEEE International SOI Conference*, pp. 66-67, 1996.

[Chuang98] C.T. Chuang, P.-F. Lu, C.J. Anderson, "SOI for Digital CMOS VLSI: Design Considerations and Advances", *Proceedings of the IEEE*, pp. 689-720, April, 1998.

[Krishnan98] S. Krishnan, J. Fossum, "Grasping SOI Floating-Body Effects", *Circuits and Systems*, pp. 32-37, July 1998.

[Nowka98] K. Nowka, T. Galambos, "Circuit Design Techniques for a Gigahertz Integer Microprocessor", *Proc. of International Conference on Computer Design*, pp. 11-16, 1998.

[Pelella95] M. Pelella, J. Fossum, D. Suh, S. Krishnan, K. Jenkins, "Low-Voltage Transient Bipolar Effect Induced by Dynamic Floating-Body Charging in PD/SOI MOSFETs", *Proc. of IEEE International SOI Conference*, pp. 8-9, 1995.

[Shahidi98] G. Shahidi, A. Ajmera, F. Assaderaghi, R. Bolam, H. Hovel, E. Leobandung, W. Raush, D. Sandana, D. Schepis, L. Wagner, L. Wissel, K. Wu, B. Davari, "Device and Circuit Issues in SOI Technology", *Proc. of IEEE Custom Integrated Circuits Conference*, pp. 339-346, 1998.

[Srivastava91] P. Srivastava, A. Pua, L. Welch, "Issues in the Design of Domino Logic Circuits", *Proc. of 8th Great Lakes Symposium on VLSI*, pp.108-115, 1998.

[Wei96] A. Wei, D. Antoniadis, "Measurement of Transient Effects in SOI DRAM/SRAM Access Transistors", *IEEE Electron Device Letters*, vol. 17, no. 5, pp. 193-195, May, 1996.