# Inserting Test Points to Control Peak Power During Scan Testing

Ranganathan Sankaralingam and Nur A. Touba

Computer Engineering Research Center
Department of Electrical and Computer Engineering
University of Texas, Austin, TX 78712
{ranga,touba}@ece.utexas.edu

## *Abstract*

*This paper presents a procedure for inserting test points at the outputs of scan elements of a full-scan circuit in such a manner that the peak power during scan testing is kept below a specified limit while maintaining the original fault coverage. If the power in a clock cycle during scan testing exceeds a specified limit (which depends on the peak power the chip has been designed to supply), a "peak power violation" is said to occur. Given a set of vectors, simulation is used to identify the cycles in which peak power violations occur (called "violating cycles"). For each violating cycle, the reduction in power caused by a control-0 and control-1 test point at each scan element is determined by simulation. The optimization problem then is to select as few test points as possible to eliminate all violating cycles. We present a heuristic procedure for minimizing the number of test points using integer linear programming techniques. The test points are activated and deactivated in a manner such that there is neither any loss in fault coverage nor peak power violations in the capture cycle. Experimental results indicate that the proposed procedure is very effective in controlling peak power during scan testing using a small number of test points.*

## 1. Introduction

The peak power drawn in a single clock cycle during scan testing can be much larger than during normal operation. During normal circuit operation, typically a relatively small percentage of the flip-flops change value in each clock cycle. However, when scanning in test vectors, typically a much larger percentage of the flip-flops will change value in each clock cycle resulting in excessive switching activity in the circuit. If a large number of flip-flops switch simultaneously in a clock cycle, it is likely that a large number of internal nodes will switch as well, resulting in a large current spike. A chip's power supply/ground pins and distribution system may be designed for handling the peak power during normal operation, and it may not be able to handle the large peak power that could occur during scan testing. If the peak power during test is too large, then there will be a $V_{dd}$ drop/ground bounce that may cause problems (e.g., memory elements may lose their state or a phase-lock loop may malfunction). With the rapid increase in chip complexity, the problem of excessive peak power during scan testing is becoming an important issue in industry.

The average power dissipation during scan testing can be controlled by reducing the scan frequency. However, the peak power during scan testing cannot be controlled by reducing clock frequency and hence is more difficult to control. Moreover, controlling peak power requires ensuring that the peak power dissipation in any single clock cycle does not exceed the capabilities of the chip, which is more difficult than simply reducing the average power dissipation per clock cycle.

Proceedings of the 17th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'02)
1063-6722/02 $17.00 © 2002 **IEEE**

## 1.1 Previous Work

Previous work in low power scan testing has mostly focused on the problem of controlling heat dissipation by reducing the average power dissipation during scan testing [Wang 94, 97ab, 99], [Dabholkar 98], [Girard 99a], [Sankaralingam 00, 01] (see [Bonhomme 02] for a survey). These techniques are applicable in cases where the heat dissipation during testing exceeds the package's limit.

Some design-for-test (DFT) techniques reduce peak power in addition to average power. In [Whetsel 00], an adapted scan chain architecture that segments a single scan chain to minimize switching activity during scan shifting is proposed. This approach greatly reduces average power and can avoid peak power problems during scan shifting, but requires additional DFT hardware. In [Lee 00], a method for adding delay elements to interleave the capture cycles for multiple scan chains is proposed for reducing peak power during scan capture. In [Girard 99b], a technique for reducing peak power during built-in self-test (BIST) is proposed which involves partitioning a circuit and performing separate BIST sessions on each partition. In [Corno 99], a technique for modifying test sequences for sequential non-scan testing is proposed for reducing peak power.

In [Hertwig 98] and [Gerstendörfer 99], logic is added to hold the output of all scan cells at a constant value during scan shifting thereby reducing power dissipation. This approach greatly reduces average power, and will avoid peak power problems during scan shifting, but will not help with peak power problems during the capture cycle. The peak power in the capture cycle can be very high since all the inputs will simultaneously switch from the constant value to the value specified by the vector (see results in [Basturkmen 02]). A drawback of this approach is that it degrades circuit performance because it adds extra logic to the functional path of all scan elements.

In [Sankaralingam 02], a method is proposed to modify the vectors of a deterministic test set by reassigning certain bits of the test vectors to make sure that the peak power is below a user-specified threshold. This is done without reducing the fault coverage or adding DFT hardware.

In [Basturkmen 02], a method to reduce peak power during BIST is proposed. Scan chains are grouped into units called *scan groups*. In any test cycle, only a single scan group shifts or captures data, hence reducing peak power. A significant increase in test time is required in order to maintain fault coverage while simultaneously reducing peak power.

## 1.2 Proposed Work

In this paper, a procedure is proposed for inserting test points into a conventional full-scan circuit so that the peak power during scan testing is kept below a specified limit while maintaining the same fault coverage. Given a set of scan vectors that have peak power violations during scan testing, simulation can be done to identify the cycles in which violations occur. The number of transitions being injected into the combinational part of the circuit because of transitions in the scan elements due to shifting can be reduced if control-0 and control-1 test points are placed at the outputs of some scan elements.

A heuristic procedure for inserting a minimal number of test points to eliminate all violations is presented. The procedure is based on integer linear programming techniques. The procedure can avoid test points on scan elements in the critical path of the circuit. A special signaling scheme for controlling the test points to avoid peak power problems when the test points are activated and deactivated is proposed.

Note that whereas the method in [Gerstendörfer 99] uses a scan architecture in which a control-0 point is effectively placed at the output of all scan elements, the proposed method inserts test points on only a subset of the scan elements and both control-0 and control-1 points

are considered. While the method in [Gerstendörfer 99] targets average power, the proposed method targets peak power.

## 2. Overview of proposed scheme

The model of power consumption used here is a zero-delay, weighted transition model. When an internal node changes state, power is consumed. The transition is weighted by the number of fanouts of the node. The power consumed in a cycle is approximated by summing the weighted transitions of all nodes in the circuit. *Peak power* is the maximum of the number of weighted transitions in a single cycle, over all cycles in the test session. Note, however, that the proposed method can be used with other power consumption models.

As a vector is scanned into the circuit though a mux-D scan cell, the value in the flip-flop is applied to the combinational part of the circuit. During scan shifting, a large number of scan elements may change state in every shift cycle, injecting a large number of transitions into the combinational part of the circuit. However in functional mode, typically, only a very small number of the flip-flops change state every cycle. Hence the peak power in a test session can much greater than that during functional mode. Power consumption can be reduced by reducing the number of transitions being injected into the combinational part of the circuit during shift cycles through the scan elements.

An effective way to reduce the number of transitions injected during shift cycles is to add test points to a subset of the scan elements to hold the output of the flip-flop at a constant value during shift cycles. Inserting control-0 and control-1 test points at the output of a mux-D scan element results in the scan elements shown in Fig. 1.

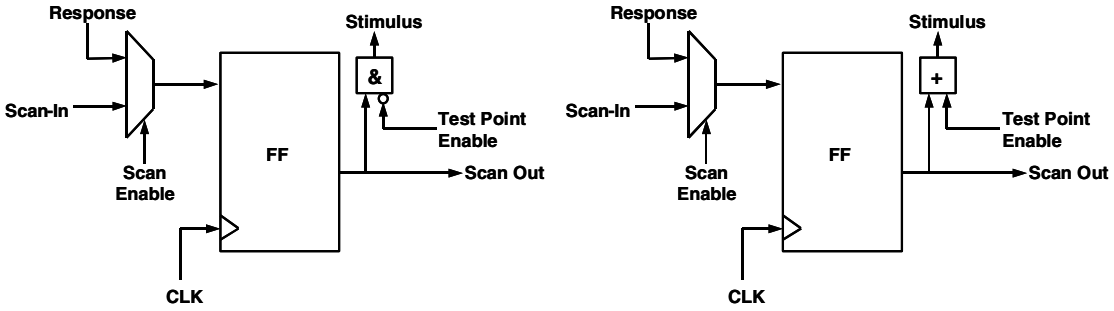


Figure 1. Mux-D scan element with control-0 test point (left) and control-1 test point (right)

The ***Test Point Enable*** signal is activated during scan shifting to prevent changes in the value of the flip-flop from propagating into the combination part. It is deactivated in the capture cycle to apply the values specified by the test vector to the combinational part. The protocol for activating and deactivating ***Test Point Enable*** will be explained in detail in Sec. 5.

## 3. Problem formulation

In this section, we describe how integer linear programming can be used to select test points to eliminate a given set of violating cycles.

### 3.1 Mapping to integer linear programming

Given a test set and circuit, we do cycle-by-cycle simulation of all cycles in the test session to calculate the power consumed in every clock cycle. The user specifies a limit on peak power. All cycles with power consumption greater than the specified limit are termed *violating cycles*. The goal is to insert control-0 and control-1 test points at the output of as few scan elements as possible to eliminate the violating cycles. Clearly, this is an optimization problem in which we attempt to minimize the number of test points.

There are two candidate test points per scan element, since we can insert either a control-0 test point or a control-1 test point at that scan element. For each candidate test point, we estimate the reduction in power caused by that test point by simulating the independent insertion of that test point during the test session. If there are $N_v$ violating cycles and $2S$ candidate test points (i.e. $S$ scan elements), we get the reduction in power when each of the $2S$ test points is independently inserted in the $N_v$ violating cycles. We use an event-driven, selective trace simulation procedure to estimate the power reduction [Ulrich 94]. This process is fast since this method does not result in evaluating the whole circuit and also because only a small fraction of the total cycles are violating cycles.

An $N_v$ by $2S$ matrix $\boldsymbol{A}$ can be formed where each column corresponds to one of the $2S$ candidate test points and each row corresponds to one of the $N_v$ violating cycles. Each element in the matrix $A(r,2i)$ gives the reduction in power when a control-0 test point is inserted at the $i^{\text{th}}$ scan element for the $r^{\text{th}}$ violating cycle. $A(r,2i+1)$ gives the reduction for a control-1 test point.

Each of the test points can either be selected or not selected. The optimization problem is to decide which test points to select. Since we have $2S$ candidates, we need $2S$ variables. Let $\boldsymbol{x}$ be a $2S$-sized column vector of variables which is used to represent which of the candidate test points are selected in the optimal solution. The elements of $\boldsymbol{x}$ can be either 0 or 1. $x(j)$ is 1 if the $j^{\text{th}}$ test point is selected and 0 otherwise.

We select test points to satisfy the condition that the power consumed in all cycles should be under a specified limit, $L$. For each violating cycle, during simulation we can calculate by how much the power consumption exceeds the limit. These values can be put in a column vector. For $N_v$ violating cycles, an $N_v$-sized column vector $\boldsymbol{R}$ results.

We assume that if two test points are selected, the resulting reduction in power is the sum of the reductions due to each. In general, this is not true and Sec. 4 gives a procedure to deal with this. The goal is to select as few test points as possible such that the reduction due to these test points is greater than the required reduction. Given the matrices $\boldsymbol{A}$, $\boldsymbol{x}$ and $\boldsymbol{R}$, the conditions that the optimal solution must satisfy to eliminate all violating cycles is given by the following inequality:

$$\boldsymbol{A}\boldsymbol{x} \geq \boldsymbol{R}$$

This is an optimization problem where the objective is to minimize $\Sigma x(j)$. The constraints on the optimal solution are linear equations in $x(j)$. Since the variables in $\boldsymbol{x}$ are restricted to taking values 0 or 1, this is an integer linear program.

Consider the following example where a circuit has 4 scan elements (i.e., $S=4$) and 5 violating cycles (i.e., $N_v=5$). We would get a matrix $\boldsymbol{A}$ with 5 rows and 8 columns. The power reduction for each candidate test point is shown below. Let the required reduction in power for this example be $\boldsymbol{R} = [8, 22, 40, 1, 20]$.

Table 1. Reduction in power due to each test point candidate

| | *c-0 at scan element 0* | *c-1 at scan element 0* | *c-0 at scan element 1* | *c-1 at scan element 1* | *c-0 at scan element 2* | *c-1 at scan element 2* | *c-0 at scan element 3* | *c-1 at scan element 3* |
|---|---|---|---|---|---|---|---|---|
| Violating Cycle 1 | 10 | 20 | 11 | 0 | 5 | 5 | 23 | 2 |
| Violating Cycle 2 | 12 | 15 | 0 | 13 | 14 | 21 | 34 | 43 |
| Violating Cycle 3 | 6 | 27 | 33 | 23 | 4 | 9 | 15 | 32 |
| Violating Cycle 4 | 15 | 29 | 13 | 22 | 19 | 17 | 2 | 15 |
| Violating Cycle 5 | 22 | 12 | 7 | 14 | 20 | 47 | 3 | 16 |

The procedure is stated as pseudo-code below:

*For each violating cycle* $VC_c$, c = 1..Nv
  Pow = *Num. Weighted Transitions*
  R(c) = L – Pow
  *For each scan element* $S_i$, *i* = 1..S
    *Simulate circuit with* $S_i$ = S0  *// Try control-0 test point*
    A(c,2i) = Pow – *Num. Weighted Transitions*
    *Restore State*
    *Simulate circuit with* $S_i$ = S1  *// Try control-1 test point*
    A(c,2i+1) = Pow – *Num. Weighted Transitions*
    *Restore State*
  *EndFor*
*EndFor*

### 3.2 Preventing conflicts in test point selection

The optimization condition as stated above does not prohibit selection of both a control-0 and control-1 test point at the same scan element. This would happen if both *x(2i)* and *x(2i+1)* were set to 1 in the optimal solution.

Prohibiting such cases can be easily accomplished by adding more conditions. Let $S_i$ be the $i^{th}$ scan element. We can express the condition that if selected, $S_i$ should be selected either as a control-0 or control-1 test point, but not both, as $x(2i) + x(2i+1) \leq 1$. Negating throughout, we get $-x(2i) - x(2i+1) \geq -1$. Making sure that this condition is satisfied can be accomplished by adding an extra row to $\boldsymbol{A}$ with –1 in columns *2i* and *2i+1* and 0 elsewhere. An extra corresponding row is added to $\boldsymbol{R}$ containing –1. Since there are *S* scan elements, *S* extra conditions result.

For the example shown above, the inequalities are shown inFig. 2. The rows with $\boldsymbol{R}$ set to –1 are those that were added to prevent both control-0 and control-1 test points at the same scan element.

$$\begin{bmatrix} 10 & 20 & 11 & 0 & 5 & 5 & 23 & 2 \\ 12 & 15 & 0 & 13 & 14 & 21 & 34 & 43 \\ 6 & 27 & 33 & 23 & 4 & 9 & 15 & 32 \\ 15 & 29 & 13 & 22 & 19 & 17 & 2 & 15 \\ 22 & 12 & 7 & 14 & 20 & 47 & 3 & 16 \\ -1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \\ x_8 \end{bmatrix} \geq \begin{bmatrix} 8 \\ 22 \\ 1 \\ 20 \\ -1 \\ -1 \\ -1 \\ -1 \end{bmatrix}$$

Figure 2. Inequalities for the example

### 3.3 Avoiding test points on critical paths

In certain scan elements are known to be on the critical path, it is very easy to prevent test points from being inserted on those scan elements. If scan element $S_i$ is on the critical path, simply setting $2i^{th}$ and $(2i+1)^{th}$ columns in all rows of $\boldsymbol{A}$ to zero will prevent that scan element from being selected for test point insertion.

## 4. Selection of test points

In principle, a solution to eliminate all violating cycles can be derived by just giving the integer linear programming (ILP) solver the matrices $\boldsymbol{A}$ (which contains the estimates of power reductions of the candidate test points) and $\boldsymbol{R}$ (which contains the required power reductions). However, if $\boldsymbol{A}$ has a very large number of rows and columns (corresponding to a large number of violating cycles and scan elements), the ILP solver may require large amounts of memory and take an unacceptably long time to solve the optimization problem. To reduce run time and memory requirements, we adopt the heuristic procedure described below.

Let us derive new matrices $\boldsymbol{A_K}$ and $\boldsymbol{R_K}$, which contain the data corresponding to the top $K$ of the violating cycles, with the violating cycles sorted in decreasing order of required power reduction. The number $K$ should be chosen such that the resulting matrices $\boldsymbol{A_K}$ and $\boldsymbol{B_K}$ can be solved by the ILP solver in a reasonable amount of time. Fixing these violating cycles requires that $\boldsymbol{A_K x} \geq \boldsymbol{R_K}$. If $K$ is much smaller than the total number of violating cycles, the size of the new problem is much smaller the original one. The ILP solver will be able to solve this problem much more quickly. Let $\boldsymbol{x_K}$ be the set of test points the IP solver returns. The reason behind targeting the top $K$ violating cycles is that test points that solve the power problem for high-power vectors are also likely to solve the power problems of many more violating cycles with less power consumption.

We insert the test points of $\boldsymbol{x_K}$ into the circuit and simulate all test cycles again. For violating cycles that still remain, we simulate the independent insertion of all test points not already selected by $\boldsymbol{x_K}$. This procedure results in two new matrices $\boldsymbol{A_2}$ and $\boldsymbol{R_2}$. Since many of the violating vectors not explicitly targeted by $\boldsymbol{x_K}$ would have been eliminated, $\boldsymbol{A_2}$ and $\boldsymbol{R_2}$ and are usually much smaller than $\boldsymbol{A}$ and $\boldsymbol{R}$ (10-30 times smaller). If $\boldsymbol{A_2}$ and $\boldsymbol{R_2}$ are sufficiently small, the problem can be solved in its entirety. Otherwise the top $K'$ violating cycles from $\boldsymbol{A_2}$ and $\boldsymbol{R_2}$ can be extracted to derive some more test points. This process is repeated until all violating cycles are eliminated.

The elements of $\boldsymbol{A}$, which are the estimates for the power reduction produced by the candidate test points, are accurate only if the candidate test point is the only one present. While solving the optimization problem, if selecting one test point is not enough to fix all peak power violations, multiple test points are selected. The assumption that is made is that the power reduction of a set of test points is equal to sum of the reduction due to each test point in the set. If some violating cycles are not eliminated, we add more test points to eliminate them. While performing simulation to estimate the power reduction of new test points, the presence of already-inserted test points is accounted for. Hence the accuracy of later iterations is more than that of earlier iterations.

## 5. Scheme for activating and deactivating test points

The test points fix the outputs of certain scan elements to a constant value if ***Test Point Enable*** is active. However to prevent a decrease in fault coverage, the values applied to the circuit under test during the capture cycle should be the same values that are specified by the vector. In order to accomplish this, the test points should be deactivated in the capture cycle. It should be set to logic 1 for as many cycles as possible to maximize peak power reduction.

### 5.1 Adapting conventional scan in the presence of test points

For the proposed scheme, the ***Test Point Enable*** signal should be logic 0 during the capture cycle. This can be accomplished by setting ***Test Point Enable*** to logic 0 in the last shift cycle. This will ensure that the values that are applied to the circuit under test. The signaling scheme used during full-scan adapted to deal with test points is shown in Fig. 3.

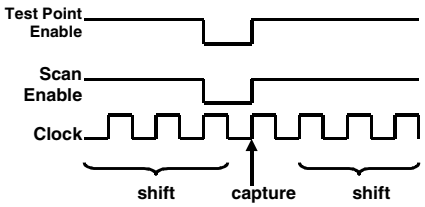


Figure 3. Clocking scheme with test points present

The advantage of this scheme is that there no extra test cycles are needed to accommodate the presence of test points and not much extra logic is required since the ***Scan Enable*** signal can be connected to ***Test Point Enable*** in all scan elements. However, in the last shift cycle transitions are injected into the circuit due to two reasons. Some transitions are injected into the circuit due to transitions in the scan chains due to the last shift cycle. In addition to this, the test points are deactivated, due to which some scan elements switch from a constant 1/0 to the value specified in the test vector. Because of this some more transitions are injected into the circuit. The reason some scan elements were candidates for insertion of test points is that inhibiting transitions on those scan elements results in a large reduction in power consumption. Hence transitions in those scan elements in addition to the transitions due to the scan chain shifting can result in a peak power violation in the last shift cycle. A similar argument applies to the first shift cycle after the capture cycle, where transitions due to the first shift and those due to test point activation are injected into the circuit.

## 5.2 Preventing violations in last and first shift cycles

To prevent peak power violations, the last shift before the capture cycle must be decoupled from the test point deactivation and the first shift cycle after the capture cycle must be decoupled from test point activation to prevent peak power violations. We propose the clocking scheme shown in Fig. 4 to avoid peak power problems in the capture cycle. In this scheme, test points are deactivated one cycle after the last shift. The extra clock cycle delay is to allow the change in inputs due to the last shift to propagate through the combinational logic before the test points are deactivated. This decouples the two sources of transitions in the circuit so that they don't occur in the same cycle where they may cause peak power violations. The same idea is used for activating the test points after the capture cycle. An extra cycle is placed after the capture cycle to decouple the activation of the control points.

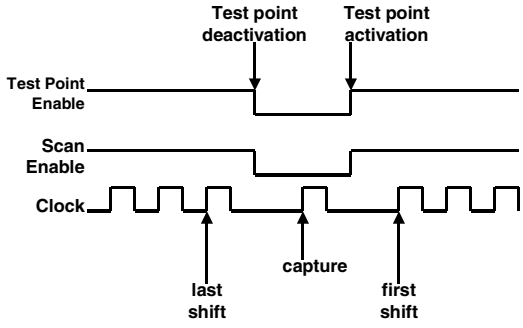


Figure 4. Clocking scheme to avoid power problems in capture cycles

Note that the architecture described here does not suffer from the problem of excessive power consumption in capture cycles in [Gerstendörfer 99]. Since only a subset of the scan elements transition from a fixed value to the vector-specified value during test point activation and deactivation, the power consumed is much lower than would be the case if all switched.

### 5.3 Test time overhead

Typically there are hundreds of scan shifts for every capture cycle. Most of the test time is spent in scan shifting. The overhead of this scheme is two cycles for every capture cycle. Hence the extra test time required for this scheme is very small compared to the total test time.

### 5.4 Implementation of proposed scheme

The implementation of the proposed scheme is very simple. The ***Scan Enable*** signal and the ***Test Point Enable*** signal can be made identical as illustrated in Fig. 3 and Fig. 4. Hence ***Test Point Enable*** is simply connected to ***Scan Enable*** and there is no need to route a separate global signal for it. Since the tester controls the clock signal of the circuit-under-test, the proposed clocking sequence can be easily implemented in the tester program.

## 6. Experimental Results

We implemented the proposed method on several of the largest ISCAS-89 benchmark circuits. We assumed a conventional full scan architecture. The primary inputs of the circuit were also assumed to be part of the scan chain. We generated test vectors for the full-scan versions of the circuits using a commercial automatic test pattern generation (ATPG) tool. The unspecified values in the test cubes from the ATPG tool were filled such that the number of transitions during scan-in would be as low as possible (i.e., minimum-transition fill [Sankaralingam 00]). Simulation was done to identify the violating cycles and the power reduction due to the candidate test points. A commercial ILP solver was used to select test points. Simulation and the ILP solver were used together to eliminate all violating cycles as described in Sec. 5. Test points were inserted to reduce the peak power of the ATPG generated test set by 30%. There was no increase in the number of vectors in the test set or decrease in fault coverage.

Table 2. Results for ISCAS89 benchmarks for 30% reduction in peak power

| Circuit | Percent. Violating Cycles | Percent. Violating Vectors | Num. Scan Elements | **Num. Test Points** | **Decrease in Peak Power** | Decrease in Average Power |
|---|---|---|---|---|---|---|
| s5378 | 70% | 100% | 216 | **23** | **30%** | 27% |
| s9234 | 16% | 100% | 247 | **15** | **30%** | 29% |
| s13207 | 8% | 75% | 700 | **42** | **30%** | 29% |
| s15850 | 10% | 66% | 611 | **8** | **30%** | 32% |
| s38417 | 8% | 27% | 1664 | **119** | **30%** | 33% |

The experimental results are shown in Table 2. The first column shows the name of the benchmark circuit. The second column gives the percentage of cycles that violated the peak power constraint among all test cycles. As can be seen, the percentage of cycles is small in most cases. The third column shows the percentage of test vectors which had at least one violating cycle during scan-in of that vector. As can be seen, a very large number of vectors have at least one violating cycle. This is because the small number of violating cycles are distributed over a large number of vectors. If a simple approach like dropping all vectors with violating cycles were resorted to, a significant decrease in fault coverage would result since a significant number of vectors would need to be dropped. The fourth column shows the number of scan elements in the circuit. The fifth column shows the number of scan elements that were converted to test points. This column gives the number of test points that were necessary to reduce peak power by 30%. The sixth column gives the reduction in average power. As can

be seen, the reduction in average power is not as much as reported in [Gerstendörfer 99] since the number of test points is much lower. However, the reduction in peak power is much greater than the reduction in peak power for that scheme. Using a small number of test points prevents large power consumption in capture cycles, which happens in [Gerstendörfer 99].

## 7. Conclusions

Peak power during testing can be reduced by inserting test points at the outputs of a few scan elements in a conventional full-scan circuit. Significant reductions in peak power with a small number of test points are possible. It is very easy to prohibit test point insertion on scan elements on the critical path. Test set size and fault coverage are both unaffected. A test point activation scheme with a very small test time overhead is proposed to prevent peak power problems in the cycles immediately preceding and succeeding the capture cycle.

## Acknowledgements

This material is based on work supported in part by the National Science Foundation under Grant No. MIP-9702236 and in part by the Texas Advanced Technology Program under Grant No. 003658-0644-1999.

## References

[Basturkmen 02] Basturkmen, N. Z., S. M. Reddy, and I. Pomeranz, "A Low Power Pseudo-Random BIST Technique," *Proc. of International Conference on Computer Design*, 2002.

[Bonhomme 02] Bonhomme, Y., P. Girard, C. Landrault, S. Pravossoudovitch, "Test power: a big issue in large SOC designs," *Proc. of IEEE Intl. Workshop on Electronic Design, Test and Applications*, pp. 447-449, 2002.

[Corno 99] Corno, F., M. Rebaudengo, M. Sonza Reorda, M. Violante, "On Reducing the Peak Power Consumption of Test Sequences," *European Conference on Circuit Theory and Design*, pp. 247-250, 1999.

[Dabholkar 98] Dabholkar, V., S. Chakravarty, I. Pomeranz, and S.M. Reddy, "Techniques for Minimizing Power Dissipation in Scan and Combinational Circuits During Test Application," *IEEE Trans. on Computer-Aided Design*, Vol. 17, No. 12, pp. 1325-1333, Dec. 1998.

[Gerstendörfer 99] Gerstendörfer, S., and H.-J. Wunderlich, "Minimized Power Consumption for Scan-Based BIST," *Proc. of International Test Conference*, pp. 77-84, 1999.

[Girard 99a] Girard, P., L. Guiller, C. Landrault, and S. Pravossoudovitch "A Test Vector Inhibiting Technique for Low Energy BIST Design," *Proc. of VLSI Test Symposium*, pp. 407-412, 1999.

[Girard 99b] Girard, P., L. Guiller, C. Landrault, and S. Pravossoudovitch "Circuit Partitioning for Low Power BIST Design with Minimized Peak Power Consumption," *Proc. of Asian Test Symposium*, pp. 89-94, 1999.

[Goel 81] Goel, P., "An Implicit Enumeration Algorithm to Generate Tests for Combinational Logic Circuits," *IEEE Trans. on Computers*, Vol. C-30, No. 3, pp. 215-222, Mar. 1981.

[Hertwig 98] Hertwig, A., and H.-J. Wunderlich, "Low Power Serial Built-In Self-Test," *Proc. of European Test Workshop*, pp. 49-53, 1998.

[Lee 00] Lee, K.-J., T.-C. Huang, and J.-J. Chen, "Peak-Power Reduction for Multiple-Scan Circuits during Test Application," *Proc. of Asian Test Symposium*, pp. 453-458, 2000.

[Sankaralingam 00] Sankaralingam, R., R.R. Oruganti, and N.A. Touba, "Static Compaction Techniques to Control Scan Vector Power Dissipation", *Proc. of VLSI Test Symposium*, pp. 35-40, 2000.

[Sankaralingam 01] Sankaralingam, R., B. Pouya, and N.A. Touba, "Reducing Power Dissipation During Test Using Scan Chain Disable", *Proc. of VLSI Test Symposium*, pp. 319-324, 2001.

[Sankaralingam 02] Sankaralingam, R., and N.A. Touba, "Controlling Peak Power During Scan Testing", *Proc. of VLSI Test Symposium*, pp. 153-159, 2002.

[Ulrich 94] Ulrich, E. G., V. D. Agrawal, J. H. Arabian, "Concurrent and Comparative Discrete Event Simulation", Kluwer Academic Publishers, 1994.

[Wang 94] Wang, S., and S.K. Gupta, "ATPG for Heat Dissipation Minimization during Test Application," *Proc. of International Test Conference*, pp. 250-258, 1994.

[Wang 97a] Wang, S., and S.K. Gupta, "DS-LFSR: A New BIST TPG for Low Heat Dissipation," *Proc. of International Test Conference*, pp. 848-857, 1997.

[Wang 97b] Wang, S., and S.K. Gupta, "ATPG for Heat Dissipation Minimization for Scan Testing," *Proc. of Design Automation Conference*, pp. 614-619, 1997.

[Wang 99] Wang, S., and S.K. Gupta, "LT-RTPG: A New Test-Per-Scan BIST TPG for Low Heat Dissipation," *Proc. of International Test Conference*, pp. 85-94, 1999.

[Whetsel 00] Whetsel, L., "Adapting Scan Architectures for Low Power Operation," *Proc. of International Test Conference*, pp. 863-872, 2000.