Logic BIST Architecture Using Staggered Launch-on-Shift for Testing Designs Containing Asynchronous Clock Domains

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Abstract—**This paper presents a new at-speed logic *built-in self-test* (BIST) architecture using staggered launch-on-shift (LOS) for testing a scan-based BIST design containing asynchronous clock domains. The proposed approach can detect inter-clock-domain structural faults and intra-clock-domain delay and structural faults in the BIST design. This solves the long-standing problem of using the conventional one-hot LOS approach that requires testing one clock domain at a time which causes long test time or using the simultaneous LOS approach that requires adding capture-disabled circuitry to normal functional paths across interacting clock domains which causes fault coverage loss. Given a fixed number of BIST patterns, experimental results showed that the proposed staggered clocking scheme can detect more faults than one-hot clocking and simultaneous clocking.**

Keywords—staggered launch-on-shift, staggered launch-on-capture, single-capture, double-capture

I. INTRODUCTION

Logic *built-in self-test* (BIST) [1, 2] is a *design-for-testability* (DFT) technique in which a portion of a circuit on a chip, board, or system is used to test the digital logic circuit itself. Logic BIST is crucial for many applications, in particular, for life-critical and mission-critical applications. These applications are commonly found in aerospace/defense, automotive, banking, computer, medical, networking, and telecommunications industries, which require on-chip, on-board, in-system, and in-field self-test to improve the reliability of the entire system, as well as the ability to perform remote test and diagnosis. Logic BIST has also proved to be beneficial for consumer electronics applications, in that it helps significantly reduce the manufactured devices' defect level as the process technology moves toward 65 nm and below.

The logic BIST technique widely used in the industry is based on the *Self-Test Using a MISR and Parallel Shift register sequence generator* (**STUMPS**) structure [3]. In the STUMPS architecture, a *pseudo-random pattern generator* (**PRPG**) is used to generate pseudo-random patterns and shift each pattern in parallel to the inputs of scan chains embedded in a scan-based design and a *multiple-input signature register* (**MISR**) is used to compact the test responses shifted out of the scan chain outputs to create a *signature*. After a pre-determined number of test cycles are executed, the final signature is then compared against an embedded golden (good circuit) signature to judge whether the *circuit under test* (CUT) passes or fails. As no test patterns are supplied externally, logic BIST can reduce test cost and also allow the circuit to perform self-test in the field.

While logic BIST offers many benefits, its real value is in providing at-speed testing for high-speed and high-performance circuits. These circuits often contain multiple clock domains, each running at a frequency that is either synchronous or asynchronous to the other clock domains. Two clock domains are said to be **synchronous** if the active edges of both clocks controlling the two clock domains can be aligned precisely or triggered simultaneously. Two clock domains are said to be **asynchronous** if they are not synchronous.

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Despite its conceptual simplicity, logic BIST faces many practical hurdles, especially in at-speed testing for multi-clock, multi-frequency circuits. Each clock in such a circuit controls a clock domain, whose clock skew is minimized and which runs at a frequency either synchronous or asynchronous to other clock domains. The most critical yet difficult part of logic BIST is how to detect intra-clock-domain faults and inter-clock-domain faults thoroughly and efficiently with a proper capture-clocking scheme.

Previous STUMPS-based logic BIST schemes proposed in [4-6] have not been effectively applied in practice. The reason is mainly due to the need to manipulate test frequency when the CUT contains asynchronous clock domains. The problem of testing intra-clock-domain faults within each asynchronous clock domain at-speed can be solved by using the conventional **one-hot clocking** approach that tests one asynchronous clock domain at a time. This approach results in long test time. Another approach is to use the **simultaneous clocking** approach that tests all asynchronous clock domains simultaneously. This approach, however, requires adding isolation logic among interacting clock domains that causes fault coverage loss across the interacting clock domain logic blocks through which data are not allowed to propagate. Both approaches can adopt the basic ***launch-on-capture*** (LOC) or ***launch-on-shift*** (LOS) clocking scheme for at-speed testing of intra-clock-domain delay faults. The LOC scheme was referred to as **broad-side** in [7]; whereas the LOS scheme was referred to as **skewed-load** in [8].

As indicated earlier, both approaches can result in either long test time or fault coverage loss. This paper is intended to solve the above two problems. A new logic BIST architecture using **staggered LOS** - a **staggered clocking** scheme - is proposed to achieve true at-speed test quality for any multi-clock, multi-frequency asynchronous design and detect inter-clock-domain faults across asynchronous clock domains.

The staggered clocking approach places all capture clocks in an ordered sequence to test these asynchronous clock domains in a sequential order. This approach does not require adding isolation logic between interacting clock domains, and thus can detect inter-clock-domain faults between interacting clock domains, though additional hardware is required to generate the staggered capture clock pulses. The reason why the staggered LOS approach is proposed is mainly based on the observation that staggered LOS can achieve higher BIST fault coverage than **staggered LOC** [9], although staggered LOS may incur higher physical implementation cost due to the need to use an at-speed scan-enable signal for each clock domain.

This paper is the first to disclose the logic BIST architecture supporting the staggered LOS scheme patented in [10] and show experimental results on industrial designs. Throughout this paper, it will be assumed that the STUMPS-based architecture is used and that each clock domain contains one test clock and one scan enable signal. The faults we will consider include intra-clock-domain and inter-clock-domain **structural faults** (also called **combinational faults** or **DC faults**), such as stuck-at faults and bridging faults, as well as timing-related intra-clock-domain **delay faults**, such as transition faults and path-delay faults. For non-BIST applications, please refer to an approach applied to core-based designs [11].

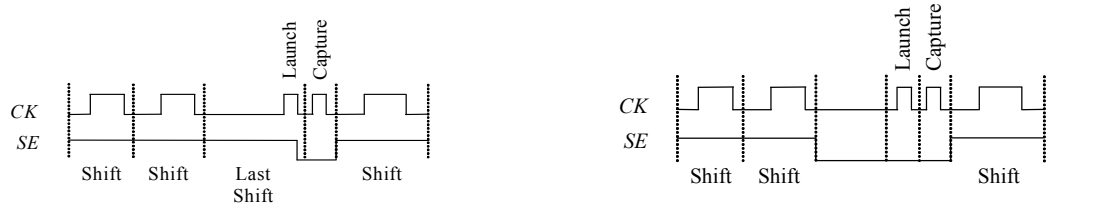
The rest of the paper is organized as follows: Section II describes two basic clocking schemes for **at-speed delay fault testing** followed by two conventional approaches using launch-on-shift. Section III presents the proposed logic BIST architecture. Section IV discusses the proposed at-speed staggered LOS scheme used in the BIST architecture. Section V shows results on two industrial designs. Section VI concludes the paper.

II. BACKGROUND

An **intra-clock-domain fault** resides in one clock domain and gets detected within the same clock domain. An **inter-clock-domain fault** resides across the clock domains and gets detected at a receiving clock domain. Two basic capture-clocking schemes can be used to test multiple clock domains at-speed: (1) *skewed-load* (which is now commonly called *launch-on-shift* [LOS]) and (2) *double-capture* (also referred to as broad-side but is now commonly called *launch-on-capture* [LOC]). Both schemes can detect structural faults and delay faults within each clock domain (called intra-clock-domain faults) or across clock domains (called inter-clock-domain faults).

Launch-on-shift uses the last shift clock pulse followed immediately by a capture clock pulse to launch a transition and capture its output test response, respectively. Launch-on-capture uses two consecutive capture clock

pulses to launch the transition and capture the output test response, respectively. In either scheme, both launch and capture clock pulses must be running at the domain's operating speed or at-speed. The difference is that launch-on-shift requires the domain's scan enable signal *SE* to switch its value between the launch and capture clock pulses making *SE* act as a clock signal. Fig. 1 shows sample waveforms using the basic launch-on-shift and launch-on-capture at-speed clocking schemes.



(a) Launch-on-Shift (a.k.a. Skewed-Load) **(b) Launch-on-Capture (a.k.a. Double-Capture)**

Figure 1. Basic At-Speed Test Schemes.

Typically, testing a scan-based BIST design based on skewed-load for at-speed delay fault testing can achieve higher fault coverage with a shorter test length [12-16]. The problems are that skewed-load can cause unwanted over-testing because more false paths can be exercised, and incur higher implementation cost because the scan enable signal *SE* must be operated at-speed for each clock domain. This is in sharp contrast to double-capture in which only a slow-speed, global scan enable signal *GSE* for all clock domains is needed.

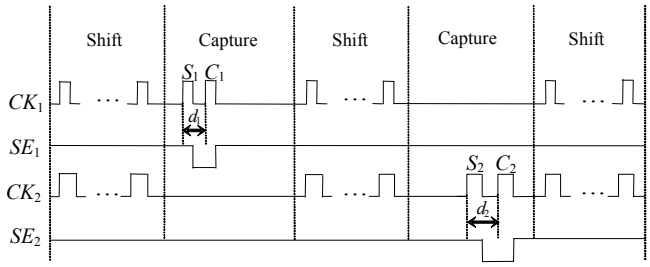


Figure 2. One-Hot Launch-on-Shift.

There are two conventional capture-clocking approaches that can be used to implement launch-on-shift: (1) one-hot launch-on-shift and (2) simultaneous launch-on-shift. The two approaches are described below.

A. One-Hot Launch-on-Shift

Using the one-hot launch-on-shift approach, a launch clock pulse followed by a capture clock pulse are applied to only one clock domain during each capture window, while all other test clocks are held inactive. An example timing diagram is shown in Fig. 2. It applies shift-followed-by-capture pulses (S_1-followed-by-C_1 or S_2-followed-by-C_2) to detect intra-clock-domain delay faults, and each scan enable signal (SE_1 or SE_2) must switch operations from shift to capture within one clock cycle (d_1 or d_2). Thus, this approach can be used for at-speed testing of intra-clock-domain delay faults. The disadvantage is long test time.

B. Simultaneous Launch-on-Shift

The long test time problem of one-hot launch-on-shift can be resolved by using the simultaneous launch-on-shift scheme illustrated in Fig. 3. The **simultaneous launch-on-shift** approach allows testing to be performed on all clock domains in parallel. This approach is helpful when clock domains do not interact with each other. For clock domains where data may propagate from one clock domain to the other, the values of source scan cells in the originating clock domains or across the clock domains must be forced to constant values (such as 0's and 1's) during the BIST operation to avoid any pattern mismatch.

The major advantages of using this approach are that (1) all intra-clock-domain delay faults can be tested simultaneously and (2) this approach is applicable for testing all clock domains in parallel without the need to align or placing clocks in a special order, but simply using whatever clock pulses available in each clock domain. However, it exposes the design to one drawback which is not present in one-hot launch-on-shift: the added capture-disabled circuitry (isolation logic) on all source scan cells could cause fault coverage loss across clock domains.

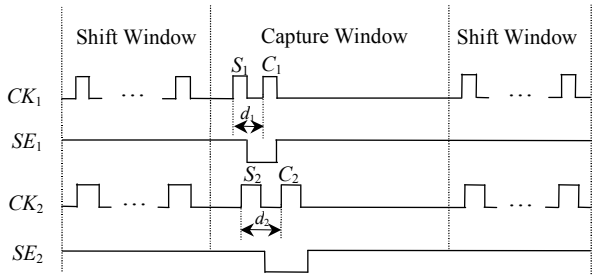


Figure 3. Simultaneous Launch-on-Shift.

III. STAGGERED LAUNCH-ON-SHIFT

The basic idea is to use an ordered sequence of capture clocks to test each clock domain running at its intended operating frequency (at-speed) during the capture operation. The order can be properly selected based on the nature of the BIST design.

The proposed **staggered launch-on-shift** scheme is to remedy the long test time problem of one-hot launch-on-shift and fault coverage loss problem of simultaneous launch-on-shift. A test timing control example is shown in Fig. 4. In this figure, capture pulses S_1-followed-by C_1 and S_2-followed-by-C_2 are applied in a sequential or staggered order in the capture window to test all intra-clock-domain delay faults and all structural faults in the design. The two last shift pulses (S_1 and S_2) are used to create transitions at the outputs of some scan cells, and the output responses to these transitions are captured by the following two capture pulses (C_1 and C_2), respectively. Both delays d_1 and d_2 are set to their respective clock domains' operating frequencies; whereas d_3 is set to 2 or more capture clock cycles controlling the receiving clock domain to ensure safe data propagation across the two clock domains so that no unknowns (X's) are captured.

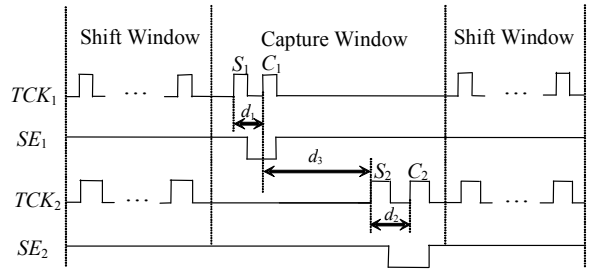


Figure 4. Staggered Launch-on-Shift.

Hence, this scheme can be used to test all intra-clock-domain delay faults and inter-clock-domain structural faults in **asynchronous clock domains**. However, there may be some structural fault coverage loss among clock domains if only one single, fixed ordered sequence of clock pulses is used across all capture cycles. This fault coverage loss is mostly related to sequentially redundant faults. It can be avoided or reduced when one-hot clocking is employed or the order of the two capture clocks is reversed.

IV. LOGIC BIST ARCHITECTURE

This section describes the logic BIST architecture based on the staggered launch-on-shift clocking scheme. Clock gating circuitry is added to the BIST controller to generate the required capture-clocking pulses.

A. General Architecture

The new logic BIST architecture is illustrated in Fig. 5. The BIST architecture for testing the BIST-ready core consists of a test pattern generator (TPG) for generating test stimuli, an input selector for providing pseudo-random or top-up ATPG patterns for the core-under-test, an output response analyzer (ORA) for compacting test responses, a clock gating block for generating test clocks from original or functional clocks, and a BIST controller for coordinating the whole BIST operation.

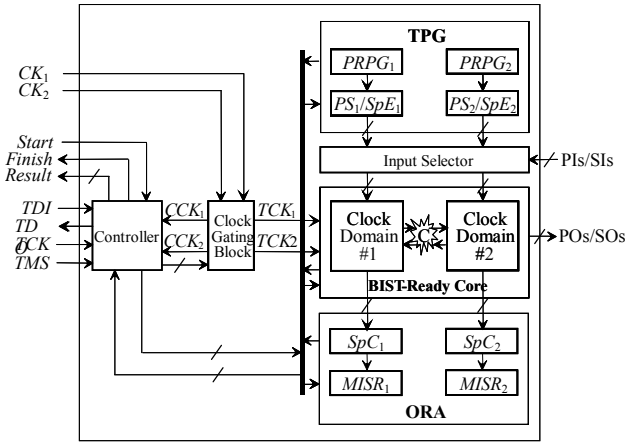


Figure 5. Logic BIST Architecture.

The test clocks are placed in a sequential (or staggered) order so that launch-on-shift clock pulses can be supplied to the BIST-ready core. The self-test operation is started by asserting the Start signal, its end is indicated by the Finish signal, and its result is shown by the Result signal. A standard IEEE 1149.1 Boundary-Scan interface under the control of the test access port (TAP) controller is used for loading initialization and configuration data or for downloading internal states for fault diagnosis.

B. BIST-Ready Core

The BIST-ready core is a scan-based design that follows all scan design rules. In addition to complying with all scan design rules, the design must also follow BIST-specific design rules, *e.g.*, to avoid bus conflict at any tri-state bus, disable asynchronous set/reset signals and false paths, and block unknown (X) values so these X's would not be captured and propagated to the MISRs.

C. TPG Circuitry and ORA Circuitry

In general, clock skews between two interacting clock domains in a BIST-ready core, as shown in Fig. 5, are not aggressively managed. In order to avoid additional design efforts for clock skew management in logic BIST, two PRPG-MISR pairs, one for each clock domain, can be used, even though both clock domains may operate at the same frequency. However, if hardware overhead is a major concern, one PRPG-MISR pair can be used. Also, linear phase shifters, (PS_1 and PS_2) (*a.k.a.* space expanders [SpE_1 and SpE_2]) can be used to reduce the length of PRPGs, and space compactors (SpC_1 and SpC_2) can be used to reduce the length of MISRs.

D. Test Control Circuitry

The test control circuitry consists of a BIST controller and a clock gating block. The inputs to the clock gating block are system clocks CK_1 and CK_2, which become CCK_1 and CCK_2 after going through some buffers. In addition, the clock gating block is controlled by signals from the BIST controller to generate test clocks TCK_1 and

TCK_2. The timings of TCK_1 and TCK_2, especially in capture mode, play a critical role in determining the test capability and physical implementation ease of the logic BIST scheme. The BIST controller works in tandem with an embedded TAP controller, which complies with the IEEE 1149.1 Boundary-Scan standard to coordinate the test, debug, and diagnosis tasks.

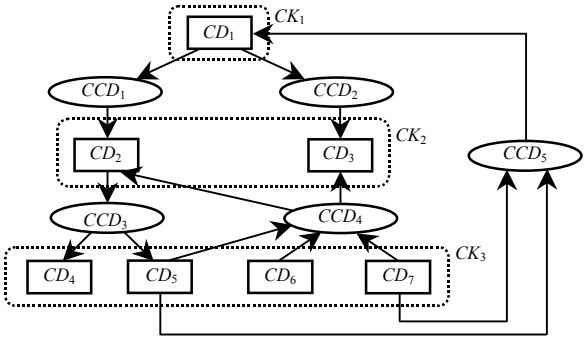


Figure 6. Clock Grouping Example.

A BIST design nowadays can contain tens of clock domains. To reduce test application time, we identify all clock domains that do not interact with each other first. **Clock grouping** is a process used to analyze all data paths in the circuit to determine all independent or non-interacting clocks, which can be grouped and applied simultaneously.

An example of the clock grouping process is shown in Fig. 6. This example shows the results of performing a circuit analysis operation on a scan design to identify all clock interactions, where an arrow shows a data transfer from one clock domain to a different clock domain. As seen in Fig. 6, the circuit in this example has 7 clock domains, $CD_1 \sim CD_7$, and 5 crossing-clock-domain data paths, $CCD_1 \sim CCD_5$.

From this example it can be seen that CD_2 and CD_3 are independent of each other, and hence their related clocks can be applied simultaneously during test of CK_2. Similarly, clock domains CD_4 through CD_7 can also be applied simultaneously during test of CK_3. Therefore in this example, 3 grouped clocks instead of 7 individual clocks can be used to test the circuit during the capture operation. The identified clock groups can also be used for capture clocking using the two above-mentioned LOS schemes described in Section II.

E. Staggered LOS Clock Generation

In order to generate an ordered sequence of capture clocks, one can use daisy-chain clock-triggering or token-ring clock-enabling for testing asynchronous clock domains. Take Fig. 4 as an example. The daisy-chain clock-triggering technique would mean that the completion of the shift window triggers the TCK_1 signal to generate two at-speed clock pulses for the first clock domain (S_1 and C_1), and make SE_1 switch operation mode from shift to capture. The completion of the generation of the two at-speed clock pulses in TCK_1 in turn triggers the TCK_2 signal to generate two at-speed clock pulses (S_2 and C_2) for the second clock domain, and make SE_2 switch operation mode from shift to capture, and so on. Finally, after a predefined capture period, the window is switched from capture to shift. The design of the *on-chip clock control* (OCC) circuit is very similar to that described in [17].

The token-ring clock-enabling technique is very similar to the daisy-chain clock-triggering technique. The only difference between them is that the former uses a clock edge to trigger the next event, while the latter uses a signal level to enable the next event.

To further increase the fault coverage of the design, the order of the capture clocks is programmable. Also, an LOC-LOS test mode is provided allowing designers to mix the use of staggered LOC clocking with staggered LOS clocking.

V. EXPERIMENTAL RESULTS

The logic BIST architecture proposed in this paper using the staggered LOS scheme has been evaluated on two industrial designs. The results are given below.

TABLE I. DESIGN STATISTICS

	Design *S*	Design *Q*
# of Primitives	*289,230*	*680,656*
# of Flip-Flops	*18,480*	*53,925*
# of Clock Domains	*8*	*10*
# of Clock Groups	*3*	*3*
# of PRPG/MISR Pairs	*8*	*10*

Table I summarizes the statistics of the two industrial designs. The two designs were taken from two customers' evaluation circuits for consumer electronics applications. To reduce test time, we developed a program to identify all independent clock groups first. A clock group consists of clocks that do not interact with each other. This allows all clocks in the clock group to be activated simultaneously during capture without suffering from any clock skew issue. In the experiments, we then applied pseudo-random patterns and performed fault simulation based on the number of clock groups identified by the clock grouping program. The computer used was a 64-bit based PC operating at 2.5GHz under the Linux operating system.

The one-hot LOS and staggered LOS clocking schemes were first applied independently to the two industrial designs listed in Table I. We chose to exclude the simultaneous LOS clocking scheme from comparison here because it cannot detect inter-clock-domain structural faults. We first applied 64,000 pseudo-random BIST patterns to both designs. For one-hot clocking shown in the second column, we pro-rated the number of BIST patterns based on the percentage of gates to be graded within each clock group. Tables II and III summarize the experimental results. Both transition and stuck-at fault models are used, where the "transition faults" row only considers intra-clock-domain transition faults within each clock domain. On the other hand, the "stuck-at faults" row considers all intra-clock-domain and inter-clock domain stuck-at faults.

TABLE II. EXPERIMENTAL RESULTS ON DESIGN *S*

	One-Hot	Staggered		
BIST Fault Coverage				
Transition Faults	***69.66%***	*74.97%*	***69.66%***	*70.58%*
Stuck-At Faults	***84.44%***	*87.93%*	*83.52%*	***84.44%***
# of BIST Patterns	*64,000*	*64,000*	*22,240*	*26,900*

TABLE III. EXPERIMENTAL RESULTS ON DESIGN *Q*

	One-Hot	Staggered		
BIST Fault Coverage				
Transition Faults	***81.20%***	*81.62%*	***81.21%***	*81.37%*
Stuck-At Faults	***87.88%***	*88.07%*	*87.73%*	***87.88%***
# of BIST Patterns	*64,000*	*64,000*	*47,296*	*53,000*

The results on both tables show that staggered clocking achieved higher transition fault coverage than one-hot clocking. We also calculated the BIST stuck-at fault coverage using the same set of LOS patterns. The proposed staggered scheme also resulted in higher stuck-at fault coverage. To further demonstrate that one-hot clocking would need much more BIST patterns (and thus longer test time) to reach the fault coverage of staggered clocking, the last two columns of both tables show the resulting numbers of BIST patterns required for staggered clocking to achieve the one-hot clocking transition fault coverage and stuck-at fault coverage, respectively.

It should be noted that theoretically, staggered clocking should always produce higher fault coverage than one-hot clocking (with the same test length). The reason is because staggered clocking allows all clock domains to be pulsed during each capture window, and thus more faults can be detected. While the experimental results shown in Tables II and III have demonstrated the effectiveness of the proposed staggered scheme, one-hot clocking may by luck result in higher fault coverage because logic BIST uses pseudo-random patterns. For top-up ATPG applications, however, one can expect that staggered clocking followed by one-hot clocking would produce fewer ATPG patterns than one-hot clocking alone to achieve the same fault coverage.

VI. CONCLUSIONS

Delay fault testing based on *launch-on-shift* (LOS) is of growing importance in the industry due to its ability in delivering higher fault coverage than using *launch-on-capture* (LOC). When a BIST design contains asynchronous clock domains, using the conventional one-hot and simultaneous launch-on-shift approaches can result in long test time and cause fault coverage loss, respectively. To address both problems, this paper proposed a new staggered launch-on-shift approach and presented a new at-speed logic BIST architecture for testing these BIST designs. Given the same number of BIST patterns, experimental results have shown that the proposed approach has yielded higher fault coverage for both transition faults and stuck-at faults than the one-hot approach. Also, it does not require adding capture-disabled circuitry across interacting clock domains as in the case of using the simultaneous LOS approach.

Note that this paper only focuses on basic capture-clocking schemes to demonstrate that staggered LOS clocking can detect more stuck-at faults and intra-clock-domain transition faults than one-hot LOS clocking and simultaneous LOS clocking for designs containing asynchronous clock domains, for a given number of BIST patterns. To achieve more than 90% BIST transition fault coverage for multimillion-gate designs, it is required to augment the staggered LOS clocking scheme with additional fault coverage improvement techniques, such as multi-activation capture cycles [18], hybrid LOC-LOS clocking [19], test point insertion [20, 21] or other techniques discussed in [22] and [23]. We plan to explore efficient approaches toward this direction and compare the pseudo-random transition results between the LOS and LOC schemes in future work. We also plan to explore the feasibility of detecting (asynchronous and synchronous) inter-clock-domain delay faults at-speed using the proposed staggered scheme.

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