Using Partial Masking in X-Chains to Increase Output Compaction for an X-Canceling MISR

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Abstract

An X-Canceling MISR [Touba 07] provides the ability to tolerate unknowns (X's) in the output response with very little loss of observability of non-X values. When the density of X's is low, an X-Canceling MISR is extremely efficient as the number of control bits depends only on the total number of X's in the output response. However, for higher X-densities, an X-Canceling MISR becomes less efficient. This paper describes a very effective approach for using an X-Canceling MISR for designs with high X-density. It utilizes the idea of stitching together scan cells that capture the largest number of X's into "X-chains" as was proposed in [Wohl 08]. In the proposed approach, a partial X-masking approach is used for the X-chains to eliminate the vast majority of the X's at very little cost in terms of control bits. Only the X's coming from the scan cells not in the X-chains plus X's that are left unmasked in the X-chains need to be handled by the X-canceling MISR thereby significantly reducing the total number of control bits required. Experimental results show an order of magnitude improvement in the output compaction can be achieved.

Keywords: output compression; output masking; X-chains

1. Introduction

The number of unknown *'X'* values in the output response is increasing due to larger numbers of false paths, multi-cycle paths, analog blocks, tri-state buses, and uninitialized memories. Compacting output streams that have *X's* is a major issue for test compression and BIST. *X* values corrupt the final signature making it unknown. A number of schemes have been developed to deal with the problem of *X's* in the output response.

One approach is to modify the circuit-under-test (CUT) to eliminate the sources of *X*-values. This involves blocking sources of *X* within the circuit by inserting design-for-testability (DFT) hardware to prevent *X*s from propagating into scan cells [Wang 06]. Another approach, which does not require modifying the CUT, is *X*-masking which masks out *X*'s at the input to the compactor. Mask control data is used to specify which scan chain outputs should be masked during which clock cycles. Many schemes for *X*-masking hardware design and mask control data compression have been developed [Barnhart 01], [Wohl 01, 03, 04], [Pomeranz 02], [Chickermane 04], [Volkerink 05], [Chao 05], [Tang 06], [Rajski 06a], [Rajski 08], [Mrugalski 09]. A third approach is to use an *X*-tolerant compactor which can compact an output stream that contains *X*'s without the need for *X*-masking. *X*-tolerant compactors have been developed based on linear combinational compactors [Mitra 04a], [Patel 03], [Sharma 05], [Wohl 08], convolutional compactors [Rajski 05], and circular registers [Rajski 06b], [Gizdarski 10].

In [Touba 07], the concept of canceling out *X*'s from MISR signatures was proposed. An *X*-canceling MISR methodology was described which can achieve arbitrarily high error coverage very efficiently where error coverage is the percentage of scan cells that are observed in the presence of *X*'s. Symbolic simulation is used to express each bit of the MISR signature as a linear equation in terms of the *X*'s. Linearly dependent combinations of MISR signature bits are identified with Gaussian elimination and are XORed together to cancel out all *X* values thereby yielding deterministic values that are invariant of what the final values of the *X*'s end up being during the test.

The advantage of an *X*-canceling MISR is that it is very precise in canceling out the *X*'s, losing observation of very few of the non-*X* values. Thus it retains both the modeled and non-modeled fault coverage of the original test set. Conventional *X*-masking approaches which mask out entire scan chains or entire scan slices are more blunt approaches which lose observation of a considerable number of scan cells in the process of masking out *X*'s. This results in more test vectors needing to be applied to achieve the same fault coverage and impacts non-modeled fault coverage. When the *X*-density is low, an *X*-canceling MISR is very efficient and requires fewer control bits than conventional *X*-masking approaches. However, as the *X*-density increases, the control bits for *X*-canceling begins to exceed those required for *X*-masking, and it becomes less efficient.

Some previous work has looked at improving the efficiency of an *X*-canceling MISR by trying to reduce the number of *X*'s that reach it. In [Datta 11], circular registers are used to stack *X's* on top of each other so they can be treated as a single *X* when performing *X*-canceling. In [Ramdas 12], a toggle-masking scheme is used to mask

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consecutive bits of X's at the output of all scan chains. This requires $log_2(n+1)$ dedicated control bit channels from the tester for n scan chains and significant design overhead (n XOR gates, n MUX gates, n flip-flops and a $log_2(n+1)$ by $(n+1)$ decoder). The proposed scheme performs a much lower cost partial X-masking requiring only one dedicated control bit channel from the tester and only one AND gate per chain for a subset of scan chains.

It has been observed by researchers [Czysz 10], [Wohl 10], that there is a lot of locality in the scan cells where X's are captured. A relatively small percentage of the scan cells capture the vast majority of the X's that are generated. In [Wohl 08], the idea of stitching together the scan cells that capture the most X's into a small number of "X-chains" was proposed in the context of combinational compaction. The modes of the combinational compactor were designed so that the X's in the X-chains could be tolerated with less cost. This paper proposes an approach that uses the idea of X-chains in the context of an X-canceling MISR. In the proposed approach, a partial X-masking scheme is used for the X-chains to mask the vast majority of the X's at very low cost. The partial X-masking scheme involves analyzing the output response in the X-chains and avoiding masking slices when there will be loss of fault detection. In the slices where the X-chains are not masked, any X's that appear are allowed to pass through to the MISR which will be referred to here as "X-leaking." In conventional X-masking scheme, X-leaking is not tolerable because it will corrupt the MISR signature. Consequently, over masking ends up being done to ensure that there is no X-leaking. This results in loss of observability and consequently loss of fault detection. More ATPG vectors end up being used to achieve the desired modeled fault coverage. With an X-Canceling MISR, X-leaking is not a problem because the X's can be canceled out in the MISR signature. The responses in the scan slices that are not part of the X-chains also go into the X-canceling MISR where any X's that appear are canceled.

The proposed approach exploits the fact that the number of control bits required to cancel X's in an X-canceling MISR depends only on the total number of X's. So it is very efficient to handle any residual X's that don't get canceled in the X-chains. By masking the vast majority of the X's with the low cost partial masking in the X-chains, the control bits required to handle the remaining X's that get into the X-canceling MISR are greatly reduced.

The paper is organized as follows: Sec. 2 reviews the operation of an X-canceling MISR. Sec. 3 describes the proposed scheme. Sec. 4 discusses how the number of X-chains is selected. Sec. 5 shows experimental results, and Sec. 6 is a conclusion.

2. Review of X-Canceling MISR

This section gives a brief overview of the operation of an X-canceling MISR. A more detailed explanation can be found in [Touba 07].

Assume the output response has been captured in the scan chains after applying a test vector. The value in each scan cell is represented with a symbol. An example is shown in Fig. 1. Once the output response has been shifted in to the MISR, the final MISR signature can be expressed in terms of the symbols through symbolic simulation. Each MISR bit is represented by a linear equation of the scan cell symbols. Fig. 1 illustrates this symbolic representation. The final value of the top bit of the MISR is $X_1 \oplus O_3 \oplus O_8 \oplus O_{13}$, where X_i denotes an X value and O_i indicates a non-X value.

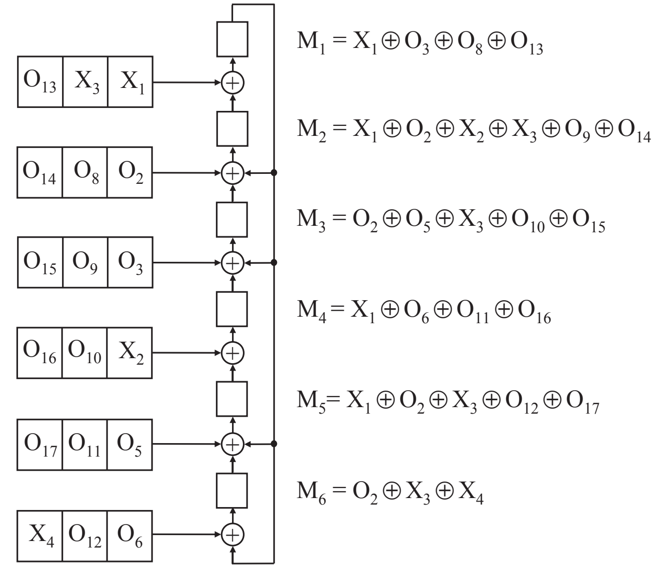

Figure 1. Example of Symbolic Simulation of MISR

$$\begin{array}{l} M_1 = X_1 \\ M_2 = X_1 \oplus X_2 \oplus X_3 \\ M_3 = X_3 \\ M_4 = X_1 \\ M_5 = X_1 \oplus X_3 \\ M_6 = X_3 \oplus X_4 \end{array} \rightarrow \begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix}$$

Figure 2. Linear Equations for MISR in Fig. 1

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \begin{array}{l} M_1 \\ M_2 \\ M_3 \\ M_4 \\ M_5 \\ M_6 \end{array} \xrightarrow{\text{Gaussian Elimination}} \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{array}{l} M_1 \\ M_1 \oplus M_2 \oplus M_3 \\ M_3 \\ M_3 \oplus M_6 \\ M_1 \oplus M_3 \oplus M_5 \\ M_1 \oplus M_4 \end{array}$$

Figure 3. Gauss-Jordan Elimination of MISR Equations

The focus here is on the unknown values, so each MISR bit equation can be reduced to a linear combination of the X values by assigning *0* to each non-X values without loss of generality. These linear combinations can be expressed in the form of a matrix as shown in Fig. 2. Each entry in the matrix has a *1* if the MISR bit corresponding to the row depends on the X corresponding to the column.

If the number of columns is less than the number of rows, i.e., the number of X's is less than the MISR size, then some row combinations will be linearly dependent. Gauss-Jordan elimination [Cullen 97] can be performed on the matrix in Fig. 2 to identify the linearly dependent combinations of rows as illustrated in Fig. 3. The last two rows in Fig. 3 have all *0*s and this indicates combinations of MISR bits in which all the X's cancel out. The first all-*0* row corresponds to $M_1 \oplus M_3 \oplus M_5$. This implies that XORing MISR bits M_1, M_3, and M_5 generates an "X-canceled" signature bit which depends only on scan cells that captured non-X values as shown below:

$$M_1 \oplus M_3 \oplus M_5 = O_3 \oplus O_5 \oplus O_8 \oplus O_{10} \oplus O_{12} \oplus O_{13} \oplus O_{15} \oplus O_{17}$$

The values of these X-canceled MISR bit combinations are deterministic and can be predicted through simulation. Therefore, during test, they can be compared with their fault-free values in order to detect errors.

The architecture of an X-canceling MISR is shown in Fig. 4. The MISR captures response across many clock cycles and may span multiple test vectors until the MISR fills up with X's. The MISR signature is then processed by selectively XORing linearly dependent combinations of MISR bits in terms of the X's to generate X-free output response to send to the tester. The error coverage can be made arbitrarily high by generating and checking a sufficient number of X-canceled output responses. The probability of not detecting an error drops by a factor of 2 for each X-canceled combination that is checked. If q X-canceled combinations are checked, then the error coverage for it will be $1\text{-}2^{-q}$. So if q=7, then the error coverage will be 99.2%, and each MISR signature can capture up to $(m\text{-}7)$ X's where m is the size of the MISR.

3. Proposed Scheme

The proposed scheme involves stitching X-chains from the scan cells that capture the most X's as described in [Wohl 08]. Each scan cell is marked as an X-cell if the frequency at which it captures X's is above a certain threshold. The threshold used is adjusted based on the number of X-chains desired. Scan stitching is then performed from the set of X-cells to create the X-chains. Once all the X-chains are created, the rest of the scan cells are stitched as regular scan chains. Once all scan chains are stitched the scan chains can be reordered and/or repartitioned but will need the additional restriction that X-chains can only be repartitioned with other X-chains and not with regular scan chains.

A block diagram of the proposed scheme is shown in Fig. 4. As can be seen, there is a mask bit that is set to 0 to mask the data coming out of X-chains to a known value which is 0. The masking is done on a cycle-by-cycle basis. This mask bit is set to 0 in all cycles except when one of the data bits coming from the X-chains has a value that must be observed to ensure detection of faults. This is determined by keeping track of which scan cells the fault effects propagate to during fault simulation and marking them as D's. When performing X-masking, the D's should not get masked. One tester channel is used to drive the X-chain mask control bit

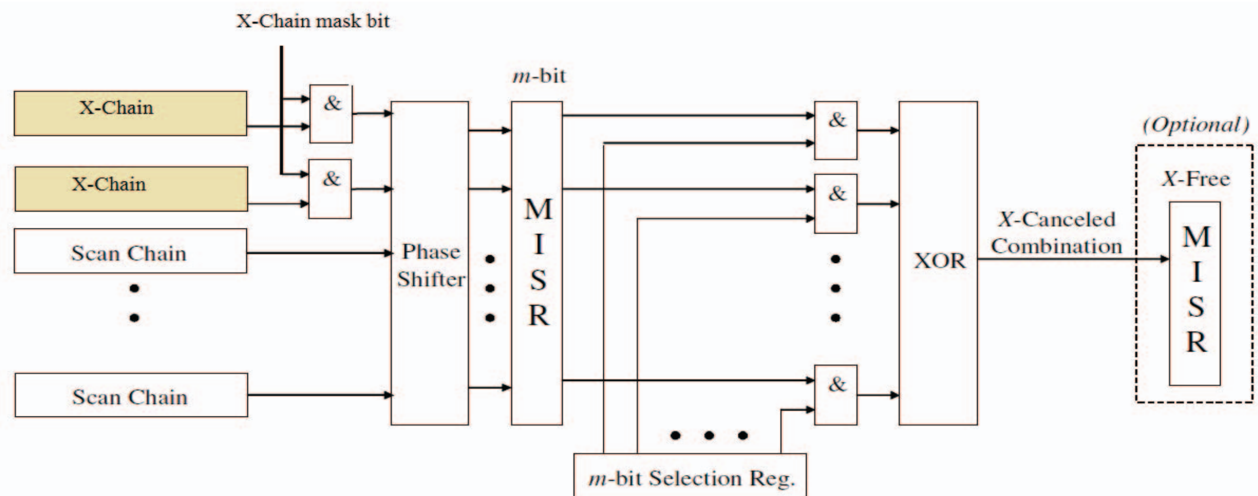

Figure 4. X-canceling MISR Architecture with X-Chains

and masks all the *X*-chains in clock cycles when no *D*'s occur, but does not mask *X*-chains in cycles when there are one or more *D*'s. When the *X*-chains are not masked, there is a possibility of an *X* passing through to the MISR which results in "*X*-leaking". In conventional *X*-masking applications, *X*-leaking cannot be tolerated, but in this scheme with an *X*-canceling MISR, they can be canceled out in the MISR signature.

The advantage of using the proposed scheme compared to just using a conventional *X*-canceling MISR is that it takes fewer control bits to mask out *X*'s in the *X*-chains than it does to cancel them out in the MISR signature. One control bit is used in each clock cycle, and since the *X*-chains have a high density of *X*'s, many *X*'s get canceled out. This significantly reduces the number of *X*'s that have to be canceled out in the *X*-canceling MISR.

The overall effectiveness of this scheme will depend on how many *X*-chains are used, since the greater the number of *X*-chains the greater the chances that one of them will have a *D* in a given scan slice and thus result in more *X*-leaking. On the other hand if the number of *X*-chains are too small, then there will be more *X*'s in the regular scan chains and that will also lead to more *X*'s in the MISR. The ideal number of *X*-chains that are used will thus be design dependent. Selecting the optimal number of *X*-chains is discussed in the next section.

4. Selecting Number of X-Chains

The optimal number of *X*-chains depends on the frequency of *X*'s and the frequency of *D*'s. Table 1 shows experimental results for a circuit where different numbers of *X*-chains were tried. The first column shows the number of *X*-chains. The second column shows the percentage of the *X*'s that ended up being captured in the *X*-chains. As the number of *X*-chains increases, the percentage of *X*'s captured in the *X*'s chains increases until it reaches 100% with 36 *X*-chains. The third column shows the total percentage of *X*'s masked in the *X*-chains (which obviously cannot be greater then the percentage of *X*'s captured in the *X*'s chains). The reason why the percentage of *X*'s masked is less then the percentage captured in the *X*-chains is because of the presence of *D*'s in the *X*-chains which prevent masking in some clock cycles. As the number of *X*-chains increases, the chance of a *D* appearing during a given clock cycle goes up and consequently the amount of *X*-leaking also goes up. As can be seen, the percentage of *X*'s that are masked peaks at 12 *X*-chains. When the number of *X*-chains is increased to 18, even though the total number of *X*'s in the *X*-chains increases from 95.6% to 99.0%, the *X*'s masked goes down because the *D*'s cause more *X*-leaking. The last column shows the total number of control bits which is equal to one bit per clock cycle for the *X*-chain mask control bit plus the control bits required for canceling out the *X*'s that get into the *X*-canceling MISR. The number of control bits is minimized for 12 *X*-chains because at that point the percentage of *X*'s masked is maximized meaning less *X*-canceling is required. This information is also shown graphically in Fig. 5 where the total control bits is plotted on the y-axis with the number of *X*-chains in the *X*-axis. As can be seen, as the number of *X*-chains is increased, initially the total control bits is reduced until it is minimized at some point beyond which it begins to increase as additional *X*-chains are added.

This same type of curve was observed for all circuits in which experiments were performed. Selecting the optimal number of *X*-chains involves performing simulations to find the number of *X*-chains where the curve minimizes.

It is possible to partition the *X*-chains and use multiple tester channels to bring in more control signals to perform partial *X*-masking on each of the partitions of *X*-chains. While this will reduce *X*-leaking, the gain in terms of overall control bits is not substantial enough to offset the cost of using the additional tester channels. As can be seen in Table 1, 89.2% of *X*'s is already masked with 12 *X*-chains. So the maximum possible improvement for more masking is limited to only 10.8% which is simply not enough to make the use of an additional tester channel to support more *X*-chains to be worthwhile.

Table 1. Experimental Results for Ckt-*A* Using Different Numbers of *X*-chains

Num. *X*-Chains	*X*'s in *X*-Chains	*X*'s Masked	Total Control Bits
4	58.7%	58.1%	22.3M
8	84.5%	81.4%	10.7M
12	95.6%	89.2%	6.8M
18	99.0%	87.3%	7.8M
36	100%	73.6%	14.6M

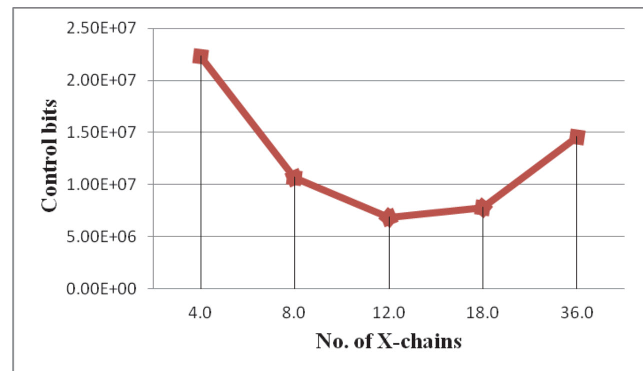

Figure 5. Reduction in Control Bits versus *X*-Chains for Ckt-*A* with 1% *D*'s

5. Experimental Results

Experiments were performed on three industrial circuits with different *X*-densities to evaluate the proposed method of using partial masking in *X*-chains in conjunction with an *X*-canceling MISR [Touba 07]. A 256 bit MISR was used, however, as shown in [Touba 07], the total number of control bits is relatively independent of the size of the MISR, so different size MISRs would show similar improvements. The circuits themselves were not available to us, so we were not able to perform fault simulation to mark the exact locations of the *D*'s. Instead, *D*'s were randomly injected assuming different percentages of *D's*.

Table 2 shows results for three different circuits for different numbers of *D*'s and *X*-chains. The *X*-density for each circuit (which is the percentage of *X*'s) is shown in the first column. The second column shows the total number of bits stored on the tester for using an *X*-canceling MISR as described in [Touba 07]. The third column shows the number of *X*-chains that was used. Three different numbers of *X*-chains were tried for each circuit. The next columns show the results for the proposed scheme assuming 0.5% *D*'s, 1% *D*'s, and 2% *D*'s. For each case, the total number of bits stored on the tester is shown and the improvement factor versus using an *X*-canceling MISR by itself is shown.

As can be seen in Table 2, a significant improvement in compression is achieved with the proposed scheme for both low and high *X*-density circuits. The greatest improvement is for Ckt-*B* which has the highest *X*-density. For Ckt-*C*, even though the *X*-density is very low it still gives significant improvement in compression. It can be expected that as the *X*-density increases, the proposed scheme will provide increasing larger improvement factors.

6. Conclusions

An *X*-canceling MISR was shown in [Touba 07] to be very efficient for small *X*-densities. The scheme proposed in this paper exploits this fact by combining *X*-canceling with partial *X*-masking to handle high *X*-densities. The result of masking *X*'s in *X*-chains is that the MISR has a lot fewer *X*'s and requires less cancelling which in turn means less control bits needed. Because the proposed method can handle *X*-leaking, it is able to achieve high compression while still providing very precise masking where very little observation of non-*X* values is lost. This results in fewer test vectors and hence better test vector compression, output response compression, and test time. Since the test data bandwidth is always fully utilized with an *X*-canceling MISR, the test time reduction will scale directly with the reduction in control bits.

Table 2. Experimental Results for Proposed Partial Masking in *X*-Chains for Different Designs

Circuit	*X*-Canceling [Touba 07] Bits	Num. *X*-Chains	**0.5% *D*'s**		**1% *D*'s**		**2% *D*'s**	
			Bits	Improve Factor	Bits	Improve Factor	Bits	Improve Factor
Ckt-A X-density = 2.4%	49.97M	10	5.1M	9.7	8.2M	6.1	10.3M	4.8
		12	5.2M	9.6	6.8M	**7.3**	9.8M	**5.1**
		15	4.6M	**10.8**	6.8M	7.3	11.0M	4.6
Ckt-B X-density = 2.7%	21.33M	2	8.5M	2.5	8.5M	2.5	8.5M	2.5
		4	3.6M	5.9	3.6M	5.9	4.0M	5.3
		6	1.9M	**11.2**	2.3M	**9.3**	3.0M	**7.1**
Ckt-C X-density = 0.5%	5.2M	1	1.9M	2.7	1.9M	2.7	1.9M	2.7
		2	1.5M	**3.5**	1.5M	**3.5**	1.5M	**3.5**
		4	1.5M	3.5	1.6M	3.3	1.7M	3.1

Acknowledgements

This research was supported in part by the National Science Foundation under Grant No. CCF-0916837.

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