Delay Testing of SOI Circuits: Challenges with the History Effect

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Abstract

Testing Partially-Depleted Silicon-On-Insulator (PD-SOI) integrated circuits presents new challenges that were not concerns in previous bulk CMOS technologies. Gates are affected by a variation in delay based on threshold voltage fluctuations. The fluctuations are dependent on the switching history of the device and this poses a serious challenge with regard to testing delays. To ensure worst-case operation, pre-conditioning of the path is necessary prior to a delay test. This paper provides background on SOI device operation and describes why and how pre-conditioning is accomplished It is shown that a three-pattern delay test where the V1 and V3 patterns are the same is required to pre-condition the path for worst-case delay. Two novel scan latch designs that are capable of applying the three-pattern tests are presented.

1. Introduction

Partially-Depleted Silicon-on-Insulator (PD-SOI) technology has recently emerged as a strong candidate for main stream low-power high-performance digital applications. Fabricating MOSFETs on a buried oxide layer provides total isolation between transistors. This isolation decreases junction capacitance thus allowing devices to operate at higher frequencies or at substantially lower power at the same frequency. SOI eliminates the possibility of latch-up permitting higher packing densities which reduces the required silicon area as well as routing capacitance between devices [Chuang 98], [Krishnan 98].

However, isolating the body of a transistor leads to complications for design and test. Primarily, the threshold voltage can be modulated based on the body effect due to fluctuations in the body voltage. The body effect describes how the threshold voltage is reduced as the body voltage is increased. The modulated threshold voltage causes variation in the delay based on the switching history of the device and specifically, how that history affects the body voltage. Variation of gate delay poses some serious challenges for testing integrated circuits in SOI and will require new test techniques to test critical paths under the worst-case switching history. Traditional at-speed functional testing will not ensure worst-case switching histories for most paths.

Many of these problems can be addressed during the design phase with the use of body contacts. Body contacts are used to tie the body voltage to a specified level, however, they result in increased area and reduce some of the advantages of the floating body. Limited use of body contacts in some circuits, particularly PLLs, IOs, and sense amps, is inevitable. However, the vast majority of transistors in combinatorial logic and memories will be left floating. Fully-Depleted SOI (FD-SOI) eliminates many of these issues as well, however, current manufacturing processes to date can not produce the across-wafer tolerances necessary for the thickness of the active silicon layer. The threshold voltage is influenced by this thickness based on the amount of silicon volume available to deplete, and thus FD-SOI can not currently be used in main stream applications until further progress is made.

This paper discusses the issues involved in testing paths in SOI circuits for worst-case delays. It is shown that three-pattern delay tests are required to precondition paths to emulate worst-case switching histories. New scan latch designs are presented for applying the three-pattern tests. By using these new scan latches in select locations in the scan chain, the three-pattern tests can be applied to test critical timing paths in SOI circuits under the worst-case conditions.

The paper is organized as follows: Section 2 discusses the impact of the floating bodies on testing delays in PD-SOI circuits. Section 3 describes a three-pattern test necessary to emulate a worst-case switching history for these circuits. Section 4 briefly delineates two existing scan elements for comparison with two proposed implementations that are capable of performing the three-pattern test, with Sec. 4.1 describing in detail the first element and Sec. 4.2 describing the second. Section 5 includes simulation results that illustrate the need for testing under the worst-case switching histories using the proposed three-pattern delay tests. The conclusion is given in Sec. 6.

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2. The Impact of PD-SOI on Path Delays

The primary challenge with testing integrated circuits fabricated in SOI is the history-dependent delay. Having a unique switching history, each path in a sequential circuit will have a different variation of delay based on the unique history. The enumeration of all possible switching histories for each path is impossible. However the switching histories for each device can be simplified to three possible initial states - OUT-HI, OUT-LO, and SSS [Wei 96], [Krishnan 98]. Simplifying the history into these three initial conditions provides the means for manageable analysis of the impact of the switching history on device operation and testing.

Using a typical CMOS inverter as an example, the first state, OUT-HI, is static in nature and is characterized by a logic low input and logic high output for an extended period (much greater than the clock period). The body voltage of both transistors will reach a level between the corresponding source and drain due exclusively to reverse-bias leakage in the drain/body diode and forward-bias current from the source/body diode. With the output at a logic high level, the drain of both transistors is at V_{dd}, consequently the level of the body voltage of the NFET approaches the cut-in voltage of the source/body diode while the PFET body voltage rests at V_{dd} (V_s=V_b=V_d=V_{dd}). The threshold voltage of the NFET is thus reduced relative to the bulk case, (one of the advantages of SOI is the general reduction in delay due to the reduced V_t) while the threshold voltage of the PFET is, at least in the static sense, left at the bulk level. This combination of threshold voltages for the P and N FET's tend to decrease the propagation delay for high to low transitions (Tphl) to an approximate best-case value and increase the propagation time from low to high (Tplh) to a worst-case value [Krishnan 98] until equilibrium levels are reached in subsequent switching.

Conversely, the second case, OUT-LO, is where a static logic high level is applied to the input and the output is low for an extended period. The PFET body voltage will then be a potential barrier drop from V_{dd} while the NFET body voltage will rest at ground. This results in delays opposite to the OUT-HI state, fast Tplh and slow (worst-case) Tphl.

The third state, Switching Steady State case (SSS) is characterized by a continuous oscillation of the input at the clock frequency. In this simplification, the body voltages of both the PFET and NFET reach an average equilibrium level. For the NFET, the average body voltage is typically higher than the ground reference as is used in bulk technology, and consequently the threshold voltage is lower than bulk, V_{t0}. The dynamic level of the body voltage results from several complicated mechanisms, including capacitive coupling with the gate/source/drain, reverse-bias leakage in the source/drain junctions, forward-bias injection of carriers, recombination, and impact ionization. Similarly affected, the body voltage of the PFET is lower than V_{dd} as in the bulk case and the threshold voltage is reduced below that of bulk to an equilibrium level as well. Additionally, in the SSS case, the body voltages tend to a higher equilibrium value at higher frequencies based on an increase in impact ionization due to more frequent switching. This increase in body voltage could possibly result in shorter delays then described in the faster transitions in the two static cases. However the worst-case transitions for Tplh and Tphl are bound by states OUT-LO and OUT-HI respectively, because they effectively represent the SSS case with an infinite period.

By simplifying each path's history into three possible initial states, meaningful analysis can be made of the impact of the floating body on the delay through a path. All switching histories can be approximated by these simplified cases. A gate with inputs remaining inactive for some time frame would be approximated by one of the two static cases, OUT-HI or OUT-LO, depending on the value of the outputs. All other gates with actively switching inputs would be approximated by the SSS case. The time frame used to define inactivity depends on the time constants of the mechanisms that affect the body voltage. The time constants are different for each unique SOI fabrication process, but could be in the order of hundreds of clock cycles. A switching history that can be approximated by OUT-HI provides best-case Tphl and worst-case Tplh, while OUT-LO provides the reverse. The SSS case generally provides propagation delays that fall between the other two extremes (although it can provide best-case values at high frequencies due to increased impact ionization).

Having discussed the three possible initial conditions, pulse stretching can now be described. Fig. 1 illustrates a two inverter buffer. In this depiction, the first inverter, *I1*, is pre-conditioned with the input low and output high, thus it is in the OUT-HI state. The input of the second inverter, *I2*, is high and the output is low. Consequently the NFET of *I1* is "strong" while the PFET counterpart is "weak" due to variation in threshold voltage. Conversely, the FET's of *I2* are reversed in strength relative to *I1* due to the opposite pre-conditioning. If subsequently, a pulse is applied to the input of *I1*, the *I1* NFET and *I2* PFET are activated and due to the reduced threshold on these transistors the transition propagates quickly through the buffer. However, when the input is returned to a logic low state, the *I1* PFET and the *I2* NFET are activated and the delay is aggravated by the lower drive capability, resulting in a worst-case delay. This extended delay is highlighted with arrows in Fig. 1.

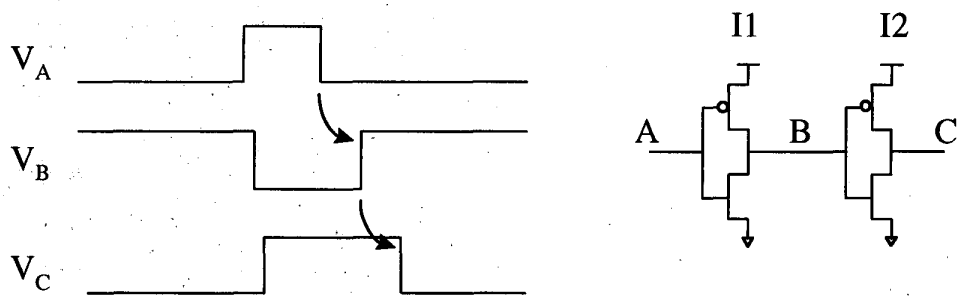

Figure 1. Illustration of Pulse Stretching Phenomenon in PD-SOI

During typical functional testing of integrated circuits, a majority of the paths are switching with an average frequency that is less than the clock frequency but much faster than the time frame defining inactivity and hence would be approximated by the SSS case. As described before, the SSS case would not provide worst-case delays for most paths, and consequently traditional at-speed functional testing could not guarantee worst-case operation. This is a problem because the device may be operated in the field in such a way that the worst-case switching history may arise which could result in the device failing (i.e., the delay along a path may be longer than the clock period). New approaches for testing will be necessary that pre-condition paths for worst-case delays.

3. Three-Pattern Delay Testing with Pre-conditioning for SOI

To test the worst-case propagation delay through a path, a three-pattern test will be required. Three-pattern tests have previously been used to initialize the state of a gate or provide transitions on multiple inputs [Franco 91]. In the case of SOI, this method is required to provide pre-conditioning for the functional path under test. *V1* is the pre-conditioning vector and is applied to the path for the time frame necessary for the OUT-HI or OUT-LO conditions to become valid. *V2* is applied to initialize a transition and is held for a sufficiently long period so that the signal can stabilize at the capture latch input. The application time of *V2* should not exceed a single clock cycle due to the reduction of the impact of pre-conditioning on the path. Subsequently, *V3* applies the logic value that prompts the transition to be tested. This three-pattern sequence results in the pulse-stretching scenario previously described and provides the worst-case delay for the transition of the data path.

As a consequence of *V1* and *V3* being equal for the pulse-stretching test method, implementation of the three-pattern test can be simplified relative to general three-pattern testing. Test vector generation for the proposed test method is compatible with existing two-pattern test generation software. Effectively, *V2* and *V3* of the proposed method are analogous to *V1* and *V2* of a traditional two-pattern delay test. Conveniently, *V3* shares the same value as the pre-conditioning vector, *V1*. Table 1 summarizes the relationship of the vectors of both the traditional two-pattern delay test with the proposed pulse- stretching three-pattern delay test for SOI.

Table 1. Summary of Vectors for Traditional Two Pattern Test and Proposed SOI Test

	Traditional Two-Pattern Test	**Proposed Three-Pattern Test for PD-SOI**
V1	Initializes the transition	Pre-conditions the data path
V2	Launches the transition	Initializes the transition
V3		Launches the transition (same value as pre-conditioning vector, V1)

4. Scan Elements Capable of Implementing Proposed Three-Pattern Test

Given that three-pattern delay tests are required for testing SOI circuits, the question then is how to apply such tests. Some complications arise when extending the conventional approaches used for applying two-pattern delay tests to the case where three patterns are required. Two-pattern delay tests are applied using a conventional scan chain by either "scan-shifting" or "functional justification" [Cheng 93].

Scan-shifting involves shifting the V1 pattern into the scan chain, and then generating the V2 pattern by a one-bit shift of the V1 pattern. Extending scan-shifting for the proposed three-pattern tests would require that a one-bit shift of the V2 pattern would have to generate a V3 pattern that is the same as the V1 pattern. This is very unlikely, and hence scan-shifting is not a viable solution for applying three-pattern tests.

Functional justification involves shifting the V1 pattern into the scan chain and then generating the V2 pattern through the functional logic in the next clock cycle. This requires ATPG across two time frames which can be computationally expensive and sometimes leads to aborts in the ATPG process. Functional justification can be extended for three-pattern testing by generating the V3 pattern through the functional logic in the following clock cycle. This requires ATPG across three time frames and hence is more time consuming and more likely to lead to aborts in the ATPG process. However, functional justification may be sufficient for applying the proposed three-pattern tests in some designs.

An alternative to functional justification is to use enhanced scan elements which contain additional latches. Enhanced scan element designs have been proposed for two-pattern delay testing [Malaiya 84], [Glover 88], [Dervisoglu 91]. The idea is to add an extra latch to the scan element so that both the V1 and V2 patterns can be stored and applied in succession. In this paper, two new scan elements are proposed that can provide the three-pattern test necessary to exercise SOI in the worst-case conditions. These designs exploit the fact that the V1 and V3 vectors are the same to minimize the area and number of control signals. For comparison purposes, a brief description of the operation and design of both a standard scan element as well as an enhanced two-pattern delay test scan element are presented followed by the proposed scan elements.

Fig. 2 illustrates the standard scan element used in Level Sensitive Scan Design (LSSD) [Eichelberger 78]. In system mode, a two-phase clocking scheme is used with clocks *C1* and *C2* for the master and slave latches respectively, while *ACLK* is left at a logic low. In test mode, *ACLK* and *C2* are alternately pulsed to scan values through the scan path and, once complete, *C1* captures the value from the tested data path.

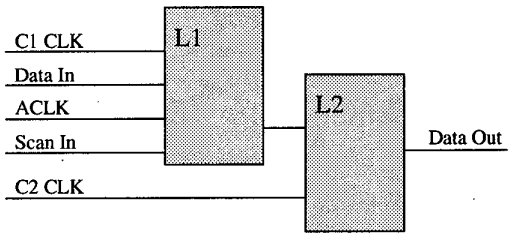

Figure 2. Standard LSSD Scan Element

The two-pattern delay test scan element proposed in [Dervisoglu 91] is shown in Fig. 3. (The scan element has been modified for a two-phase clocking scheme for comparison purposes with the two proposed scan elements.) An additional latch is introduced relative to the standard LSSD element in Fig. 2. This permits the storage of test vectors *V1* and *V2* as described previously. In system mode, clocks *C1* and *C2* are used to exercise latches *L1* and *L2* as a flip-flop, while all other clocks are held low. In scan mode, the master-load (*ML*) signal is asserted while *SI_CLK* and *SO_CLK* are alternately pulsed, scanning in the final value vector, *V2*. The scan path traverses through *L2* and *L3*, but with *ML* asserted, *L1* also captures the value of *V2*. A second scan operation is completed with *ML* deasserted, which isolates *L1* from the final value vector, *V2*, as it is scanned through *L2* and *L3*. Once complete, the initial value is stored in *L2* and the final value in *L1*. System clocks are then used to complete the traditional two-pattern delay test.

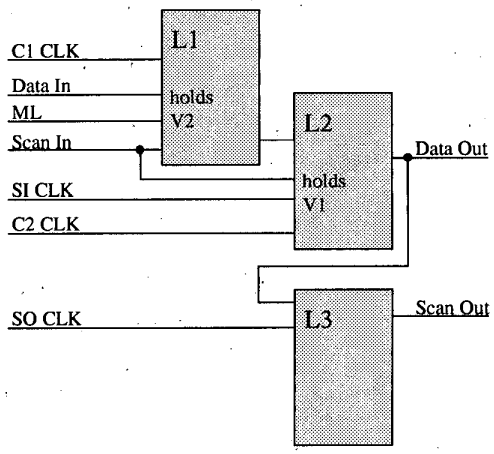

Figure 3. A Two-Pattern Delay Test Scan Element

4.1 Proposed Scan Element 1

Fig. 4 illustrates the first of two proposed scan element capable of implementing the three-pattern SOI test

method, scan element 1. In system mode, clocks *C1* and *C2* are used together in a two-phase clocking scheme. All other clocks are held low, and the scan element is used as a functional flip flop with *Data In* as the input, *Data Out* as the output. There are two scan modes, A and B, which are used to shift in the *V2* and *V3* values independently and comprise two parallel scan paths with the *L1* latch common to both. Scan path B is used to shift in the value of *V2* into *L3*. This is accomplished by alternately pulsing the *B1 CLK* to capture *Scan In B* into *L1* and pulsing the *B2 CLK* to transfer the *L1* value into *L3*. Subsequently, scan path A is used to shift in the value for *V1/V3* into latch *L2*. By alternately pulsing the *ACLK* and the *C2 CLK*, the values are shifted while maintaining the previously scanned value of *V2* in *L3*.

Once the *V1/V2/V3* vectors have been established, the logic level of *V1* is applied to the data path for an extended period of time for pre-conditioning. The *C3 CLK* is toggled to transfer the *V2* value stored in *L3* into *L2* and consequently the *V2* value is presented to the functional path. This initializes the path for the transition to be tested. By pulsing the *C2 CLK*, the value of *V3* held in *L1* is transferred to *L2* and provides the logic value necessary to transition the path. *C1 CLK* is pulsed to capture the data at the input of the latch that terminates the path. The operation is done in the time frame dictated by the delay value to be tested, C2 *CLK* rise (launching the value of *V3* into the data path) to the fall of *C1 CLK* (sampling the value at the input of the capture latch).

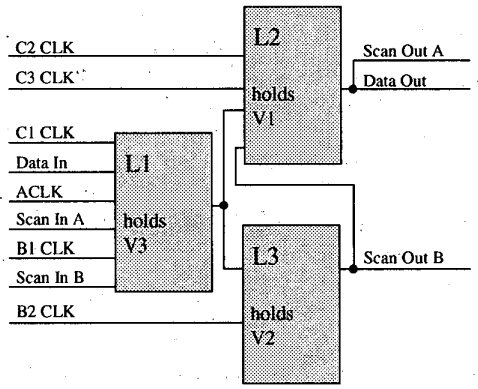

Figure 4. Scan Element 1

One of the advantages of scan element 1 is the number of latches used. However, the signals required for this implementation include one additional clock and one additional scan path relative to the two-pattern scan element. In addition, scan element 1 has two scan paths each the length in scan elements as a standard LSSD scan path. As a result of both parallel scan paths sharing a common latch (*L1's* in each element) the paths have to be scanned in separately, doubling the scan-in time for this technique.

4.2 Proposed Scan Element 2

A second approach trades area for fewer and less complicated signals. Scan element 2 is illustrated in Fig. 5. By using four latches, the same two clocks used for latches *L1* and *L2* can be used for latches *L3* and *L4* in scan mode. One additional clock (relative to the stuck-at test scan element) is necessary in this configuration, *C3 CLK*, and it is used to toggle the value of *V2* into *L2*. The *C2 CLK* is then pulsed to re-establish the value of *V1/V3* in *L2* to prompt the tested transition. *C1 CLK* is pulsed to capture the tested level at the latch terminating the path.

Although this method simplifies the clocking signals necessary for three-pattern delay testing, the additional latches increase the required area and the scan path length is doubled (assuming every path will be three-pattern delay tested), increasing test time required for scan-in. Note that not all scan elements in the scan path have to be implemented with this more elaborate scan element. Only those scan elements that source the paths to be delay tested require scan element 2. All other scan elements including the capture latches can be implemented with the standard LSSD scan element. If only a small fraction of the paths are selected for delay testing then it follows that the impact on scan length and the area overhead would be negligible. Furthermore, only one additional clock would be necessary for test purposes relative to the standard LSSD scan element.

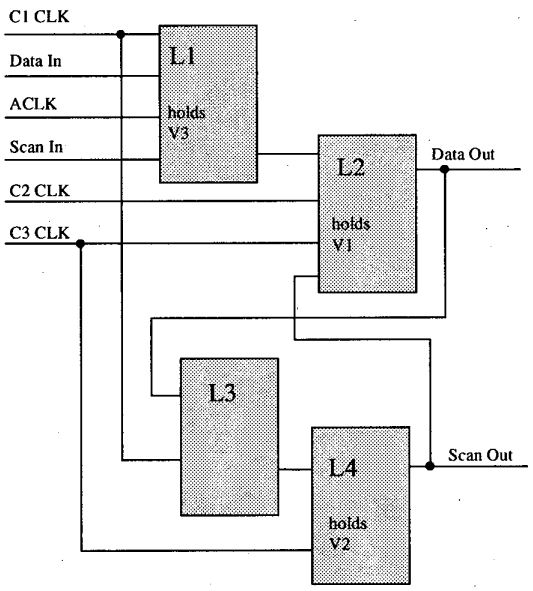

Figure 5. Scan Element 2

Table 2. Simulation Results

Path		Propagation Delay – Tplh [ps]			Propagation Delay - Tphl [ps]		
Benchmark	Length of Path in Gates	Worst-case Switching History	Fast-case Switching History	Percent Variation	Worst-case Switching History	Fast-case Switching History	Percent Variation
C432	20	1522	1404	7.7%	1243	1148	7.6%
C499	13	1773	1614	8.9%	1602	1479	7.6%
C1355	24	1683	1559	7.3%	1985	1817	8.5%
C2670	32	3092	2820	8.7%	2494	2207	11.5%
C3540	42	4231	3679	13%	3410	3108	8.9%
C5315	48	3110	2848	8.4%	3103	2812	9.4%

5. Simulations

Simulations were run to illustrate the need for testing under the worst-case switching histories using the proposed three-pattern delay tests. This was done using the University of Florida's SOISPICE4.5 [Fossum 94]. SOI spice models (based on a 0.18 μm PD-SOI technology) were created for the most critical path (determined through static timing analysis) of several benchmark circuits [Brglez 85]. The propagation delay in SOI circuits for two different switching histories were determined: the worst-case switching history (in terms of delay) and a switching history that approximates the best-case. The results are shown in Table 2. The name of the benchmark circuit is given followed by the number of gates along the critical timing path. The low-to-high and high-to-low propagation delays are shown for the best-case and fast-case switching histories in units of picoseconds. The percent variation due to the switching history is shown.

As can be seen from the results, the delay variation ranges from 7.3% to 13%. Note that this variation in delay is due to the floating body effect in SOI and does not occur in traditional bulk technologies. At-speed functional testing and traditional two-pattern delay testing do not consider the switching history and hence may test the path under fast-case conditions. The three-pattern delay tests proposed in this paper are needed to pre-condition the path so that it is tested under the worst-case switching history.

6. Conclusion

PD-SOI is clearly an emerging technology for high-performance, low-power digital applications and this paper has discussed the issue of delay variation in device testing. PD-SOI presents some serious challenges in terms of testing delays that are dependent on the switching-history of the device. Conventional functional testing does not address worst-case timing due to this history effect and new techniques must be employed to ensure testing of the worst-case conditions. It was shown that three-pattern delay tests where the V1 and V3 patterns are the same can be used to pre-condition a path for the worst-case switching history.

The three-pattern tests can be applied to the circuit-under-test using functional justification with a standard scan path (if possible) or by using the proposed scan elements. The proposed scan elements add additional overhead compared with standard scan elements. However, for test methodologies that require scan-based delay testing only on a small fraction of the worst-case delay paths, the cost in silicon area can be negligible by selectively replacing scan elements that launch the transition with new scan elements capable of implementing the proposed three-pattern test. This also results in less significant increases in scan-chain length, and consequently, scan-in times.

A recent paper [Canada 99] has described a PD-SOI fabrication process in which the order of influence of the different mechanisms that affect the body voltage had changed. All previously published literature describes the pulse-stretching scenario, however, after pre-conditioning transistors fabricated in the reported process, pulse-shrinking occurred, where the first edge delay increased relative to the second. In this case, a three-pattern test would not be required for pre-conditioning to the worst-case switching history. Traditional two-pattern delay testing could be used provided the first vector is held long enough to pre-condition the path to generate the worst-case propagation delays. Additionally, FD-SOI will eventually eliminate many of floating-body effects seen in PD-SOI, however, manufacturing problems associated with FD-SOI may take years to overcome.

Delay variation due to the history effect in PD-SOI will be even more pronounced as voltages are scaled in future technologies. This is due to the increased ratio of the threshold voltage variation to V_{dd}, and consequently, the complications of the history effect on delay testing will become one of the most substantial challenges faced by the SOI test community.

Acknowledgements

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