Delay Testing of Partially Depleted Silicon-On-Insulator (PD-SOI) Circuits

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***Abstract*—Partially depleted silicon-on-insulator (PD-SOI) technology has garnered more attention recently with regards to replacing traditional bulk-silicon technology as the mainstream technology of choice for high-performance/low-power digital applications. The increase in performance is due to the buried oxide layer, which provides a dramatic decrease in the source and drain junction capacitance, as well as a reduction in the traditional back biasing resulting from the body effect. The reported performance increases have been between 20% and 35%. However, this increase in performance comes at a cost of complexity from a performance measurement and delay testing perspective. Where the SOI transistor is faster than the bulk transistor, there exists a variation in delay caused by threshold voltage shifts that must be accounted for during manufacturing test. This paper explores these issues and proposes new test techniques for this promising technology.**

***Index Terms*—Delay testing, flip-flop design, silicon-on-insulator (SOI) testing.**

I. Introduction

PARTIALLY depleted silicon-on-insulator (PD-SOI) technology has become a leading candidate for replacing traditional bulk CMOS as the mainstream fabrication process for high-performance/low-power VLSI designs. Based on a reduction in diffusion capacitance, SOI provides a reduction in delay or a corresponding reduction in dynamic power consumption. Source and drain diffusion capacitance increases as the supply voltage is reduced in each new generation of bulk technology, consequently, this advantage of SOI becomes increasingly more attractive as we continue to scale technology. Furthermore, the isolation of the transistor body in SOI leads to several other advantages including the dynamic threshold voltage, the elimination of latch-up and a reduction of the soft-error rate [1]–[3].

As illustrated in Fig. 1, the most striking difference between traditional bulk and SOI technology is that the body of the SOI transistor is now dielectrically isolated from the substrate by a buried oxide layer. This gives rise to several advantages of SOI over bulk technology. The exposed area of the source and drain diffusions to the substrate is significantly reduced, virtually eliminating the diffusion capacitances in both of these nodes. This translates into a reduction of both delay and power consumption, particularly for paths that are not wire resistance–capacitance (*RC*) limited. Additionally, due to the isolation of the body, the body voltage is now floating and is established by a combination of leakages and capacitive coupling with the external connections of the transistor. In many cases, the floating body leads to enhanced performance by avoiding the reverse-biasing of the source to body junction, which occurs in bulk technology for high fan-in static circuits or pass transistor circuits. This reverse biasing—often referred to as back biasing—increases the transistor threshold voltage due to the body effect, and results in diminished drive capability. Moreover, the floating body can provide a dynamic threshold voltage effect, which describes how the threshold voltage is transiently decreased during switching (improving performance) and increased during the off state (improving leakage). Interestingly, the original motivation for SOI in the late 70s was related to the improvement in the soft-error rate necessary for space and military applications, and although these advantages are still relevant, they are eclipsed by SOI's performance and energy improvements essential for today's commercial applications.

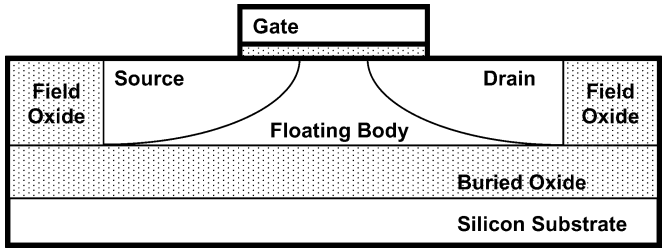

Fig. 1. Cross section of an SOI transistor.

Isolating the body of the SOI transistor, however, leads to complications for both design and test. As a result of the floating body, there now exists a relationship between the switching history of an SOI gate and the delay through the gate. The recent switching activity on the source, drain, and gate nodes of the transistor, affects the body voltage through capacitive coupling and junction leakage. Additionally, impact ionization from frequent switching generates charge in the body as well. Changes in the body voltage result in modulations of the threshold voltage, and these modulations, in turn, affect the delay through a transistor. Although the worst case delays are generally faster than equivalent delays in bulk technology, the variation of delay, which did not exist in bulk, poses some serious challenges for testing integrated circuits in SOI. New test techniques will be required to test critical paths with the worst case delays.

These problems can be addressed during the design phase with the use of body contacts. Body contacts are used to tie

Manuscript received September 15, 2003.

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Digital Object Identifier 10.1109/TVLSI.2006.878209

the body voltage to a static level (ground or $V_{\rm dd}$), however, they result in increased transistor area and eliminate the advantages of the floating body. Limited use of body contacts in some circuits, particularly PLLs, IOs, and sense amps, is inevitable. However, the vast majority of transistors in combinatorial logic and memories will be left floating. Consequently, the area and performance advantage of the floating body transistors can be amortized across the entire integrated circuit. Fully-depleted SOI (FD-SOI) eliminates many of these issues as well; however, manufacturing processes to date cannot produce the across-wafer tolerances necessary for the thickness of the active silicon layer. The threshold voltage is influenced by this thickness based on the amount of silicon volume available to deplete and, thus, FD-SOI cannot currently be used in mainstream applications until further progress is made. New band-gap engineering techniques are being explored in which metal gates are being used to further the case for fully depleted SOI; however, making the departure from 30 years of using poly-silicon gate material will require extensive manufacturing and reliability studies.

This paper is organized as follows. Section II discusses the impact of SOI on generic delay testing and describes a three-pattern scan-based delay test for providing the worst case switching history. Section III describes scan elements capable of implementing the proposed three-pattern test. Section IV furthers the discussion of the proposed three-pattern test in the context of very low-voltage testing illustrating the effectiveness in monitoring the hysteretic behavior of SOI integrated circuits. Finally, Section IV concludes the paper.

II. Delay Testing of SOI Circuits

A. Impact of SOI on Delay Testing

One significant challenge with testing integrated circuits fabricated in SOI is the history-dependent delay. Having a unique switching history, each path in a sequential circuit for a given application will have a different variation of delay. The enumeration of all possible switching histories for each path is impossible. However the switching histories for each path can be simplified to three possible initial states—OUT-HI, OUT-LO, and SSS [4], [5]. Simplifying the history into these three initial conditions, provides the means for manageable analysis of the impact of the switching history on device operation and testing.

Using a typical CMOS inverter as an example as illustrated in Fig. 2, the first state, OUT-HI, is static in nature and is characterized by a logic low input and logic high output for an extended period (much greater than the clock period). The body voltage of both transistors will reach a level between the corresponding source and drain due exclusively to reverse-bias leakage in the drain/body diode and forward-bias current from the source/body diode. With the output at a logic high level, the drain of both transistors is at $V_{\rm dd}$, consequently the level of the body voltage of the nFET approaches the cut-in voltage of the source/body diode while the pFET body voltage rests at $V_{\rm dd}$ ($V_s = V_b = V_d = V_{\rm dd}$). The threshold voltage of the nFET is, thus reduced relative to the bulk case (one of the advantages of SOI is the general reduction in delay due to the reduced V_t), while the threshold voltage of the pFET is—at least in the static sense—left at the bulk level. This combination of threshold voltages for the PFETs and NFETs tend to decrease the propagation delay for high to low transitions ($T_{\rm phl}$) to an approximate best case value and increase the propagation time from low to high ($T_{\rm plh}$) to a worst case value [5] until equilibrium levels are reached in subsequent switching.

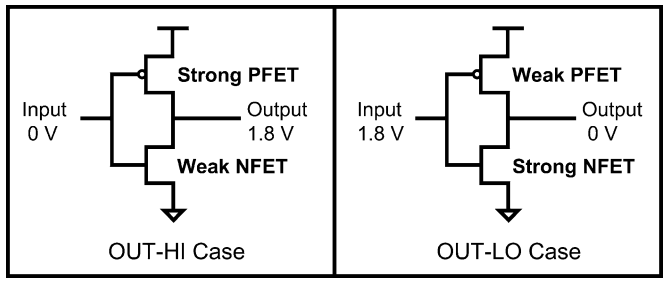

Fig. 2. Floating-body effects.

Conversely, the second case, OUT-LO, is where a static-logic high level is applied to the input, and the output is low for an extended period. The pFET body voltage will then be a potential barrier drop from $V_{\rm dd}$, while the nFET body voltage will rest at ground. This results in delays opposite to the OUT-HI state, fast $T_{\rm plh}$ and slow (worst case) $T_{\rm phl}$.

The third state, switching steady state (SSS) case , is characterized by a continuous oscillation of the input at the clock frequency. In this simplification, the body voltages of both the pFET and nFET transistors reach an average equilibrium level. For the nFET, the average body voltage is typically higher than the ground reference as is used in bulk technology, and consequently, the threshold voltage is lower than bulk. The dynamic level of the body voltage results from several complicated mechanisms, including capacitive coupling with the gate/source/drain, reverse-bias leakage in the source/drain junctions, forward-bias injection of carriers, recombination, and impact ionization. Similarly affected, the body voltage of the pFET is lower than $V_{\rm dd}$ as in the bulk case, and the threshold voltage is reduced below that of bulk to an equilibrium level as well. Additionally, in the SSS case, the body voltages tend to a higher equilibrium value at higher frequencies based on an increase in impact ionization due to more frequent switching. This increase in body voltage could possibly result in shorter delays then described in the faster transitions in the two static cases. However, the worst case transitions for $T_{\rm plh}$ and $T_{\rm phl}$ are bound by states OUT-HI and OUT-LO, respectively, because they effectively represent the SSS case with an infinite period.

By simplifying each path's history into three possible initial states, the impact of the floating body on the delay through a path can be intuitively understood. All switching histories can be approximated by these simplified cases. A gate with inputs remaining inactive for some time frame would be approximated by one of the two static cases OUT-HI or OUT-LO, depending on the value of the outputs. All other gates with actively switching inputs would be approximated by the SSS case. The time frame used to define inactivity depends on the time constants of the mechanisms that affect the body voltage. The time constants are different for each unique SOI fabrication process, but could be in the order of hundreds of clock cycles.

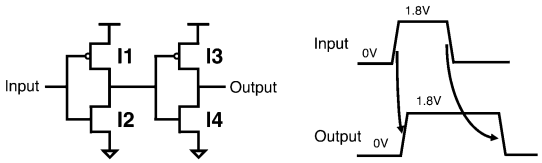

Fig. 3. Pulse stretching.

A switching history that can be approximated by OUT-HI, provides best case $T_{\rm phl}$ and worst case $T_{\rm plh}$, while OUT-LO provides the reverse. The SSS case generally provides propagation delays that fall between the other two extremes (although it can provide best case values at high frequencies due to increased impact ionization).

Having discussed the three possible initial conditions, pulse stretching can now be described. Fig. 3 illustrates a two-inverter buffer. In this depiction, the first inverter, transistors $I1$ and $I2$, is preconditioned with the input low and output high, thus, it is in the OUT-HI state. The input of the second inverter, transistors $I3$ and $I4$, is high and the output is low. Consequently, the nFET $I1$ is "strong" while the pFET counterpart $I2$ is "weak" due to variation in threshold voltage. Conversely, the field-effect transistors (FETs) $I3$ and $I4$, are reversed in strength relative to $I1$ and $I2$ due to the opposite preconditioning. Subsequently, if a pulse is applied to the input, the $I2$ nFET and $I3$ pFET are activated, and due to the reduced threshold on these transistors, the transition propagates quickly through the buffer. However, when the input is returned to a logic low state, the $I1$ pFET and the $I4$ nFET are activated and the delay is aggravated by the lower drive capability, resulting in a worst case delay. This extended delay and stretched pulse is highlighted in Fig. 3.

During typical functional testing of integrated circuits, a majority of the paths are switching with an average frequency that is less than the clock frequency but much faster than the time frame defining inactivity and, hence, would be approximated by the SSS case. As described before, the SSS case would not provide worst case delays for most paths, and consequently traditional at-speed functional testing could not guarantee worst case operation. This is a problem because the device may be operated in the field in such a way that the worst case switching history may arise resulting in device failure (i.e., the delay along a path may be longer than the clock period). New approaches for testing will be necessary in that of precondition paths for worst case delays.

Complicating matters further—for more recent scaled technologies (0.13 μm and beyond)—there are reports of "pulse-shrinking" behavior, where the first switch after preconditioning is the worst case (slowest), as opposed to the second switch—traditionally described as the slowest. Reference [6] was the first paper to use the phrase "pulse shrinking" to describe an SOI technology and described how for some scaled SOI processes the capacitive displacement currents from the drain to the body, had increased in influence relative to the capacitive displacement currents from the gate to the body. In the case of an nFET in our example inverter, as the gate node asserts, the body is capacitively coupled upward. However, as soon as the channel is formed ($V_{\rm gs} > V_t$) under the gate oxide, this body is shielded from further coupling to the gate. Simultaneously, the drain begins to drop in voltage and the junction capacitor between the drain and body causes the body voltage to drop. Thus, the first rising edge of a pulse would occur while the body is coupled down (increasing the threshold voltage) and the opposite is true for the second switch, which enjoys increased performance due to the decreased threshold voltage. However, the fact that SOI technologies can be of one of two varieties (shrinking or stretching) is further complicated by the fact that under specific conditions (input transition time, output loading, and supply voltage) a path can switch from one type to the other. This is because decreased input transition times result in more gate-to-body coupling while larger output loads result in smaller dv/dt on the drain node and consequently reduce the coupling of the drain to the body. In fact, a chip could have paths classified as "stretching" in some conditions and "shrinking" for others. The implication to path delay testing is that the behavior of the path must be identified (shrinking or stretching) to select the most effective testing technique in light of the hysteretic effects of SOI technology.

B. Three-Pattern Delay Testing With Preconditioning

To test the worst case propagation delay through a path defined as a stretching path, a three-pattern test will be required. Three-pattern tests have previously been used to initialize the state of a gate or provide transitions on multiple inputs [7]. In the case of SOI, this method is required to provide preconditioning for the functional path under test. $V1$ is the preconditioning vector and is applied to the path for the time frame necessary for the OUT-HI or OUT-LO conditions to become valid. $V2$ is applied to initialize a transition and is held for a sufficiently long period so that the signal can stabilize at the capture latch input. The application time of $V2$ should not exceed a single clock cycle due to the reduction of the impact of preconditioning on the path. Subsequently, $V3$ applies the logic value that prompts the transition to be tested. This three-pattern sequence results in the pulse-stretching scenario previously described and provides the worst case delay for the transition of the data path.

As a consequence of $V1$ and $V3$ being equal for the pulse-stretching test method, implementation of the three-pattern test can be simplified relative to general three-pattern testing. Test vector generation for the proposed test method is compatible with existing two-pattern test generation software. Effectively, $V2$ and $V3$ of the proposed method, are analogous to $V1$ and $V2$ of a traditional two-pattern delay test. Conveniently, $V3$ shares the same value as the preconditioning vector $V1$. Table I summarizes the relationship of the vectors of both the traditional two-pattern delay test with the proposed pulse-stretching three-pattern delay test for SOI.

In those cases where a path can be guaranteed to only pulse shrink for all conditions, a traditional two-pattern delay test can be used. However, to ensure worst case delays, the path must still be preconditioned. By avoiding the need for a three-pattern delay test, the complexity of implementing delay testing in SOI circuits is greatly reduced, however the penalty of increased test time can not be avoided due to the preconditioning requirement. In general, recent scaled SOI technologies (0.13μm and beyond) tend to be pulse shrinking in nature and also will likely require less preconditioning time as body volume decreases and the body charging leakages increase in magnitude. Thus, delay-

TABLE I
VECTOR COMPARISON OF TRADITIONAL AND PROPOSED DELAY TEST

	Traditional Two-Pattern Delay Test	Proposed Three-Pattern Delay Test for SOI Ics
V1	Initializes the transition	Preconditions the data path
V2	Launches the transition	Initializes the transition
V3	Not Applicable	Launches the transition

testing circuits in future technology generations, will tend to be less complex and require less time to implement.

C. Test-Pattern Generation for Three-Pattern Tests

Given that three-pattern delay tests are required for testing pulse-stretching SOI circuits, the question then is how to apply such tests. Some complications arise when extending the conventional techniques for applying two-pattern delay tests for three-pattern testing. Two-pattern delay tests are applied using a conventional scan chain by either "scan-shifting" or "functional justification" [8]. Extending either approach to generate three pattern tests is a natural extension to the capability of currently available tools with the exception of an increase in the complexity of the problem.

Scan-shifting involves shifting the $V1$ pattern into the scan chain and then generating the $V2$ pattern by a 1-bit shift of the $V1$ pattern. Extending scan-shifting for the proposed three-pattern tests, would require that a second bit shift of the $V2$ pattern would be used to generate a $V3$ pattern with the additional restriction that $V3$ equals $V1$ (at least for flip-flops that source the tested paths). This restriction confines the search space and consequently would increase the complexity of the automatic test-pattern generation (ATPG) problem and may decrease fault coverage.

Functional justification involves shifting the $V1$ pattern into the scan chain and then generating the $V2$ pattern through the functional logic in the next clock cycle. This requires ATPG across two periods, which again would lead to increasing the complexity of the test-pattern generation. Functional justification would be more suitable for the proposed three-pattern test than scan-shifting would be, as more options would exist for maintaining the $V1/V3$ relationship. However, neither method is optimal and both would result in loss of fault coverage relative to traditional two-pattern tests.

An alternative to functional justification, is to use enhanced scan elements, which contain additional latches and can completely eliminate the additional ATPG complexity introduced by the proposed three-pattern delay test. Enhanced scan element designs have been proposed for two-pattern delay testing [9]–[11]. The idea is to add an extra latch to the scan element so that both the $V1$ and $V2$ patterns can be stored and applied in succession. In Section III, two new scan elements are proposed that can provide the three-pattern test necessary to exercise SOI in the worst case conditions. These designs exploit the fact that the $V1$ and $V3$ vectors are the same to minimize the area and number of control signals. Furthermore, the proposed flip-flop—although larger than traditional versions—is only necessary at the source of the paths to be tested and, thus, can be amortized across the entire design.

D. Simulation Results

Simulations were run to illustrate the need for testing under the worst case switching histories using the proposed three-pattern delay tests, and preliminary results were reported in [12]. This was done using the University of Florida's SOISPICE5.0 [13] SOI spice models (based on a 0.18-μm PD-SOI technology) were created for the most critical path (determined through static timing analysis) of several benchmark circuits [14]. The propagation delay in SOI circuits for two different switching histories were determined: the worst case switching history (second switch after inactivity) and a switching history that approximates the best case (first switch). The results are shown in Table II. The name of the benchmark circuit is given followed by the number of gates along the critical timing path. The low-to-high and high-to-low propagation delays are shown for the worst case and fast case switching histories in units of picoseconds. The percent variation due to the switching history is shown as well. As can be seen from the results, the delay variation ranges from 7.3% to 13%. Note that this variation in delay is due to the floating-body effect in SOI and does not occur in traditional bulk technologies. At-speed functional testing and traditional two-pattern delay testing, do not consider the switching history and hence may test the path under fast-case conditions. The proposed three-pattern delay test is therefore necessary for pulse stretching technologies to precondition the path to ensure testing under the worst case switching history.

III. SCAN ELEMENTS CAPABLE OF PROPOSED TEST

For comparison purposes, a brief description of the operation and design of both a standard scan element, as well as an enhanced two-pattern delay test scan element are presented, followed by the proposed scan elements. Fig. 4 illustrates the standard scan element used in Level-Sensitive Scan Design (LSSD) [15]. In system mode, a two-phase clocking scheme is used with clocks $C1$ and $C2$ for the master and slave latches, respectively, while *ACLK* is left at a logic low. In test mode, *ACLK* and $C2$ are alternately pulsed to scan values through the scan path and, once complete, $C1$ captures the value from the tested data path.

The two-pattern delay test-scan element proposed in [16], is shown in Fig. 5. (The scan element has been modified for a two-phase clocking scheme for comparison purposes with the two proposed scan elements.) An additional latch is introduced relative to the standard LSSD element in Fig. 4. This permits the storage of test vectors $V1$ and $V2$, as described previously. In system mode, clocks $C1$ and $C2$ are used to exercise latches $L1$ and $L2$ as a flip-flop, while all other clocks are held low. In scan mode, the master-load (*ML*) signal is asserted while *SI_CLK* and *SO_CLK* are alternately pulsed, scanning in the final value vector $V2$. The scan path traverses through $L2$ and $L3$, but with *ML* asserted, $L1$ also captures the value of $V2$. A second scan operation is completed with ML deasserted, which isolates $L1$ from the initial value vector $V1$, as it is scanned through $L2$ and $L3$. Once complete, the initial value is stored in $L2$ and the

TABLE II
PATH DELAY SIMULATION RESULTS

Path		Propagation Delay - Tphl (ps)			Propagation Delay - Tphl (ps)		
Bench-mark	Length of Path in Gates	Worst-case Switching History	Fast-case Switching History	Percent Variation	Worst-case Switching History	Fast-case Switching History	Percent Variation
C432	20	1522	1404	7.70%	1243	1148	7.60%
C499	13	1773	1614	8.90%	1602	1479	7.60%
C1355	24	1683	1559	7.30%	1985	1817	8.50%
C2670	32	3092	2820	8.70%	2494	2207	11.50%
C3540	42	4231	3679	13%	3410	3108	8.90%
C5315	48	3110	2848	8.40%	3103	2812	9.40%

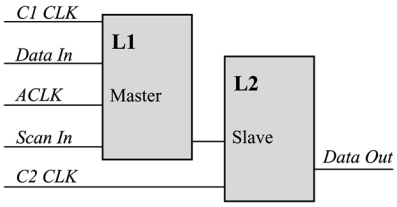

Fig. 4. Standard LSSD scan element.

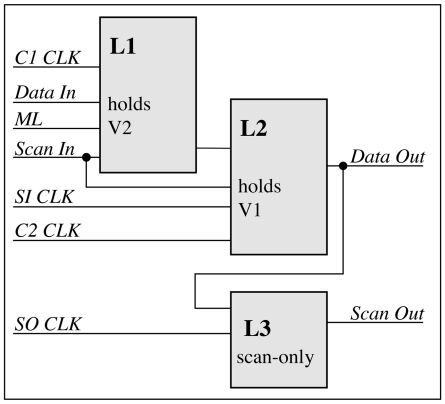

Fig. 5. Two-pattern delay test-scan element.

final value in $L1$. System clocks are then used to complete the traditional two-pattern delay test.

A. Proposed Scan Element 1

Fig. 6 illustrates the first of two proposed scan elements capable of implementing the three-pattern SOI test method, scan element 1. In system mode, clocks $C1$ and $C2$ are used together in a two-phase clocking scheme. All other clocks are with *Data In* as the input, *Data Out* as the output. There are two scan modes, A and B, which are used to shift in the $V2$ and $V3$ values independently and comprise two parallel scan paths with the $L1$ latch common to both. Scan path B is used to shift in the value of $V2$ into $L3$. This is accomplished by alternately pulsing the *B1 CLK* to capture *Scan In B* into $L1$, and pulsing the *B2 CLK* to transfer the $L1$ value into $L3$. Subsequently, scan path A is used to shift in the value for $V1/V3$ into latch $L2$. By alternately pulsing the *ACLK* and the *C2 CLK*, the values are shifted while maintaining the previously scanned value of $V2$ in $L3$.

Once the $V1/V2/V3$ vectors have been established, the logic level of $V1$ is applied to the data path for an extended period of

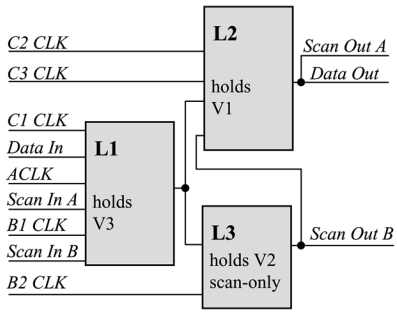

Fig. 6. Proposed scan element 1.

time for preconditioning. The $C3\ CLK$ is toggled to transfer the $V2$ value stored in $L3$ into $L2$ and, consequently, the $V2$ value is presented to the functional path. This initializes the path for the transition to be tested. By pulsing the $C2\ CLK$, the value of $V3$ held in $L1$, is transferred to $L2$ and provides the logic value necessary to transition the path. $C1\ CLK$ is pulsed to capture the data at the input of the latch that terminates the path. The operation is done in the time frame dictated by the delay value to be tested, $C2\ CLK$ rise (launching the value of $V3$ into the data path) to the fall of $C1\ CLK$ (sampling the value at the input of the capture latch).

One of the advantages of scan element 1 is the number of latches used (only one additional latch). However, the signals required for this implementation include one additional clock and one additional scan path relative to the two-pattern scan element. In addition, scan element 1 has two scan paths each the length in scan elements as a standard scan path. As a result of both parallel scan paths sharing a common latch (L1 latches in each element), the paths have to be scanned in separately, doubling the scan-in time for this technique.

B. Proposed Scan Element 2

A second approach trades cell area for fewer and less complicated signals, as well as the ability to intermix these elements with standard scan elements. Scan element 2 is illustrated in Fig. 7. By using four latches, the same two clocks used for latches $L1$ and $L2$ can be used for latches $L3$ and $L4$, respectively, in scan mode to establish the $V1/V2/V3$ vectors into the appropriate latches as shown in the figure. One additional clock (relative to the stuck-at test-scan element) is necessary in this configuration—$C3\ CLK$—and is used to toggle the value of $V2$ into L2 to initialize the transition after preconditioning. The

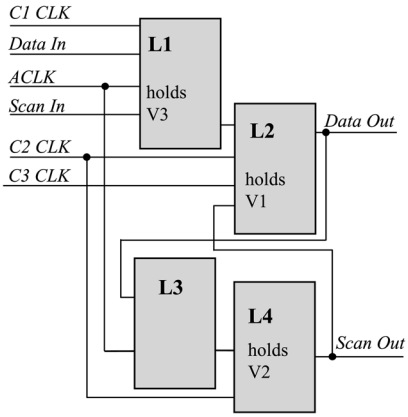

Fig. 7. Proposed scan element 2.

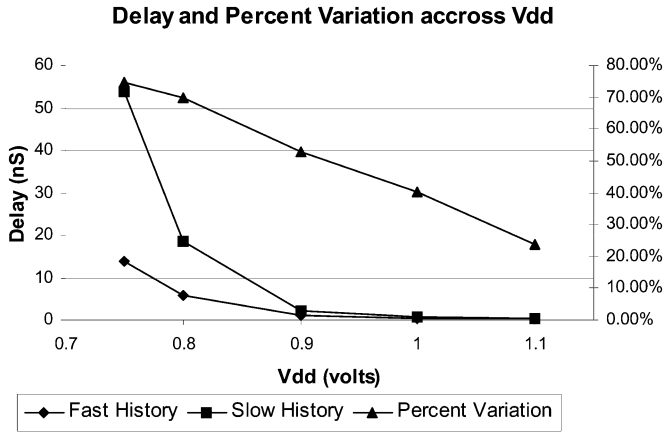

Fig. 8. Delay versus supply voltage for different histories.

$C2\ CLK$ is then pulsed to re-establish the value of $V1/V3$ in $L2$ to prompt the tested transition. Subsequently, the $C1\ CLK$ is pulsed to capture the tested level at the latch terminating the path.

Although this method simplifies the clocking signals necessary for three-pattern delay testing, the additional latches increase the required area and the scan path length is doubled (assuming every path will be three-pattern delay tested), increasing test time required for scan-in. Note that not all scan elements in the scan path have to be implemented with this more elaborate scan element. Only those scan elements that source the paths to be delay tested require scan element 2. All other scan elements including the capture latches can be implemented with the standard LSSD-scan element. If only a small fraction of the paths are selected for delay testing, then it follows that the impact on scan length (and corresponding test time) and the area overhead would be negligible. Furthermore, only one additional clock would be necessary for test purposes relative to the standard LSSD-scan element.

IV. VLV Testing of SOI ICs

The sensitivity of a transistor's performance to V_t fluctuations increases as $V_{\rm dd}$ is lowered in either bulk or SOI technology and this is one of the motivations for employing very low voltage (VLV) testing [17]–[19]. This increased sensitivity can be seen intuitively from the classic drive current equation shown as (1), where the parenthetic term approaches zero as $V_{\rm gs}$ approaches V_t—given that $V_{\rm gs}$ is bound by $V_{\rm dd}$. The transistor drive current $I_{\rm ds}$, is directly proportional to the performance of a transistor and (1) implies that $V_{\rm dd}$ must be greater than V_t to generate more than subthreshold current (leakage). As $V_{\rm dd}$ is lowered and approaches V_t, the sensitivity of the delay through a circuit to shift in the threshold voltage, increases significantly and this increased sensitivity can provide a mechanism for monitoring the extent of the history effect in SOI circuits

$$I_{\rm ds} = \frac{1}{2} \cdot K \cdot C_{\rm ox} \cdot (V_{\rm gs} - V_t)^2. \tag{1}$$

The history effect manifests itself as local shifts in threshold voltages—temporal increases or decreases—and has a negligible impact on the operation of a defect-free circuit designed with special attention given for the floating body and fabricated within the specified window of process parameters (i.e., doping, lithographic dimensions, etc.). However, minor variations in several contributing parameters, could conspire to increase the influence of the switching history on device operation and result in intermittent failures or degraded performance under specific data-dependent applications. Furthermore, some defects may promote the history effect causing local increases in the extent of the SOI-specific delay variation. These defects could include resistive shorts between any of the transistor's nodes and the body, increasing the influence of the affected node over the body voltage, and consequently, aggravating the history effect. Since this variation is data and history dependent, it may be difficult to identify parts that will fail for performance-related reasons due to test vectors not exercising critical paths under the worst case history. By ensuring that the extent of the history effect is within a specified level on a set of paths that is representative of the entire device, unexpected failures relating to history effect can be avoided.

A. History-Effect Monitor at VLV

Monitoring the history effect under normal operating conditions (voltage and temperature) is difficult at best for today's high-performance devices. By applying delay tests in the VLV regime, the delays and the delay variations become much more significant and easier to measure. Furthermore, by performing delay tests at low voltages on both edges of a preconditioned pulse, the worst case (slow) history delay and also a fast history delay for the same path can be measured—regardless of the technology being of the stretching or shrinking variety. Having measured path delays under two switching histories allows the percent variation to be calculated for the path-under test. This percent variation is the most directly representative value of the history effect in SOI. Fig. 8 illustrates this for the series of inverters. Clearly, as $V_{\rm dd}$ is decreased both the absolute magnitude of the delay, the magnitude of the difference of delays for different switching histories, and the percent variation all increase, and thereby allow for devices with increased history influence to be detected.

The simulations in this section all were done with Spice2 using the University of Florida's SOISPICE5.0 models. All inputs and outputs were properly buffered and the simulations

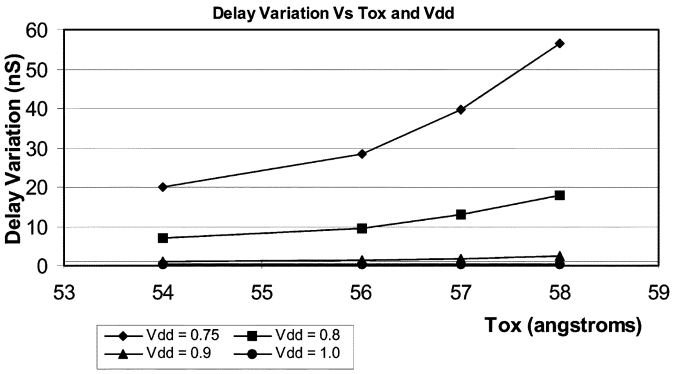

Fig. 9. Delay variation versus $T_{\rm ox}$ and $V_{\rm dd}$.

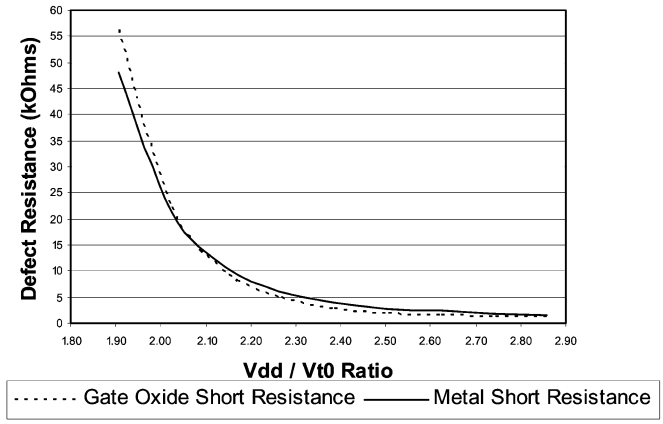

Fig. 10. Defect resistance detected versus $V_{\rm dd}/V_t$ ratio.

were extended to 500 ns to verify if results would also apply to dc testing. Similar results were also generated using the partially-depleted SOI models from the Device Group at the University of California at Berkeley BSIMPDV2.2.2 compiled with SPICE3F. Preliminary results were reported in [20].

Several papers have been published that discuss the suppression of the history effect, attempting to minimize—not eliminate—the extent of the variation of delay to manageable levels through device and circuit engineering [4], [21]. The use of VLV testing can be used in conjunction with these techniques to ensure that the extent of the history effect is within specification. The sensitivity of the history-dependent fluctuations in the V_t can be amplified without the need for higher performance test equipment, and thus, devices with a history dependence that is out of specification, can be identified more easily. As an example, Fig. 9 describes the delay variation for the series of inverters across a range of gate oxide thickness $(T_{\rm ox})$, a tightly controlled process parameter, which influences the history effect. For these simulations models, $T_{\rm ox}$ is set to a nominal 56 Å and Fig. 9 illustrates how a change as small as a single angstrom can influence the history effect significantly at very low voltages. The history dependence increases as the ratio of Cgb to Cdb is reduced [22] and the gamma coefficient of the body effect is increased with increased $T_{\rm ox}$. Although the corresponding increase in the history effect at nominal voltages is difficult to measure based on the small magnitude of the delay variation, it may be enough to cause intermittent failures as untested, close-to-critical paths are extended past the functional cycle due to the history dependence.

B. Traditional VLV Testing of SOI Circuits

In [17], a methodology was described for 0.8- and 0.6-μm bulk technology for the selection of an effective $V_{\rm dd}$ for VLV testing. The range of $V_{\rm dd}$ was established by considering the tradeoffs between flaw coverage (resistance of defect detected), test time, and noise margins. For these technologies, the acceptable range of supply voltage was based on a ratio with the threshold voltage. The case of SOI technology, however, is complicated by the fact that the threshold voltage is dynamic and depending on the switching history, each transistor has a unique value. Threshold voltages, in general, can range from 0 V (very high body-to-source voltage) to near the nominal value, V_{t0} (body to source voltage equals zero). For delay testing in the VLV regime, the use of the same original guidelines using a ratio of $V_{\rm dd}$ with the nominal threshold voltage is appropriate if the switching history is accounted for by using the techniques described in [12] for delay testing. Otherwise, the effectiveness of VLV delay testing may be compromised for cases where the threshold voltages are reduced, and in fact, defects that are deemed detectable by delay testing may become less manifest in the VLV regime than under normal operating conditions.

In [17], two sets of tests were simulated: 1) a NAND gate with a gate oxide short and 2) a metal short between two outputs of inverters in separate inverter chains. Acceptable flaw coverage (resistance detected) in the case of both gate-oxide shorts and metal-resistive shorts, was targeted to be at least 5 Kω, which represents the vast majority of both of these defect types. This provided an effectiveness metric that determined the upper end of an acceptable range of supply voltage values for very low-voltage testing. Similar simulations were performed with SOI models using the same tests and the results generally agree with the conclusions drawn in the previous report. In SOI technology, the supply voltage should be no higher than 2.25 times the threshold voltage to provide comparable flaw coverage to that reported in [17], as illustrated in Fig. 10. The reduction in the upper limit from 2.5 to 2.25 can be accounted for by the general reduction in V_t for the SOI circuits. In tests, the static input values tend to cause the active transistors to approach but never quite reach the nominal V_t. Thus, the ratio of $V_{\rm dd}$ to V_t is more conservative for this technology.

To determine the lower limit of the supply voltage, noise margins and test time were considered. From Fig. 10, it is clear that approximately two times the nominal threshold voltage ($V_{t0} = 0.42$ V in SOI simulations), is where delays begin to increase significantly for SOI. Any increase in delay for a good device must be accounted for and reconciled in the test frequency of the very low-voltage testing, and undue increases will increase the overall test time of the device. This, of course, results in increased cost. Therefore, SOI is similar to the technologies described in [17] and the lower limit of the supply voltage should be maintained above two times the nominal threshold voltage based on test-time considerations. When considering the role of noise margins in determining the lower limit, more care should be taken. The virtual elimination

of parasitic junction capacitance in SOI, results in a substantial decrease in the inherent decoupling capacitance on-chip necessary to reduce ground bounce and $V_{\rm dd}$ droop in the CMOS circuits and there is a slight reduction in the noise margins of SOI circuits, in general [23]. However, these issues can be resolved with good design practices and on-chip decoupling capacitors. Consequently, noise margins considerations are roughly the same as the original report and do not conflict with the lower limit of the supply voltage being set to two times the nominal threshold voltage for very low-voltage testing.

Reference [2] discusses the effects of temperature on the history effect in SOI, and describes how as the temperature is increased, the history effect is diminished as the body voltages tend to be forced to the slow/high V_t corner due to increased leakage and electron–hole generation in the body. Given that traditional VLV defects are generally aggravated at higher temperatures, traditional VLV tests should then be performed at the highest specified temperature allowed for the technology. This may allow for the elimination of preconditioning paths if the temperature can be raised sufficiently to minimize the history effect to negligible levels. Conversely, for the proposed hysteretic monitoring test, the temperature should be reduced to the lowest possible level to increase the history effect and improve the probability of detecting devices that are out of specification with regards to the influence of the floating body on the performance of the circuit.

V. Conclusion

This paper has explored and addressed many of the testability concerns for circuits fabricated in partially depleted SOI technology, and prior to this work, few papers have explored these test issues. The main design and device consideration that was addressed in the context of testability, was related to the PD-SOI floating-body effects—specifically the hysteretic delay as described in Section II, which identified the ineffectiveness of traditional delay testing at screening SOI circuits under the worst case switching history. The work described a potential absence of performance screening if the assumptions used in previous bulk technologies were applied to testing SOI circuits. A three-pattern delay test with preconditioning was proposed to ensure that devices would be tested under all possible data-dependent switching. In Section III, scan element designs were described that could implement the proposed delay test with a minimum of area and routing overhead. In Section IV, the subject of the floating-body effects was further explored in terms of VLV testing, which could be used to measure the extent of the hysteretic variation of threshold voltage in SOI circuits. It was shown that the sensitivity of performance to threshold shifts increases dramatically as the supply voltage is lowered and this can be used to identify devices in which the history effect is out of specification. A targeted range for the supply voltage for use with VLV tests, was determined based on noise margin, test time, and the effectiveness at detecting metal- and gate-oxide shorts. The range was more restrictive than that established in previous evaluations for two bulk technologies, which is intuitive given that the range is based on the ratio of $V_{\rm dd}$ to V_t, and in SOI technology, the V_t values are dynamic.

Acknowledgment

The authors would like to thank Prof. J. Fossum at the University of Florida, Gainesville, and the Device Group at the University of California, Berkeley, for providing the SOI Spice models.

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